Cat. No. 26-5404

$19.95

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1/ Introduction

The Tandy Model 2000 Personal Computer is modular in design to allow maximum flexibility in system configuration. The basic computer consists of a Main Unit, a detached keyboard with coiled cable for positioning the keyboard in the most convenient location, and a monitor. The Main Unit may be supplied with two internal floppy disk drives or one floppy disk drive and one internal hard disk drive. The standard monitor used with the Model 2000 is a monochrome display (green phosphor) which has a standard screen format of 80 characters width and 25 lines vertical. Since this unit is modular, it may be placed on top of the Main Unit or at any location convenient to the operator.

Internal floppy diskette storage is provided by either one or two 5-1/4" floppy disk drives. If the unit is supplied with two of these units, total internal memory storage capacity is 1.46 Mbytes. When supplied with the internal hard disk and one floppy disk storage unit, total internal memory storage becomes 10.73 Mbytes.

An optional Color Monitor may be used with the Model 2000 to provide up to eight of sixteen different colors on the screen at one time. This optional feature requires the use of a color monitor PCB assembly which plugs into one of the mother board slots at the rear of the Main Unit.

An internal 128K RAM board is standard on the Model 2000. An option to the Model 2000 is an additional 128K RAM board which provides expansion to 256K. Both boards are mounted internal to the Main Unit. An additional optional feature is a 256K RAM board which connects to the internal motherboard of the Main Unit. It is populated with 128K RAM which may be expanded to 256K RAM with the addition of RAM ICs. Two of these boards can be installed into the motherboard in the unit's card cage assembly. With all these options installed, the Model 2000 then has internal RAM memory capacity of 768K bytes.

Other options include, a mouse/clock option which allows input from a hand-positioned interface, a monitor pedestal, black and white graphics option, and a floor unit which mounts the Main Unit vertically.

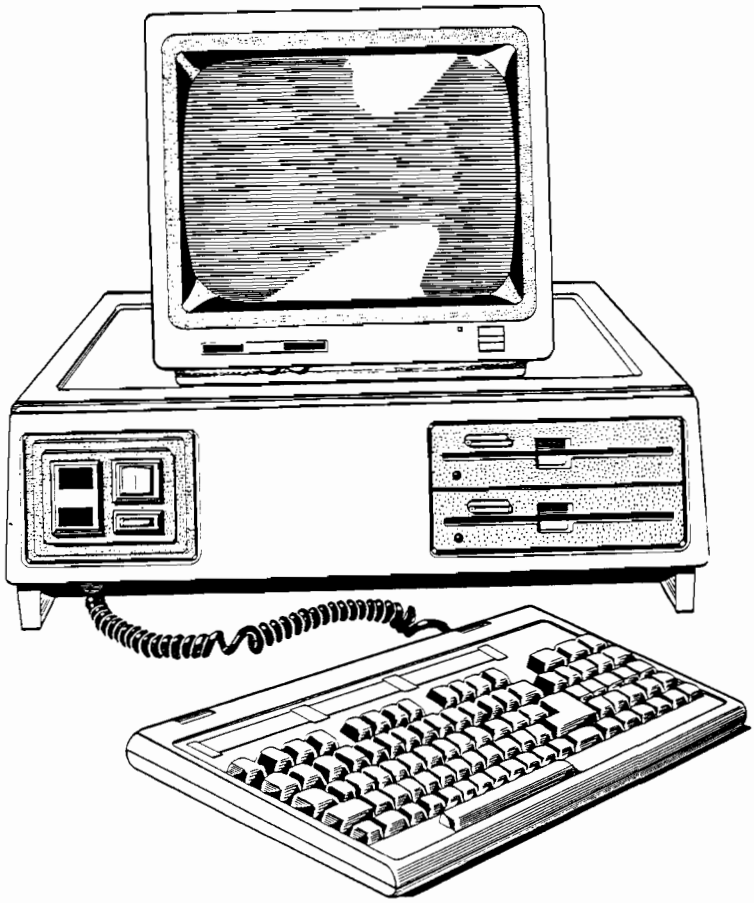


Figure 1.1 Model 2000 Computer Assembly

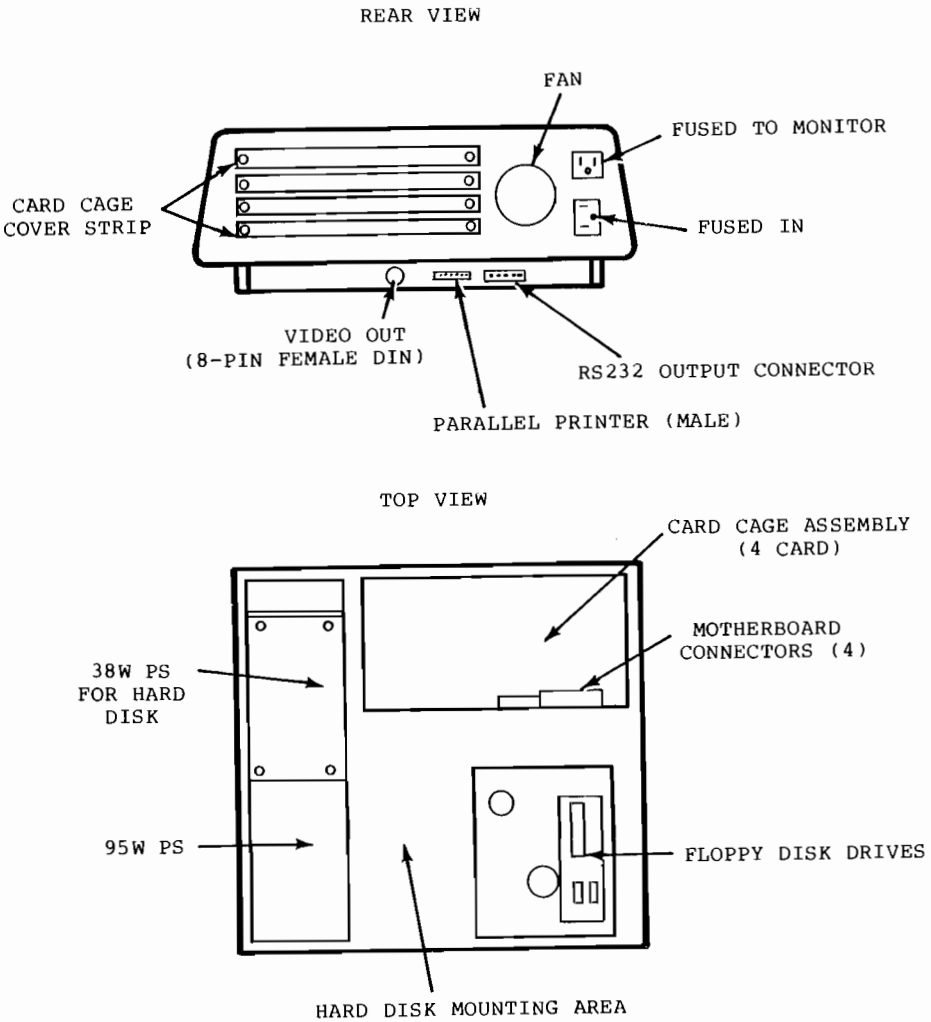


Figure 1.2 Model 2000 Major Component Subassemblies

The Main Unit is the heart of the Tandy Model 2000 microcomputer. It houses the microprocessor, Read-Only Memory (ROM - 16K for system start-up), system power supply, RAM boards and expansion slots for optional features, floppy disk drives (either one or two), and the internal hard disk drive and power supply.

The Main Logic Assembly is a large board mounted to the bottom of the Main Unit and interconnected to the keyboard, power supply, motherboard, and disk drives by a series of cables. A system block diagram is shown in Figure 1-1 showing the major components of the Model 2000 and the interconnecting cables. Both standard and optional features are included in this figure to provide a complete overall interconnection diagram of the unit.

The standard Power Supply for the Model 2000 microcomputer is a 95W switching regulator type, designed to provide adequate capacity for most all add-on features of the computer. When the system is supplied with the hard disk option, however, an additional 38W power supply is required to power the hard disk assembly separately.

The Model 2000 has a detachable keyboard which is connected to the Main Unit with a lightweight coiled cable which allows the keyboard to be used up to 3 feet away from the Main Unit for operator convenience. The keyboard features 90 keys in a standard typewriter keyboard layout with additional keys for numbers and functions.

The Floppy Diskette Drive uses special 5-1/4" double-sided, double-density diskettes to read, write or store data. These are 96 TPI soft sector diskettes. Two Disk Drive assemblies are installed in the standard unit, or it may contain one floppy disk drive and one internal hard disk drive assembly. Each of the floppy diskettes stores approximately 730 Kbytes of data. The hard disk drive is capable of storing 10 Mbytes of data. All system programs, with the exception of the system startup sequence, are stored on diskette.

The monitor used on the Radio Shack Model 2000 may be either a monochrome (#26-5111) or color (#26-5112) display. The monochrome monitor is a high resolution green phosphor display which provides excellent visual quality. It features a 12" screen with an anti-glare surface for improved viewing. The display is 25 lines of 80 characters each with the capability of displaying 256 different letters or characters. The characters are formed using a 7 x 9 matrix dot pattern.

Also available as an enhancement of the black and white monitor is a B/W graphics option board (26-5140). This feature allows the presentation of graphic material on the display monitor with individually addressed pixels. A color monitor (26-5112) is available which utilizes a 14" color screen, a color graphics option (26-26-5141), and the B/W graphics option to provide 8 color presentations at one time on the monitor.

Standard internal RAM memory consists of a plug-in 128K board. This board plugs into the Main Logic board and may be expanded to provide 256K of RAM with an additional 128K board (26-5160). In addition to this memory up to two 26-5161 boards (considered external since they are accessible from the outside of the Main Unit) may be plugged into the motherboard located at the rear of the Main Unit. These boards are populated with 128K of RAM and may be further expanded to 256K each with additional 64K x 1 RAM chips (option 26-5162). When all of these boards are incorporated into the system, they provide a total RAM capacity of 784K bytes of memory.

The Mouse/Clock option board allows input with an external input device called a "mouse" as well as providing the time of day with a battery backup clock/calendar chip. The mouse is a unit which is rolled along a desk top and encodes a digital input to the computer.

A built-in RS-232 asynchronous interface allows communication with external devices through the use of a modem. These devices may be local or remote, using a telephone line to co'm@unicate. The option supports 50 to 9600 BPS transmission speeds and utilizes a 25-pin D connector located on the rear panel of the Main Unit.

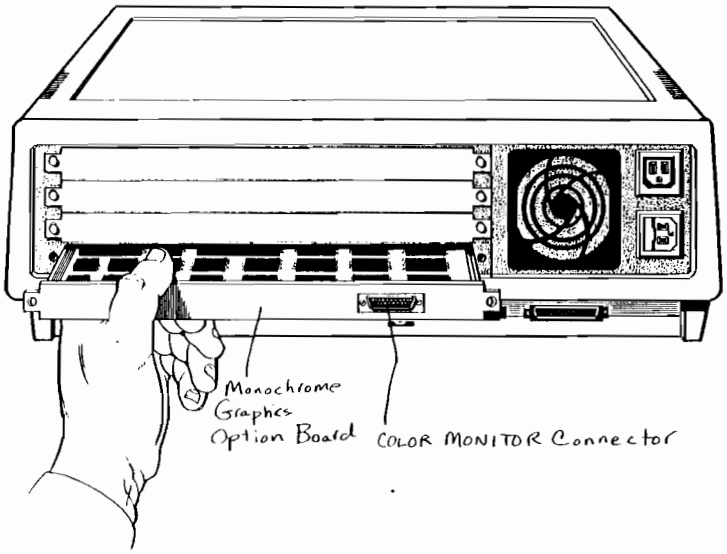


Figure 1.3 External Plug-in Option Cards

2/ Specifications

2.1 Physical Characteristics

Main Unit
- Width 19.0 inches (48.26 cm)
- Height 6.0 inches (15.24 cm)
- Depth 16.0 inches (40.64 cm)
- Weight
  - 26-5103 23.0 pounds (10.4 kgm)
  - 26-5104 26.5 pounds (12.0 kgm)

Monochrome Monitor
- Width 16.25 inches (41.28 cm)
- Height 11.4 inches (29.0 cm)
- Depth 12.2 inches (31.0 cm)
- Weight 15.4 pounds (7.0 kgm)

Keyboard
- Width 16.25 inches (41.28 cm)
- Height 1.2 inches (3.05 cm)
- Depth 7.875 inches (20.0 cm)
- Weight 2.8 pounds (1.3 kgm)

2.2 System Operating Characteristics

Storage Temperature - -40 to +160°F (-40 to 71°C)
Ambient Temperature - 55 to 85°F (12 to 29°C)
Voltage Range (USA) - 95 to 135 Vac
(Europe) - 190 to 270 Vac

Current Drain - USA - AC Main Unit/Convenience Outlet
Model 26-5103 - 3.0 Amperes
Model 26-5104 - 3.5 Amperes

European - AC current Main Unit only
Model 26-5103 - 0.94 Ampere
Model 26-5104 - 1.2 Amperes

Line Frequency - 47 to 63 Hz

2.3 Peripheral Interfaces

RS232C Connector - DB25 socket connector accessible at the rear of the main unit. Pinout connections are shown in Section 5 of this manual.

2.3 Peripheral Interfaces (con't)

Parallel Printer Connector - 34-pin connector for connection of parallel printer or modem for conversion to serial transmission. Pinout connections are shown in Section 5 of this manual.

Monochrome Monitor Connector - 8-pin socket DIN connector accessible at the rear of the Main Unit.

Motherboard - accessible from the rear of the Main Unit allows up to four optional boards to be plugged into main unit. Existing cover strip and Nylatch latches are removed and optional board is inserted and latched into place with Nylatch hardware.

2.4 Optional Features

Internal 128K RAM Board - plugs into existing 128K RAM board to give 256K bytes of internal RAM storage. Requires disassembly of the main unit for installation. See Section 2 on disassembly procedures.

External 256K Board - plugs into slot on Motherboard at rear of main unit. Supplied with 128K, but may have another 128K added for total of 256K bytes of external RAM.

Mouse/Clock Option Board - plugs into slot on Mother-board. Provides real time clock displayed on monitor screen as well as input from external "mouse" option, a hand-positioned transducer which translates "X" and "Y" position into digital encoded signal.

3/ Disassembly/Assembly

Since the Model 2000 is modular in its construction, disassembly/assembly procedures are simplified. The main modules which make up the Model 2000 are the Main Unit, the keyboard, and the display monitor. These three units may be supplemented by various I/O devices such as printers, modems, memory devices or additional monitors. Disassembly of each module will be described in the following paragraphs. Exercise case when handling the modules to prevent damage to internal components or exterior surfaces.

3.1 Main Unit

The Main Unit contains the Power ON-OFF switch and indicator, the disk drives and the system power supply. All cables interconnect this unit with external devices. Most cables are connected to the rear terminal panel of the Main Unit but there are some connections to the front panel of the Main Unit, such as the keyboard connector. Attached to the bottom of the main unit is a metal chassis which houses the main logic PCB assembly. Turn the Main Unit assembly on either the left or right side to gain access to the mounting screws. There are four screws which attach this assembly to the Main Unit housing. When properly positioned, the logic board provides interconnection from this base PCB to the Mother Board which is used for interconnecting optional feature boards. In addition to this 96-pin connector, there are other connectors which tie to the PCB. When the screws are removed from the base cover, swing the rear of the cover away from the main unit. This will allow the connectors which are at the front of the unit to be removed without damaging them.

Disconnect all connections to the main logic PCB (these include the power input, reset, and sound). With these connectors disconnected, the base assembly may be removed completely from the Main Unit assembly. The PCB is attached to the metal base assembly with nine screws. There is an insulating separator to prevent possible shorting of any of the components on the PCB to the metal base assembly.

The Main Unit housing contains the Power Supply, the Disk Drive Assemblies (either two floppy disk drives or 1 floppy and 1 hard disk drive) and the Motherboard for system options. To gain access to the interior of this unit, remove two mounting screws at the lower rear of the Main

Unit. After removing these two screws, slide the top cover forward to release the catches at the front, then lift the top cover off the assembly. The back panel portion of the case housing remains a part of the Main Unit base as well as the power switch/reset and indicator.

3.1.1 Power Supply

The 95W main power supply for the Model 2000 is located at the left side of the Main Unit and is accessible when the cover is removed from the Main Unit as noted previously. The power supply is attached to the base of the Main Unit with 6 screws, 4 of which are screwed into the bottom of the base and 2 of which are attached to the backside of the front bezel If the Main Unit has a Hard Disk assembly installed, it must be detached to provide access to the connectors which connect the power supply to the Main Logic PCB.

1. Remove the connectors attached to the Motherboard, disk drives, and Main Logic PCB.

2. Remove 4 screws which attach the power supply assembly to the base plastic.

3. Remove the two screws which connect the power supply to the front bezel assembly.

4. Lift the power supply from the Main Unit.

5. Remove 3 screws from the RH side of the power supply to allow the upper enclosure to be lifted off the supply.

6. Remove 4 connectors which attach to the power supply PCB.

7. Remove 8 screws which attach the PCB to the lower enclosure weldment.

8. Cable replacement is accomplished by removing the connectors from the enclosure weldment. All connectors are clip-mounting type connectors which allow replacement without special tools. Remove wires attached to the connector and then depress retaining clips from inside the enclosure. Slide connector out of enclosure weldment.

Assemble the power supply in the reverse order of disassembly. Ensure that the power supply is properly operating before reinstalling it in the Main Unit. See Section 7.2 for checkout procedures for the main power supply.

The 38W Hard Disk power supply assembly is attached to the underside of the power supply cover and nests above the main power supply PCB. It is accessible when the cover is removed from the main supply.

1. Remove the cover from the main unit as noted in Paragraph 3.1.

2. Remove the main power supply cover by removing the 4 mounting screws.

3. Remove the mating connectors to the 38W power supply -- there are two connectors. One is for AC input and the other for DC output. There are three DC output connectors on the PCB. The DC output connector may be attached to any one of the three on reassembly.

4. Remove the 38W power supply board from the cover by removing the 4 mounting screws.

Reassembly of the power supply is in the reverse order of disassembly. Ensure that the orientation of the supply is the same as it was prior to disassembly to prevent interference with the main power supply PCB components.

3.1.2 Disk Drives

The floppy disk drives are mounted at the right side of the Main Unit, attached to the base of the main unit with a mounting bracket on either side of the drives. The drive assemblies (including mounting brackets) may be removed from the Main Unit base by removing 4 screws in the base. After these screws and cables connected to the drives are removed, the drive assembly may be removed completely from the Main Unit.

The hard disk assembly is mounted to the left of the floppy disk drive assemblies. If the unit contains a hard disk drive assembly, it is removed from the Main unit by removing the four mounting screws and attached cables.

3.2 Keyboard Assembly

The keyboard assembly is connected by a coiled cable attached to the left side of the front plate of the Main Unit. Disconnect this connector to completely detach the keyboard assembly. Disassemble the keyboard as noted below.

3.2.1 Disassembly

1. After removing the connector from the Main Unit, turn the keyboard assembly upside down on a soft surface to prevent scratching the surface or keys.

2. Remove three screws from the front of the keyboard. Keep separate so that they may be replaced in the front 3 mounting holes.

3. Remove remaining 6 screws from the sides and back of the keyboard assembly.

4. Hold the top and bottom of keyboard assembly together and turn the assembly rightside up.

5. Lift the top cover off the assembly, exposing the keyboard printed circuit board.

6. Disconnect the cable connector at the right rear of the keyboard assembly and remove the keyboard PCB.

7. Lift the keyboard supports from the rear of the keyboard. These are positioned over the support springs in the keyboard base (two on each side).

8. The cable is secured to keyboard base with a strain relief. If necessary, squeeze the strain relief to remove the cable from the base.

9. The cable wire connections must be removed from the connector to replace the cable assembly. Use a small tool to depress spring clip in the connector and pull the wire/clip end from the connector.

10. The four keyboard support springs slide into the base from the outside of the plastic holders. See the exploded view in Section 8 if required.

3.2.2 Assembly

The keyboard is assembled in the reverse order of disassembly. Ensure that the keyboard supports are properly positioned on the support springs prior to installing the top cover. Also ensure that the shorter mounting screws are used in the front positions of the keyboard assembly to prevent damage to the keyboard plastic.

3.3 Display Unit

The Display Unit for the Tandy Model 2000 computer may be either monochrome or color, depending on individual requirements. Servicing either of the two units is covered in the service manual for the particular type monitor used. See the supplemental sections at the end of this Model 2000 service manual for servicing information.

4/ Adjustments

4.1 Power Supply Adjustment

Adjustment of voltage sources required by the Model 2000 is contained in Paragraph 7.2.1.3 Performance Test. These voltages include +5 Vdc, +12 Vdc, and -12 Vdc.

4.2 PLL Adjustment

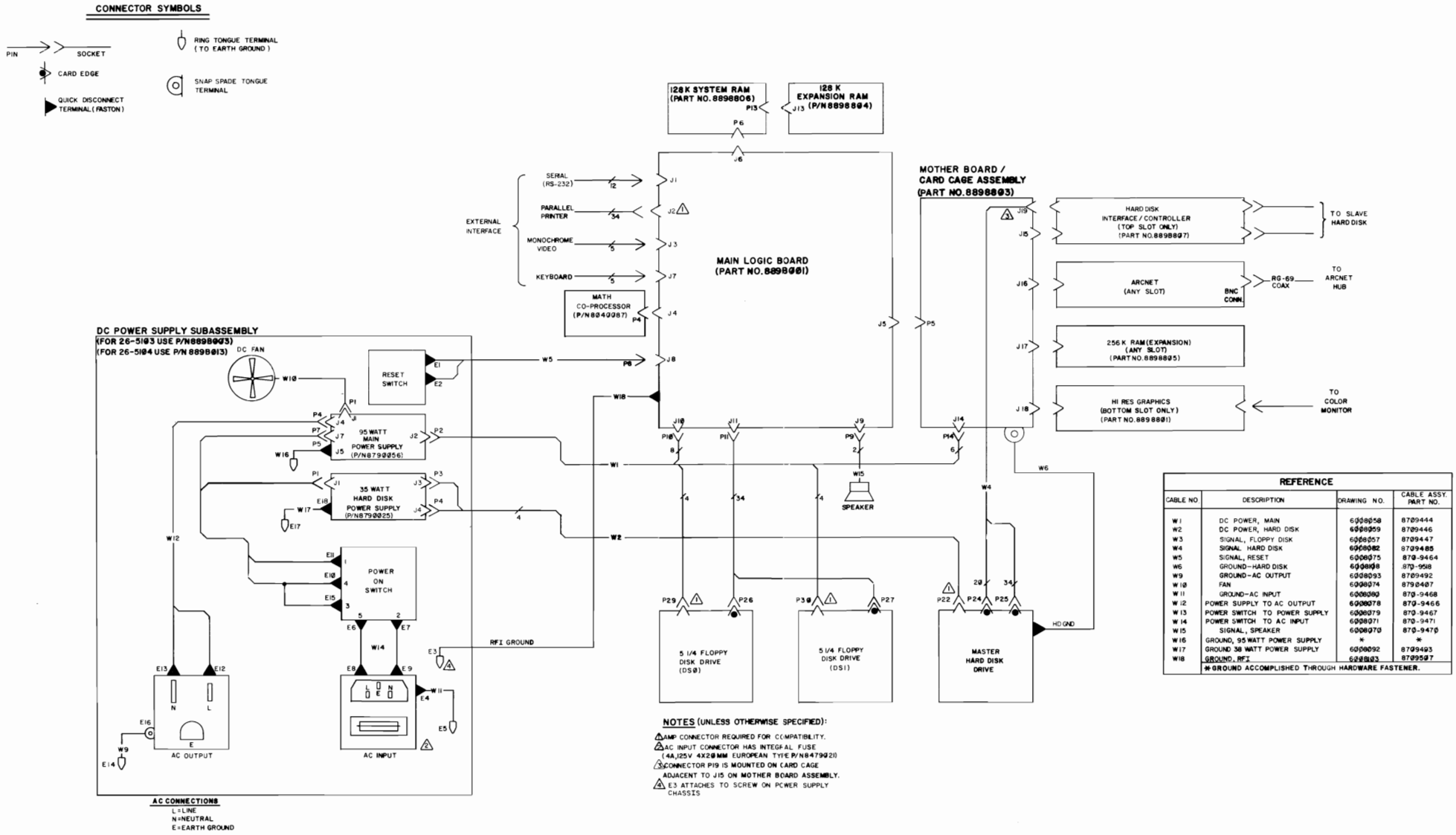
Adjustment of the PLL circuitry is accomplished by the adjustments noted in Paragraph 7.1.7.4.

4.3 Video Adjustment

Adjustments to the video circuits should be made according to the alignment instructions noted in the supplements contained in Section 10 of this manual. Instructions are included for both the Monochrome and Color Monitors.

5/ Cabling Diagrams/Pinout Connections

This section of the manual contains connector diagrams and pin out descriptions of the connectors used in the Model 2000 microcomputer. Figure 7-1 shows an interconnecting wiring diagram and identifies the connectors by symbol number. The following pages then show physical representation of the connector and corresponding pin designations.



REFERENCE

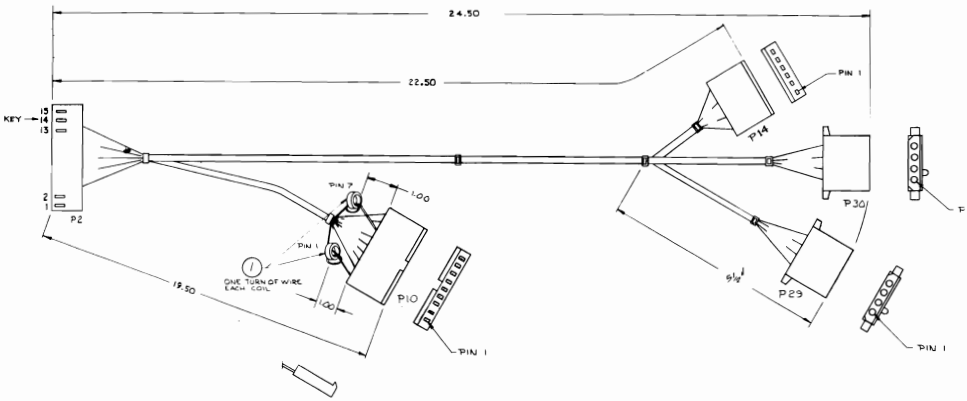
CABLE NO	DESCRIPTION	DRAWING NO.	CABLE ASSY. PART NO.
W1	DC POWER, MAIN	6000058	8709444
W2	DC POWER, HARD DISK	6000059	8709446
W3	SIGNAL, FLOPPY DISK	6000057	8709447
W4	SIGNAL HARD DISK	6000082	8709485
W5	SIGNAL, RESET	6000075	870-9464
W6	GROUND-HARD DISK	6000098	870-958
W9	GROUND-AC OUTPUT	6000093	8709492
W10	FAN	6000074	8708407
W11	GROUND-AC INPUT	6000060	870-9468
W12	POWER SUPPLY TO AC OUTPUT	6000078	870-9466
W13	POWER SWITCH TO POWER SUPPLY	6000079	870-9467
W14	POWER SWITCH TO AC INPUT	6000071	870-9471
W15	SIGNAL, SPEAKER	6000070	870-9470
W16	GROUND, 95 WATT POWER SUPPLY	*	*
W17	GROUND 38 WATT POWER SUPPLY	6000092	8709493
W18	GROUND, RFI	6000103	8709507

* GROUND ACCOMPLISHED THROUGH HARDWARE FASTENER.

NOTES (UNLESS OTHERWISE SPECIFIED):

1. AMP CONNECTOR REQUIRED FOR COMPATIBILITY.
2. AC INPUT CONNECTOR HAS INTEGRAL FUSE (4A,125V 4X20MM EUROPEAN TYPE P/N8479021)
3. CONNECTOR P19 IS MOUNTED ON CARD CAGE ADJACENT TO J15 ON MOTHER BOARD ASSEMBLY.
4. E3 ATTACHES TO SCREW ON POWER SUPPLY CHASSIS

Connector/Cable Interconnection Diagram 8000206A
Model 2000 Computer



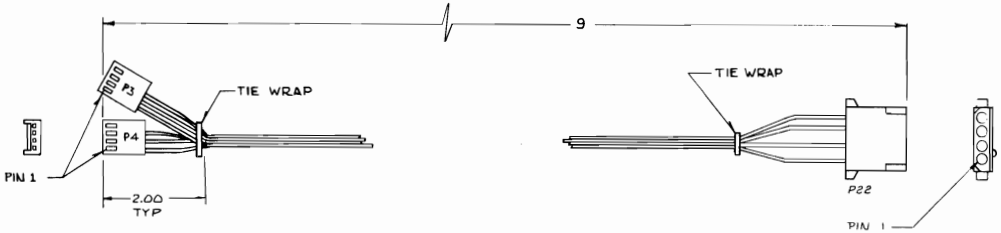
PARTS LIST

DES	QTY	DESCRIPITION	MFG / PART NO.	REMARKS
P2	1	CONN SOCKET 15 POSITION	MOLEX / 09-50-3151	
	15	CONTACT	MOLEX / 08-50-0105	FEMALE PIN
P10	1	CONN SOCKET 9 POSITION	MOLEX / 09-50-3091	
	9	CONTACT	MOLEX / 08-50-0105	
P14	1	CONN SOCKET 4 POSITION	MOLEX / 09-50-3041	
	4	CONTACT	MOLEX / 08-50-0105	
P29 P30	2	CONN SOCKET 4 POSITION	AMP / 1-480424-0	
	8	CONTACT	AMP / 61117-1	
	1	KEY	MOLEX / 19-04-0019	
1	2	COIL, TORID	FAIR-RITE / 5943000201	+12V (-12V ON P10

WIRE LIST

FUNCTION	WIRE AWG	WIRE COLOR	CONNECTO / PIN # P2	P10	P14	P29	P30
+12V	20	ORG	1			1	
	20		9				1
	20		2	1			
+12V	20	ORG	3			2	
GND	18	BLK	3			3	
			4				2
			6				3
			5	5			
			5	6			
			6	8			
			7		3		
GND		BLK	7		5		
+5V		RED	8	3			
			9	4			
			10			4	
			10				4
			11		2		
+5V	18	RED	12		4		
-12V	20	WHT	13	7			
-12V	20		13		6		
KEY	-	-	14				
ACLO	20	GRY	15	2			

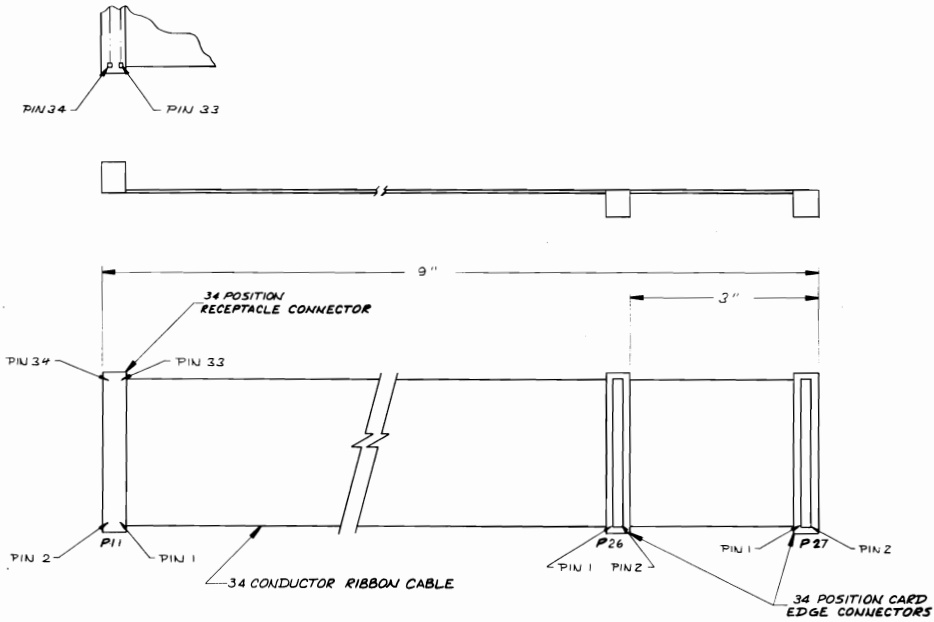
Cable Assembly W1 (6008058)



WIRE LIST								
FUNC-TION	WIRE			CONNECTOR / PIN NO.				
	AWG	COLOR		P22		P3		P4
+12V	20	ORG.		1		3		–
+12V	20	ORG.		1		–		3
GND	20	BLK		2		2		–
GND	20	BLK	...	3		–		2
+5V	20	RED		4		1		–
+5V	20	RED		4		–		1

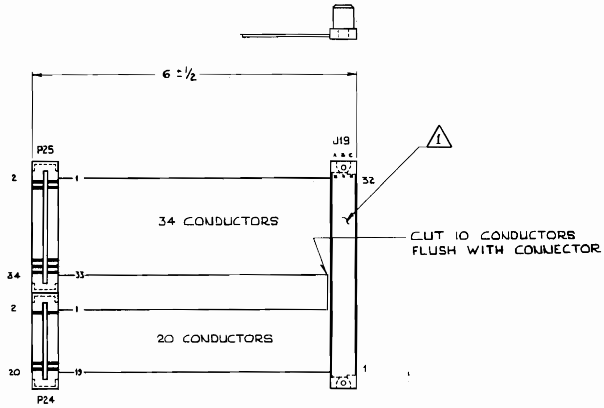
PARTS LIST				
DES	QTY	DESCRIPTION	MFG PART NO.	REMARKS
P22	1	CONN. SOCKET, 4 POSITION	AMP / 1-480424-0	
	4	CONTACT	AMP / 61117-1	
P4/P3	2	CONN. SOCKET, 4 POSITION	MOLEX / 22-01-3047	
	8	CONTACT	MOLEX / 08-50-0113	

Cable Assembly W2 (6008059)



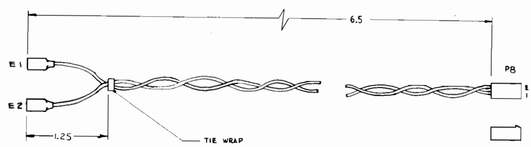
PARTS LIST				
DES	QTY	DESCRIPTION	MFG / PART NO.	REMARKS
P11	1	CONN., 34-PIN RECEPTACLE	MOLEX / 15-29-3343	STRAIN RELIEF 15-25-0069
P26,27	2	CONN., 34-PIN EDGE CARD	3M / 3463-0001	
		"	AMP/ 499930-3	
		CABLE 34-COND., .050 PITCH		

Cable Assembly W3 (6008057)



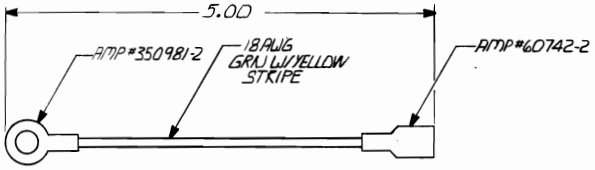
PARTS' LIST					
DESIGNATION	QTY.	DESCRIPTION	MFG.	PART NUMBER	REMARKS
J19	1	96 PIN EURO CONNECTOR	BURNDY	BPS3B96AcRaFoZ1	ROWS A & C LOADED
			BERG	75860-001	
			CANNON	GO6M96P3BLBL-004	
P24	1	20 POSITION EDGE CARD CONNECTOR	AMP	499930-6	
			3M	3461-0001	
P25	1	34 POSITION EDGE CARD CONNECTOR	AMP	499930-3	
			3M	3463-0001	
W2	1	64 COND. FLAT CABLE .050 PITCH CABLE			

Cable Assembly W4 (6008082

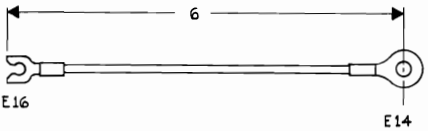


PARTS' LIST					
DESIGNATION	QTY.	DESCRIPTION	MFG.	PART No.	REMARKS
X1	1	E1-P7,2: BLK. 20 AWG GND. E1-P7,1: GRAY 20 AWG RESET			± ½ LENGTH TOLER.
E1, E2	2	QUICK DISCONNECT	AMP	2-350803-2	FULLY INSULATED
P8	1	HOUSING, 2 PIN	MOLEX	09-50-3021	W/LOCKING RAMP
	2	CONTACT	MOLEX	08 50 0105	

Cable Assembly W5 (6008075)

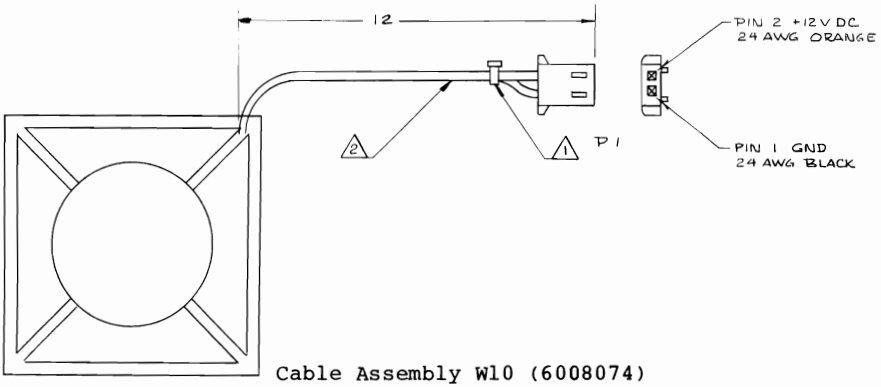


Cable Assembly W6 (6008108

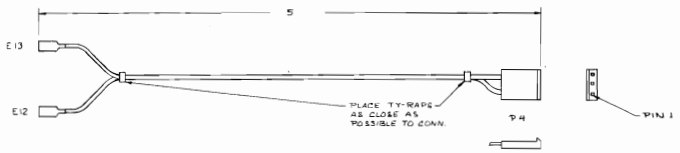


PARTS LIST				
DES.	QTY.	DESCRIPTION	MFG.	P/N
E14	1	RING TERMINAL	AMP	350981-2
E16	1	SNAPSPADE TERM.	AMP	640769-1
	1	WIRE, 18 AWG. GRN. W/YELLOW STRIPE		

Cable Assembly W9 (6008093)



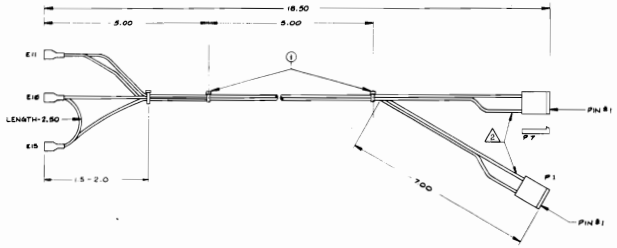
Cable Assembly W10 (6008074)



WIRE LIST								
FUNCTION	WIRE			CONNECTOR/PIN #				
	AWG	COLOR		P4				
LINE	18	BRN		E12	1			
NEUTRAL	18	BLU		E13	3			

PARTS LIST				
DES	QTY	DESCRIPTION	MFG/PART NO.	REMARKS
P4	1	3CKT HOUSING W/LOCK RAMP	MOLEX / 09-50-3031	
	2	CONTACTS	MOLEX / 08-50-0106	
E10, E11, E15	3	QUICK DISCONNECT (.25x.03)	AMP 2-520183-2	FULLY INSULATED

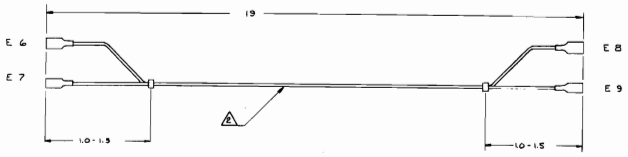
Cable Assembly W12 (6008078



WIRE LIST								
FUNCTION	WIRE			CONNECTOR/PIN #				
	AWG	COLOR		P7	P1	E10	E11	E15
LINE	18	BROWN		1		1		
LINE	18	BROWN			2			1
LINE	18	BROWN		1				1
NEUTRAL	18	BLUE	3				1	
NEUTRAL	18	BLUE		3			1	

PARTS LIST					
DESIGNATION	QTY	DESCRIPTION	MFG	PART NO.	REMARKS
P7, P1	2	3 POS CONN. W/LOCKING RAMP	MOLEX	09-50-3031	
	4	CONTACT	MOLEX	08-50-0105	
E10, E11, E15	3	1/4 x 1/32 QUICK DISCONNECT	AMP	2-520183-2	FULLY INSULATED
①	2	TIE WRAP			

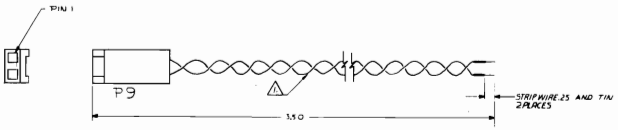
Cable Assembly W13 (6008079)



WIRE LIST					
FUNCTION	WIRE		CONNECTOR / PIN NO.		
	AWG	COLOR			
LINE	18	BRN	E6	E8	
NEUT	18	BLU	E7	E9	

PARTS LIST				
DES	QTY	DESCRIPTION	MFG/PART NO.	REMARKS
E6-E9	4	QUICK DISCONNECT .75×.03	AMP 2-350801-2	FULLY INSULATED
	2	TIE WRAP		

Cable Assembly W14 (6008071)



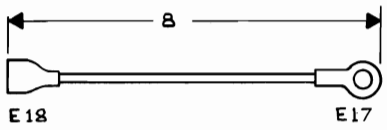
WIRE LIST				
FUNCTION	WIRE		CONNECTOR / PIN NO.	
	AWG	COLOR	P-9	
SPKOUT	24	GRY	1	TO SPEAKER + TERMINAL
GND	24	BLK	2	TO SPEAKER - TERMINAL

PARTS LIST				
DES	QTY	DESCRIPTION	MFG / PART NO.	REMARKS
P9	1	JOHN SOCKET 2 POS	MOLEX / 22-01-3027	
	2	CONTACT	MOLEX / 08-50-0113	

Cable Assembly W15 (6008070

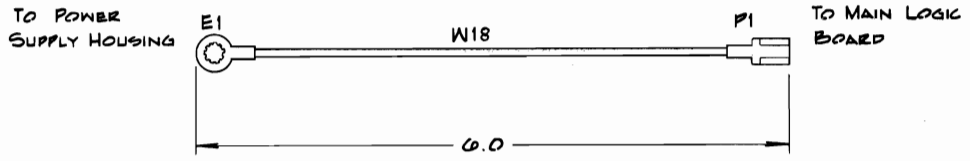
PARTS LIST					
DESIGNATION	QTY	DESCRIPTION	MFG	PART NR	REMARKS
P5	1	¼ X .031 QUICK DISCONECT	AMP	42960-5	INSULATED BARREL
E3	1	RING TERMINAL	AMP	350981-20	INSULATED BARREL
W16	1	18 GA GREEN W/YELLOW STRIP WIRE			± ½ LENGTH TOLER

Cable Assembly W16 (6008080



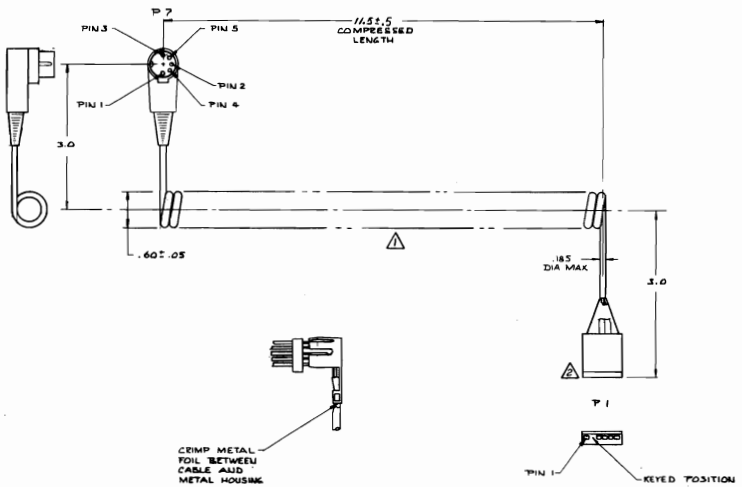
PARTS LIST					
DES.	QTY.	DESCRIPTION	MFG.	P/N	REMARKS
E18	1	1/4 x 1/32 QUICK DISCONECT	AMP	42-400-2	INS. BARREL
E17	1	RING TERMINAL	AMP	350981-2	ING. BARREL
	1	18 GA. GRN. W/YELLOW STRIPE WIRE.			

Cable Assembly W17 (6008092)



PARTS LIST				
DES	QTY	DESCRIPTION	MFG / P.N.	REMARKS
E1	1	RING TERMINAL	AMP / 61793-1	OR EQUIVALENT
P1	1	.250 FASTON RECEPTACLE	AMP / 42400-2	OR EQUIVALENT
W1	1	AWG 12/65 STRANDS OF 30 GA		GREEN W/ YELLOW STRIPE

Cable Assembly W18 (6008103)



WIRE LIST								
FUNCTION	WIRE AWG	WIRE COLOR	CONNECTOR / PIN NO. P7	P1				
KBDDAT	26	BLK	1	1				
KBDCLK	26	GRN	4	3				
KBDRSY	26	YEL	2	4				
+5VDC	26	RED	5	5				
GND	22	BARE	3	6				

PARTS LIST				
DES	QTY	DESCRIPTION	MFG / PART NO	REMARKS
P7	1	CONN 5 PIN DIN RT ANGLE	HOSHIDEN/ [illegible]	
P1	1	6 CKT HOUSING	MOLEX / 22-01-3069	MOLDED KEY IN PIN 2
	5	CONTACT	MOLEX / 08-50-0113	

Keyboard Cable Assembly 6008072

MAIN LOGIC PCB REV. @

J1 - SERIAL INTERFACE (RS-232C)
(25-PIN FEMALE RT. ANGLE DB25)

01	GROUND	02	SERTD*
03	SERRD	04	SERRTS
05	SERCTS	06	SERDSR
07	GROUND	08	SERCD
09	NO CONNECTION	10	NO CONNECTION
11	NO CONNECTION	12	NO CONNECTION
13	NO CONNECTION	14	NO CONNECTION
15	SERTXC	16	NO CONNECTION
17	SERRXC	18	NO CONNECTION
19	NO CONNECTION	20	SERDTR
21	NO CONNECTION	22	SERRI
23	NO CONNECTION	24	NO CONNECTION
25	NO CONNECTION		

J2 - PARALLEL INTERFACE
(34-PIN MALE SHROUDED RT. ANGLE)

01	LPRDATSTB	02	GROUND
03	LPRD0	04	GROUND
05	LPRD1	06	GROUND
07	LPRD2	08	GROUND
09	LPRD3	10	GROUND
11	LPRD4	12	GROUND
13	LPRD5	14	GROUND
15	LPRD6	16	GROUND
17	LPRD7	18	GROUND
19	LPRACK*	20	GROUND
21	LPRBSY	22	GROUND
23	LPRPAEM	24	GROUND
25	LPRSEL*	26	STROBEIN
27	GROUND	28	LPRFLT*
29	LPRIN0	30	LPRIN1
31	GROUND	32	LPRIN2 @
33	GROUND	34	INBUFFULL

MAIN LOGIC PCB REV. PP2

J3 - MONOCHROME VIDEO
(8-PIN DIN RT. ANGLE)

1	NO CONNECTION
2	GROUND
3	INTMON
4	BUSHSYNC
5	BUSVSYNC
6	NO CONNECTION
7	VIDEOMON
8	NO CONNECTION

J4 - MATH CO-PROCESSOR CONNECTOR
(DUAL 31-PIN, 0.100" GRID)

01	+ 5 VOLTS	02	GROUND
03	S0*	04	S1*
05	S2*	06	RESET
07	CLKOUT	08	BHE*
09	AD19	10	AD18
11	AD17	12	AD16
13	AD15	14	AD07
15	AD14	16	AD06
17	AD13	18	AD05
19	AD12	20	AD04
21	AD10	22	AD11
23	AD09	24	AD03
25	AD08	26	AD02
27	AD00	28	AD01
29	RD*	30	RD*
31	WR*	32	WR*
33	ALE	34	ALE
35	ARDY	36	ARDY
37	HOLD	38	HOLD
39	MCS0*	40	MCS0*
41	DT/R*	42	DT/R*
43	NO CONNECTION	44	MCS2*
45	NO CONNECTION	46	MCS3*
47	MCS1*	48	MCS1*
49	GROUND	50	TEST*
51	HLDA	52	HLDA
53	DEN*	54	DEN*
55	SRDY IN	56	DRQ0
57	SRDY OUT	58	DRQ1
59	LATCHED SRDY	60	MCPINT14
61	+5 VOLTS	62	GROUND

NOTE: SIGNALS INTERCEPTED AND REGENERATED BY THE MATH CO-PROCESSOR ARE INDICATED BY BOLD FACE PRINT. A JUMPER TO THE CORRESPONDING SIGNAL IS REQUIRED WHEN THE MATH CO-PROCESSOR IS NOT USED. THESE JUMPERS ARE INCORPORATED ON THE PCB ARTWORK ON THE SOLDER SIDE OF THE BOARD AND MUST BE CUT WHEN INSTALLING THE MATH CO-PROCESSOR.

MAIN LOGIC PCB REV. PP2

J5 - MOTHER BOARD CONNECTOR
(96-PIN MALE EUROCONNECTOR)

01a	NO CONNECTION	01b	NO CONNECTION	01c	NO CONNECTION
02a	GND	02b	AGVID	02c	NO CONNECTION
03a	GND	03b	GND	03c	GND
04a	BUSBLANK	04b	G/A	04c	BUSDOTCLK
05a	BUSCLK	05b	BUSHSYNC	05c	BUSVSYNC
06a	NMI*	06b	GND	06c	AINT
07a	BUSVLT	07b	NO CONNECTION	07c	NO CONNECTION
08a	BUSPCLK	08b	BUSINT03	08c	BUSPCS5*
09a	BUSRFSH*	09b	BUSINT16	09c	BUSPCS4*
10a	BUSIOR*	10b	HDCINT06	10c	BUSPCS3*
11a	BUSHLDA*	11b	RATINT12	11c	BUSLOCK*
12a	BUSBHE*	12b	BUSIOW*	12c	BUSDMARQ1*
13a	BUSMCS1*	13b	BUSMCS0*	13c	BUSDMARQ2*
14a	BUSMR*	14b	BUSMW*	14c	BUSARDY*
15a	BUSRFINH*	15b	BUSL/E*	15c	BUSINT05
16a	BUSMRST*	16b	BUSDEN*	16c	BUSINT07
17a	BUSDT/R*	17b	BUSDMACK3*	17c	BUSINT17
18a	BUSDMACK2*	18b	MEMINT15	18c	BUSDMACK1*
19a	BUSALE	19b	BUSHOLD*	19c	BUSDMARQ3*
20a	GND	20b	GND	20c	GND
21a	BUSD04	21b	BUSD05	21c	BUSD03
22a	BUSD06	22b	BUSD07	22c	BUSD15
23a	BUSD00	23b	BUSD01	23c	BUSD02
24a	BUSD14	24b	BUSD10	24c	BUSD11
25a	BUSD13	25b	BUSD09	25c	BUSD12
26a	BUSD08	26b	BUSA04	26c	BUSA00
27a	BUSA11	27b	BUSA12	27c	BUSA07
28a	BUSA18	28b	BUSA17	28c	BUSA15
29a	BUSA19	29b	BUSA13	29c	BUSA14
30a	BUSA08	30b	BUSA09	30c	BUSA01
31a	BUSA10	31b	BUSA03	31c	BUSA02
32a	BUSA16	32b	BUSA06	32c	BUSA05

MAIN LOGIC PCB REV. PP2

J6 - SYSTEM RAM INTERFACE
(40-PIN MALE HEADER, STRAIGHT)

01	IB01	02	IB00
03	IB02	04	IB04
05	IB03	06	IB05
07	IB07	08	IB06
09	DIPL	10	DOPL
11	WR0*	12	DMEMA06
13	RAS0*	14	DMEMA03
15	DMEMA00	16	DMEMA04
17	DMEMA02	18	DMEMA05
19	DME@A01	20	DMEMA07
21	GND	22	CASU*
23	GND	24	GND
25	+5 VOLTS	26	+5 VOLTS
27	+5 VOLTS	28	RAS1*
29	WR1*	30	CASL*
31	DOPU	32	DIPU
33	IB12	34	IB15
35	IB11	36	IB14
37	IB10	38	IB08
39	IB09	40	IB13

J7 - KEYBOARD INTERFACE
(5-PIN DIN, RT. ANGLE)

01	KBDDAT	02	KBDBSY*
03	GROUND	04	KBDCLK
05	KBDPOWER		

J8 - RESET
(2-PIN MOLEX W/FRICTION LOCK)

01	RES*	02	GROUND@

J9 - SPEAKER
(2-PIN MALE HEADER, POLARIZED)

01	SPKDRV	02	GROUND

J10 - DC POWER
(9-PIN MALE HEADER, POLARIZED)

01	+12 VOLTS
02	ACLO*
03	+5 VOLTS
04	+5 VOLTS
05	GND
06	GND
07	-12 VOLTS
08	.GND
09	NO CONNECTION

J11 - FLOPPY DISK CONTROLLER INTERFACE
(34-PIN MALE HEADER, STRAIGHT)

01	GROUND	02	NO CONNECTION
03	GROUND	04	FLDINUSE*
05	GROUND	06	NO CONNECTION
07	GROUND	08	FLDIDX*
09	GROUND	10	FLDDS0*
11	GROUND	12	FLDDS1*
13	GROUND	14	NO CONNECTION
15	GROUND	16	FLDMTRON*
17	GROUND	18	FLDDIR*
19	GROUND	20	FLDSTP*
21	GROUND	22	FLDWRDAT*
23	GROUND	24	FLDWE*
25	GROUND	26	FLDTRK0*
27	GROUND	28	FLDWRPRT*
29	GROUND	30	FLDRDDAT*
31	GROUND	32	FLDSDSEL*
33	GROUND	34	FLDRDY*

EXPANSION RAM PIN DEFINITIONS
(J13 - EXPANSION RAM BD.)

01	IB01	02	IB00
03	IB02	04	IB04
05	IB03	06	IB05
07	IB07	08	IB06
09	DIPL	10	DOPL
11	NO CONNECTION	12	DMEMA06
13	NO CONNECTION	14	DMEMA03
15	DMEMA00	16	DMEMA04
17	DMEMA02	18	DMEMA05
19	DMEMA01	20	DMEMA07
21	GND	22	CASU*
23	GND	24	GND
25	+5 VOLTS	26	+5 VOLTS
27	+5 VOLTS	28	RAS1*
29	WR1*	30	CASL*
31	DOPU	32	DIPU
33	IB12	34	IB15
35	IB11	36	IB14
37	IB10	38	IB08
39	IB09	40	IB13

OPTION CARD CONNECTOR PIN ASSIGNMENTS
(96-PIN EUROCONNECTOR)

01a	+5 VOLTS	01b	+5 VOLTS	01c	+5 VOLTS
02a	GND	02b	AGVID	02c	+5 VOLTS
03a	GND	03b	GND	03c	GND
04a	BUSBLANK	04b	G/A	04c	BUSDOTCLK
05a	BUSCLK	05b	BUSHSYNC	05c	BUSVSYNC
06a	NMI*	06b	GND	06c	AINT
07a	BUSVLT	07b	+12 VOLTS	07c	-12 VOLTS
08a	BUSPCLK	08b	BUSINT03	08c	BUSPCS5*
09a	BUSRFSH*	09b		09c	BUSPCS4*
10a	BUSIOR*	10b	HDCINT06	10c	BUSPCS3*
11a	BUSHLDA*	11b	RATINT12	11c	BUSLOCK*
12a	BUSBHE*	12b	BUSIOW*	12c	BUSDMARQ1*
13a	BUSMCS1*	13b	BUSMCS0*	13c	BUSDMARQ2*
14a	BUSMR*	14b	BUSMW*	14c	BUSARDY*
15a	BUSRFINH*	15b	BUSL/E*	15c	BUSINT05
16a	BUSMRST*	16b	BUSDEN*	16c	BUSINT07
17a	BUSDT/R*	17b	BUSDMACK3*	17c	BUSINT17
18a	BUSDMACK2*	18b	MEMINT15	18c	BUSDMACK1*
19a	BUSALE	19b	BUSHOLD*	19c	BUSDMARQ3*
20a	GND	20b	GND	20c	GND
21a	BUSD04	21b	BUSD05	21c	BUSD03
22a	BUSD06	22b	BUSD07	22c	BUSD15
23a	BUSD00	23b	BUSD01	23c	BUSD02
24a	BUSD14	24b	BUSD10	24c	BUSD11
25a	BUSD13	25b	BUSD09	25c	BUSD12
26a	BUSD08	26b	BUSA04	26c	BUSA00
27a	BUSA11	27b	BUSA12	27c	BUSA07
28a	BUSA18	28b	BUSA17	28c	BUSA15
29a	BUSA19	29b	BUSA13	29c	BUSA14
30a	BUSA08	30b	BUSA09	30c	BUSA01
31a	BUSA10	31b	BUSA03	31c	BUSA02
32a	BUSA16	32b	BUSA06	32c	BUSA05

MOUSE INTERFACE
(9-PIN "D" TYPE, FEMALE RT. ANGLE)

01	GROUND	02	+5 VOLTS
03	S3*	04	XA
05	XB	06	S2*
07	S1*	08	YA
09	YB		

COLOR MONITOR PIN ASSIGNMENT
(GRAPHICS BD.)

1	GROUND
2	GROUND
3	RED
4	GREEN
5	BLUE
6	INTENSITY
7	NO CONNECTION
8	HSYNC
9	VSYNC

6/ Troubleshooting Procedures

6.1 Power Supply

General diagnostics can be performed on the power supply without removing it from the chassis.

To check the power supply for correct outputs to the logic board and floppy disk, simply remove the top cover of the main unit and disconnect the power connector (P30) from the top floppy disk drive. Check for +12 Vdc (pin 1) and +5 Vdc (pin 4). If these voltages are present, replace the plug and remove the power connector (P10) from the main logic board. Check for +12 Vdc (pin 1), -12 Vdc (pin 7), and +5 Vdc (pins 3 and 4).

CAUTION

DO NOT DISCONNECT BOTH PLUGS at the same time. To function properly, the power supply must have a minimum load.

If any of the voltages do not conform to the specifications contained in Paragraph 7.2.1.1, the power supply and/or harness may be defective. Remove the power supply and troubleshoot using Paragraph 7.2.1.2.

For troubleshooting the power supply assembly, see Section 7.5.4.

6.2 Other Components

If all voltages are present as described in Paragraph 6.1 and the unit is still inoperative, replace first the RAM board and then the CPU to correct the problem. Refer to Paragraph 7.5.2 for a theory of operation on the RAM boards and 7.1.2 for the CPU theory.

7/ Theory of Operation

This section of the manual contains an explanation of the components used in the Model 2000 Microcomputer. It includes a discussion of the Main Logic Board, Power Supply Board(s), and optional boards. The discussions on the Main Logic Board are related to the overall block diagram shown in Figure 7.1. Each subsection contains a simplified block diagram, referenced to a specific page of schematic . The complete schematic of the Main Logic Board is located at the end of Section 7.1. The Power Supply used in the Model 2000 is described in Paragraph 7.2, as well as the supply required for the addition of a Hard Disk Drive Assembly. The Disk Drive Assembly description is contained in Paragraph 7.3. Information concerning the Card Cage Assembly and Motherboard is contained in Paragraph 7.4.

Discussion of optional features, such as 128K Add-On Memory, B/W Graphics Board, Color Graphics Option, Color Monitor, TV/Joystick Board, and Mouse/Clock Board is contained in the manual covering the specific option.

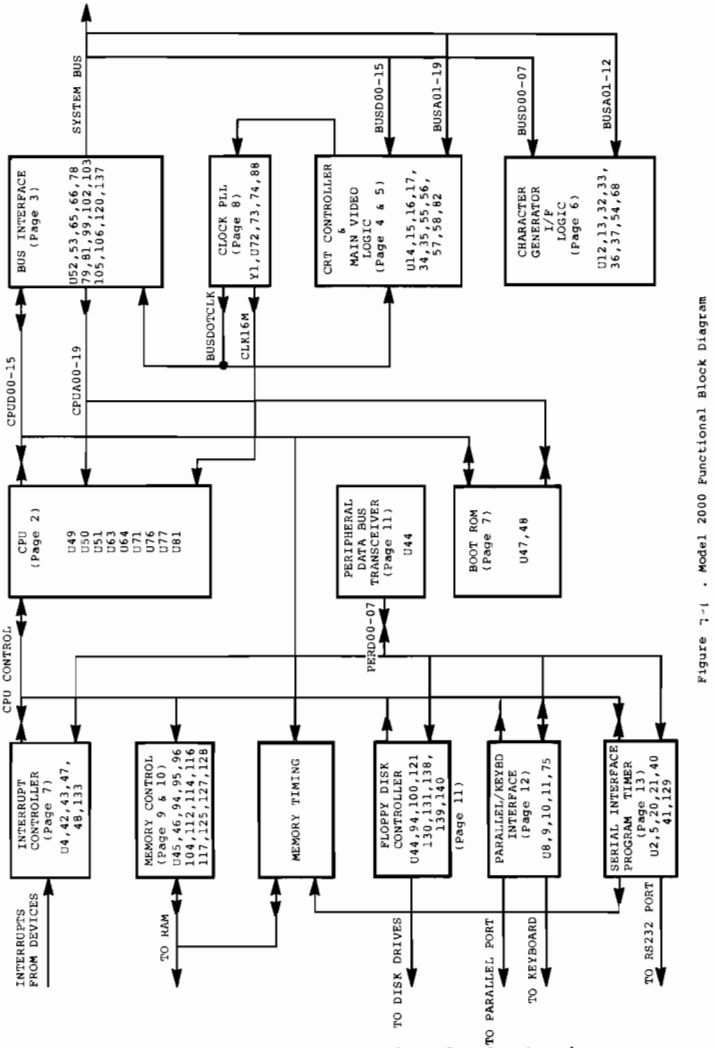


Figure 7.1 . Model 2000 Functional Block Diagram

Figure 7.1 Model 2000 Functional Block Diagram

7.1 Main Logic Board

7.1.1 General

The Main Logic Board is mounted to the underside of the Main Unit and is accessible from the underside. It is mounted to a pan assembly which provides protection and support for the board which is approximately 10" x 16". It contains connectors which allow it to be interconnected to the power supply, disk drives, reset circuitry, and motherboard assembly for optional boards.

See Section 3 for disassembly procedures for the Main Logic Board.

7.1.2 CPU (Sheet 2)

The CPU (Central Processing Unit) revolves around an Intel 80186 microprocessory chip with a clock input of 16 MHz (this yields a 125 nsec machine cycle or "T" state). It is assumed that the reader is familiar with 80186 timing and interfacing. For more information, refer to Intel literature. The CPU section includes logic to buffer and latch all data and address signals. All chip selects (except the boot ROM and character generator) are generated by this section also. A "fail safe" memory timeout circuit prevents the 80186 from waiting forever for a non-existent memory or port address to respond. A programmable DMA (Direct Memory Access) multiplexer maps four bus DMA channels into the two channels resident on the 80186. Logic that directs the bus controller to point the system buses in the right direction is contained here also.

7.1.2.1 CPU Buffering

The Intel 80186 uses a multiplexed address-data bus. The bus is demultiplexed using 74SL373 8-bit transparent latches and 74LS245 octal bi-directional bus drivers. The 74LS373 is enabled for output by CPUHLDA (CPU HoLD Acknowledge, active high) so that it may drive the address bus while the 80186 has the control of the system. The latches are controlled by CPUALE (CPU Address Latch Enable, active high). The falling edge of CPUALE locks the data into the latches for the entire memory cycle. A16 - A19 are not multiplexed with data but require latching as do S0* - S2* (Processor Status bits 0 - 2).

The data buffers are controlled by 80186 generated signals DEN* (Data ENable, active low) and DT/R* (Data Transmit/Receive, high for write cycles, low for read cycles). Within the first T state, DT/R* is set to point the data buffers in the right direction, and DEN* goes low when data appears on the bus.

7.1.2.2 CPU Address Decoding

Address decoding falls into two categories: memory and peripheral. Each is identified by unique read and write status codes on S0* - S2*. The 80186 is software programmable to generate select signals to both spaces. The Model 2000 will always be programmed as shown in Figure 1.

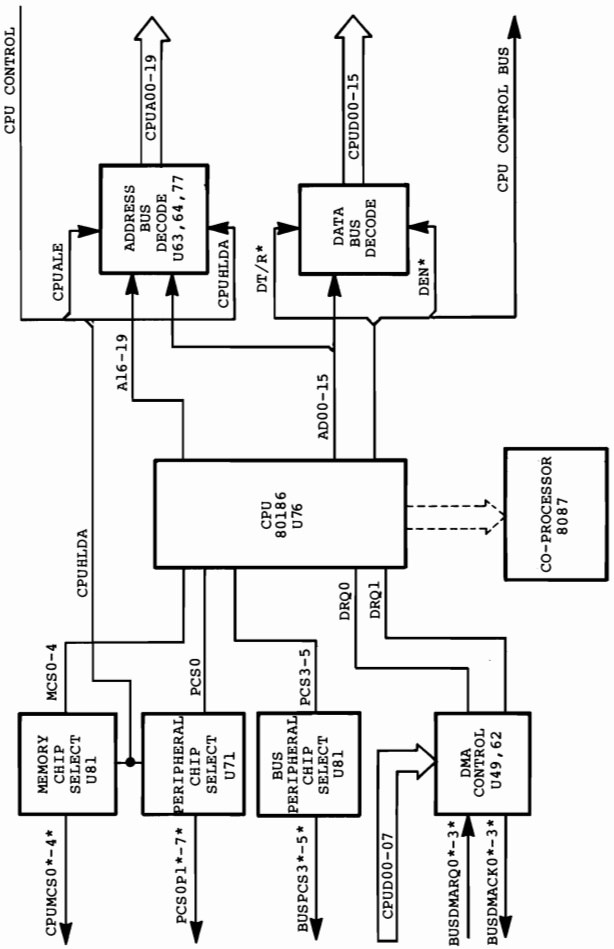


Figure 7-1. CPU Block Diagram

Signal	Memory/Peripheral	Address Range
LCS*	M	Not Used
MCS0*	M	00000H - 1FFFFH
MCS1*	M	20000H - 3FFFFH
MCS2*	M	40000H - 5FFFFH
(not used)		
MCS3*	M	60000H - 7FFFFH
(not used)		
UCS*	M	F8000H -FFFFFH
PCS0*	P	0000H - 007FH
PCS1*	P	0080H - 00FFH
PCS2*	P	0100H - 017FH
PCS3*	P	0180H - 01FFH
PCS4*	P	0200H - 027FH
PCS5*	P	0280H - 02FFH
PCS6*	P	0300H - 037FH
(not used)		

NOTE:

MCSn* address areas are programmed to insert 0 wait states and use 80186 ready inputs. The UCS* address area is programmed to insert 3 wait states and ignore 80186 ready inputs. All PCSn* areas are programmed to insert 2 wait states and ignore 80186 ready inputs.

Figure 7-2. 80186 Programmed Chip Selects

Most internal peripherals are mapped into PCS0* space. This space is split into eight 16-byte active low chip selects by a 74LS138. Both PCS0* and CPUALE condition the 74LS138 to guarantee the subsequent chip selects are valid only when all address bits are stable. The first block of 16 addresses is further broken into four 2-byte blocks (mirrored twice) by 1/2 of a 74LS139. Address assignments are given in Figure 7-4.

Address	Name	Device
0000H - 0001H	PCS0P0A*	Speaker/clocks control
0002H - 0003H	PCS0P0B*	DMA Multiplexer control
0004H - 0005H	FLDTC*	Floppy Disk Term. Count
0006H - 0007H	------	Unused (no connect)
0010H - 001F	PCS0P1	8251A
0020H - 002FH	PCS0P2	Unused (no connect)
0030H - 003FH	PCS0P3	8272A
0040H - 004FH	PCS0P4	8253-5
0050H - 005FH	PCS0P5	8255A-5
0060H - 006FH	PCS0P6	8259A (Controller 0)
0070H - 007FH	PCS0P7	8259A (Controller 1)

Figure 7-3. Peripheral Chip Select 0 Address Assignments

Four DMA acknowledge channels are generated at a base address of 0080H in CPU peripheral address space (See Figure 3). Each one is thrity-two bytes in length. BUSDMACK0* (BUS DMA ACKnowledge 0, active low) is dedicated to the internal floppy disk controller and BUSDMACK3* is dedicated to the internal hard disk. BUSDMACK1* - BUSDMACK3* are routed to the expansion bus connector.

Address	Name	Device
0080H - 009FH	BUSDMACK0*	Internal Floppy Disk Controller
00A0H - 00BFH	BUSDMACK1*	No assignment
00C0H - 00DFH	BUSDMACK2*	No assignment
00E0H - 00FFH	BUSDMACK3*	Hard Disk Controller

Figure 7-4. DMA Acknowledge Address Assignments

An additional level of decoding is required to support the Model 2000 bus structure. The CPUL/E* (CPU Local/External, high for local, low for external) is generated by a 74LS30 8-input NAND gate. The decoded chip selects for CPUMCS0*, CPUMCS1*, PCS0*, BOOT*, and BUSDMACK0* as well as INTAK* and TMOINT01* constitute local addresses. All other addresses are external.

7.1.2.3 Synchronous and Asynchronous Ready

Addressed memory and peripherals handshake with the CPU indicates that a transaction is complete by pulling CPUARDY* (CPU Asynchronous ReaDY, active low wire OR bus) low. Devices not required to handshake in this manner are those which are selected by a memory or peripheral chip select that ignores external ready inputs (See Figure 7.1), with the exceptions being the boot ROM and any interrupt acknowledge cycle (see next paragraph). CPURDY* is then inverted and connected to the ARDY (Asynchronous ReaDY, active high) input on the CPU. Once synchronized inside the CPU, ARDY is ORed with the SRDY (Synchronous ReaDY, active high) so that if either input is a logic "1", the CPU will assume that the addressed device is ready to complete the transaction.

The SRDY input to the CPU is handled differently. When the CPU is reset, UCS* (Upper memory Chip Select, active low from which the boot ROM chip select is generated) will have three wait states inserted automatically and will include external ready inputs. Because no logic provision was included for a UCS* addressed device to respond to the CPUARDY* bus, the CPU will wait indefinitely. A corresponding situation exists for INTAK* (INTerrupt AcKnowledge, active low). To overcome this, UCS* and INTAK* are logically ORed together to generate an active high signal whenever either input is active low. This signal is routed directly to the CPU SRDY input as well as to a 74LS74 which synchronizes it to the CPU clock for use with a co-processor.

7.1.2.4 Memory Timeout

A safeguard circuit is included to prevent the CPU from waiting an excessive amount of time for memory to respond with a ready. Revolving around a 74LS123 timer set for approximately 100 usec, the circuit begins timing a transaction at the leading edge of CPUALE. This forces the timer's Q output to a logical "1". The Q output is gated with CPUDEN* to form TMOINT01 (TiMeOut INTerrupt controller 0, level 1, active high) which goes active only if the timer times out while a transaction is still in progress (signaled by CPUDEN* remaining active low). TMOINT01 is inverted by an open collector gate and output in the correct sense to the CPUARDY* bus and remains low until CPUDEN* goes inactive, indicating that the CPU acknowledges the handshake. Concurrent with this operation, CPUL/E* is forced to the local state (logic "1") so that the bus

drivers are forced inactive. This action prevents a contention on the CPUARDY* bus. If the transaction completes before a timeout, the time will continue until it is restarted by another CPUALE or until it times out. (The system will not see this timeout because CPUDEN* is inactive.)

7.1.2.5 Four Channel DMA Multiplexer

The Model 2000 has provisions for multiplexing four BUSDMARQn* (BUS Direct Memory Access ReQuest n, active low) into the two 80186 resident DMA channels, DRQn (DMA ReQuest n, active high). An 8-bit write only register, located at 0002H in CPU peripheral address space, controls the multiplexing process (bit assignments are given in Figure 4). This register is cleared after a system reset. Each input channel has both an enable bit (to enable the corresponding channel for requests), and a select bit (to select the 80186 channel to which the incoming request is routed). The DMEINT16 (DMA Error INTerrupt controller 1, level 6, active high) signal is used to indicate to software that an invalid programming condition has occured (more than two enabled channels routed to the same 80186 channel). DMEINT16 will remain active until the error condition is removed. DRQn are forces low while INTAK* is active low due to a logic error in early versions of the 80186.

7	6	5	4	3	2	1	0
Chan 3 select	Chan 2 select	Chan 1 select	Chan 0 select	Chan 3 enable	Chan 2 enable	Chan 1 enable	Chan 0 enable

For select bits: 0 for DRQ0
1 for DRQ1

For enable bits: 0 for disable
1 for enable

Figure 7-5. DMA Channel Control Register (Port 0002H)

7.1.3 Bus Interface (Sheet 3)

The Model 2000 uses a unique high performance split-bus architecture. The CPU (Central Processing Unit), base peripherals (floppy disk interface, RS232 interface, and printer/keyboard interface), and the first 256K RAM reside on the local bus while the monochrome and color video systems, as well as any additional memory, are on the external bus. These buses remain independent until a device initiates a transaction that crosses the boundaries.

7.1.3.1 Bus Signal Description

BUSAnn	I/O	20 bit bidirectional address bus (BUSA00 is the least significant bit, BUSA19 is the most significant bit). 220/330 ohm split termination.
BUSDnn	I/O	16 bit bidirectional data bus (BUSD00 is the least significant bit, BUSD19 is the most significant bit). 220/330 ohm split termination.
BUSMCS0*	I/O	BUS Memory Chip Select 0, active low. Selects RAM (on main logic board) in the address reange 00000H - 1FFFFH. 2.2 kohm pullup.
BUSMCS0*	I/O	BUS Memory Chip Select 0, active low. Selects RAM (on main logic board) in the address range 00000H - 1FFFFH. 2.2 kohm pullup.
BUSINT03	I	BUS INTerrupt controller 0, level 3, rising edge sensitive. 2.2 kohm pullup.
BUSINT05	I	BUS INTerrupt controller 0, level 5, rising edge sensitive. 2.2 kohm pullup.
HDCINT06	I	Hard Disk Controller INTerrupt controller 0, level 6, rising edge sensitive. 2.2 kohm pullup.
BUSINT07	I	BUS INTerrupt controller 0, level 7, rising edge sensitive. 2.2 kohm pullup.
RATINT12	I	Mouse Controller INTerrupt controller 1, level 2, rising edge sensitive. 2.2 kohm pullup.

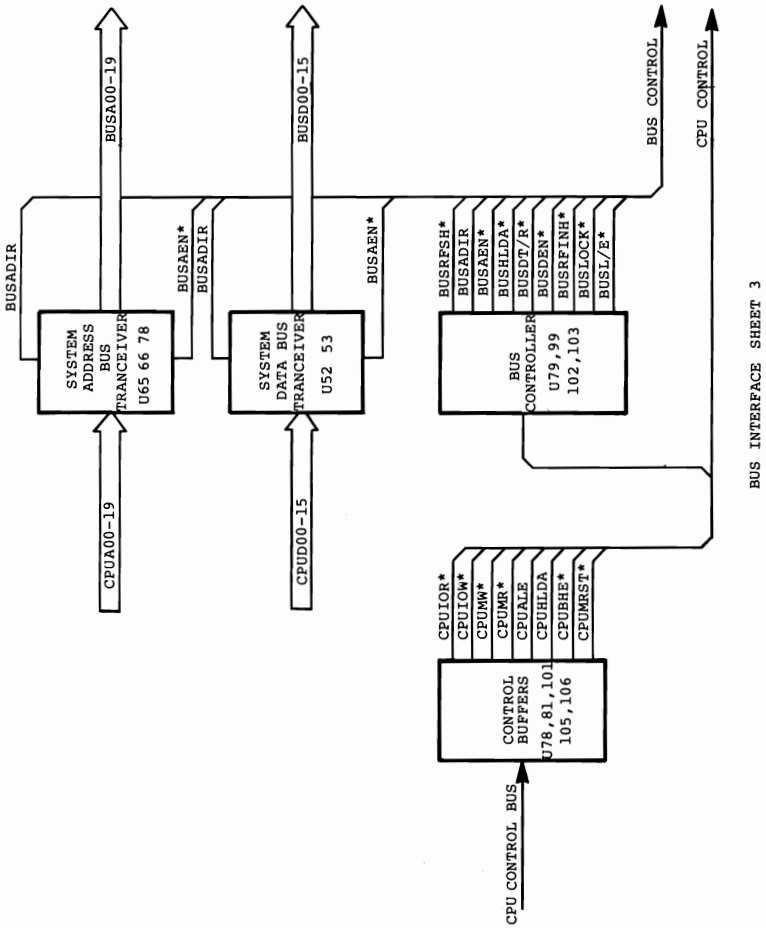


Figure 7-6. Bus Interface Block Diagram

MEMINT15	I	MEMory INTerrupt controller 1, level 5, rising edge sensitive. 2.2 kohm pullup. Open collector bus.
BUSINT17	I	BUS INTerrupt controller 1, level 7, rising edge sensitive. 2.2 kohm pullup.
BUSNMI*	I	BUS Non-Maskable Interrupt, active low. 2.2 kohm pullup. Open collector bus.
BUSDMARQn*	I	BUS Direct Memory Access ReQuest n (1 - 3), active low. 2.2 kohm pullup.
BUSDMACKn*	I	BUS Direct Memory Access ACKnowledge n (1 - 3), active low. 2.2 kohm pullup.
BUSMR*	I/O	BUS Memory Read, active low. 220/330 ohm split termination.
BUSMW*	I/O	BUS Memory Write, active low. 220/330 ohm split termination.
BUSIOR*	I/O	BUS I/O Read, active low. This line may not be driven by an external master. 220/330 ohm split termination.
BUSIOW*	I/O	I/O Memory Write, active low. This line may not be driven by an external master. 220/330 ohm split termination.
BUSMRST*	O	BUS Master ReSeT, active low. Indicates that the CPU is in a reset state. This signal is never tri-stated. 2.2 kohm pullup.
BUSALE	O	BUS Address Latch Enable, active high. When active, bus addresses are unstable. Addresses may be latched at the falling edge of BUSALE. This signal is never tri-stated. 2.2 kohm pullup.
BUSDT/R*	I/O	BUS Data Transmit/Receive, high for transmit, low for receive. This signal indicates the direction that data will flow across the bus. 220/330 ohm split termination.

BUSDEN*	I/O	BUS Data ENable, active low. When active, this signal enables the bus data buffers. 220/330 ohm split termination.
BUSHOLD*	I	BUSH HOLD, active low. This line is pulled low by a bus master when the system bus is required for a transaction. Open collector bus. 2.2 kohm pullup.
BUSHLDA*	O	BUS HoLD Acknowledge, active low. This line is driven low when the bus controller honors the bus request on BUSHOLD*. 2.2 kohm pullup.
BUSLOCK*	I	BUS LOCK, active low. Signals the bus controller that a locked transaction is in progress on the bus and may not be disturbed by another device. 2.2 kohm pullup.
BUSBHE*	I/O	BUS Bus High Enable, active low. This signal enables the high byte (BUSD08 - BUSD15) for access. 220/330 ohm split termination.
BUSL/E*	I	BUS Local/External, high for local, low for external. This signal informs the bus controller if memory on the main logic board (local), or expansion memory is requested for an external master. 2.2 kohm pullup.
BUSARDY*	I/O	BUS Asynchronous ReaDY, active low. When a device is ready to complete a transaction, it will pull this line low. This line is always pointing in the opposite direction from the address lines, so that an external master may communicate with internal memory. Open collector bus. 220/330 ohm split termination.
BUSRFSH*	O	BUS ReFreSH, active low. This signal is the logical OR of CPUMR or CPUMW to indicate to a memory refresh controller that a hidden refresh may occur. THis signal is never tri-stated. 2.2 kohm pullup.

BUSRFINH*	O	BUS ReFresh INHibit, active low. This signal indicates that the current bus master has a fixed memory access time and will not insert wait states so refresh cycles should be inhibited. Never tri-stated. 220/330 ohm split termination.
BUSPCLK	O	BUS Processor CLocK. Buffered CLKOUT from the CPU. May be used for synchronization with the CPU. This signal is never tri-stated. 2.2 kohm pullup.
		THE FOLLOWING SIGNALS ARE CONNECTED TO THE BOTTOM EXPANSION CONNECTOR ONLY
BUSDOTCLK	O	BUS DOT CLocK. The system dot clock either 22.387290 MHz or 27.984113 MHz, depending on the monochrome video mode selected. No termination.
BUSVSYNC	O	BUS Vertical SYNChronization, active low. When active, this signal indicates a vertical synchronization interval. No termination.
BUSHSYNC	O	BUS Horizontal SYNChronization, active low. When active, this signal indicates a horizontal synchronization interval. No termination.
BUSBLANK	O	BUS BLANK, active high. When active, this signal indicates that the video beam is blanked. No termination.
AINT	I/O	Alphanumeric video INTensity. This bit reflects the intensity of the video beam on the monochrome monitor outlet (high for full intensity, low for partial intensity). No termination.
AGVID	I/O	Alphanumeric/Graphic video data. This bit reflects the state of the video on the monochrome monitor outlet (high for on, low for off). No termination.

G/A*	I	Graphic/Alphanumeric. This bit describes the source of the data that appears on the AGVID/AINT buses. If high, video from the high resolution option card will appear on the bus; if low, video from the monochrome sub-system will appear. Pulled up by 2.2 kohm resistor on the main logic board.
BUSVLT	O	BUS Visible Line Time, active high. When active, this signal indicates that the video beam may be visible. No termination.

7.1.3.2 Bus Controller

The bus controller logic is contained in two PAL (Programmable Array Logic) devices. An eight-bit synchronizing latch, clocked by BUSDOTCLK, is used to force changes in state of all signals to occur synchronously. The first PAL (U103, a 16L8) decodes the present bus state and outputs a bus state code on outputs X0* - X4*. It also directly controls BUSADIR and BUSAEN* based on the control inputs. The current bus state also indicates whether the CPU must be halted to honor the bus request, so HOLD is also output by U103.

The second half of the bus controller (U102, also a 16L8) decodes the bus state code and asserts the proper control on the bus. It acknowledges all hold requests and asserts BUSRFINH* when necessary. It also maintains control over BUSDEN* and BUSDT/R*. If the bus is granted to an external master, these lines are tri-stated so that the master may direct the data as necessary.

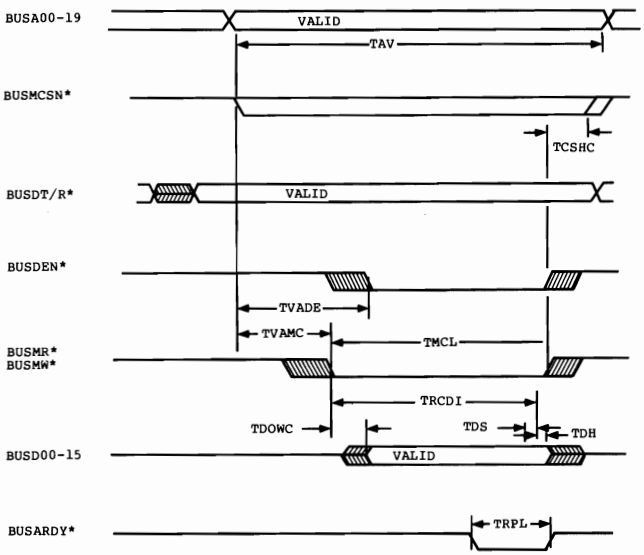
All requests are arbitrated in conjunction with the requester's L/E* signal to determine the extent of action taken. The 80186 has the lowest priority followed by the external bus master. The monochrome video controller has the highest priority. If an external master requests the local bus (as indicated by the associated L/E* being driven high), the CPU is put in a HOLD state and all buses are given to the requester. As long as the CPU does not request the external bus, transactions may occur on that bus without halting the CPU. If an external transaction is in progress and the CPU requests the external bus, it will wait (by virtue of CPUARDY* being high) until the transaction is complete. It is highly recommended that transactions take less than 100 usec because the memory timeout circuit will abort the transaction. All external master devices are expected to drive all tri-stated I/O signals listed in the

previous section or be satisfied with the default condition.

The latched status code signals (LS0* - LS2*) are decoded by a 74F138. Two signals enable the decoder: CPUALE and CPUHLDA. The latched status bits are not guaranteed to be stable until CPUALE falling edge and while the CPU is in a hold state, the status bits indicate a passive state (all 1s) and may be disregarded. The read and write signals (MR*, MRF*, MW*, IOR*, and IOW*) are further conditioned by RD* and WR* as necessary to generate read and write signals with the correct timing.

7.1.3.3 Bus Timing Parameters

Symbol	Parameter	Min	Max	Unit	Comments
t_{VAMC}	Valid address to memory command	20		ns	
t_{AV}	Address valid length	415		ns	Assuming no wait states
t_{VADE}	Valid address to data enable	130	190	ns	
t_{MCL}	Memory command pulse width (read or write)	190		ns	Assuming no wait states
t_{RCDI}	Memory read command to data in	175		ns	Assuming no wait states
t_{DS}	Data setup before data in	20		ns	
t_{DH}	Data hold after data in	10		ns	
t_{DOWC}	Data valid after write command	15	200	ns	
t_{RPL}	BUSARDY* pulse length	125		ns	To generate recognition
t_{CSHC}	Chip select hold after command	35		ns	
t_{BACA}	BUSHLDA* active to address and control driven by requestor	500		ns	
t_{CIBI}	Control inactive before BUSHOLD* inactive	20		ns	



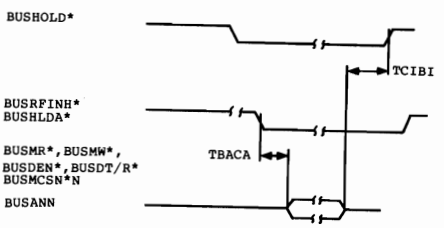


Figure 7-7. Timing Parameter Diagram

7.1.4/ VIDEO SYSTEM (Pages 4 & 5)

The Standard Microsystems Corporation CRT9XXX chip set constitutes the major components of the monochrome video sub-system. Specifically, the CRT9007 Video Processor and Controller (VPAC) is at the center of the system. It generates all video character-related timing such as horizontal sync, vertical sync, composite blank, etc. It also generates memory addresses so that the two CRT9212 Double Row Buffers (DRB) may latch character and attribute data. Attribute data is presented directly to the CRT9021 Video Attribute Generator in the format given below, while the character itself is latched and presented one CCLK* (Character Clock - 357 nsec) later to the RAM-based character generator. The attributes are delayed within the CRT9021 by two CCLK*s so that the character dots from the character generator may "catch up".

The VPAC addresses in system memory (as defined by the address control register) are directed toward even bytes. Ihis allows an entire word of character and attribute data to be loaded into the 9212s in a single, word-wide memory cycle. Confusion may arise when referencing the SMC specification, because that document assumes that the CRT9007 is addressing byte-wide memory. Therefore, each entry in the video row table takes four bytes in system memory, with the two bytes associated with that entry located at even addresses. The fourteen-bit address written to the row table entry should be divided by 2 to account for the VPAC addressing offset. The data at the odd addresses is unused. Also, the addresses of the VPAC registers should be multiplied by 2 to get the correct offset into the system peripheral address space.

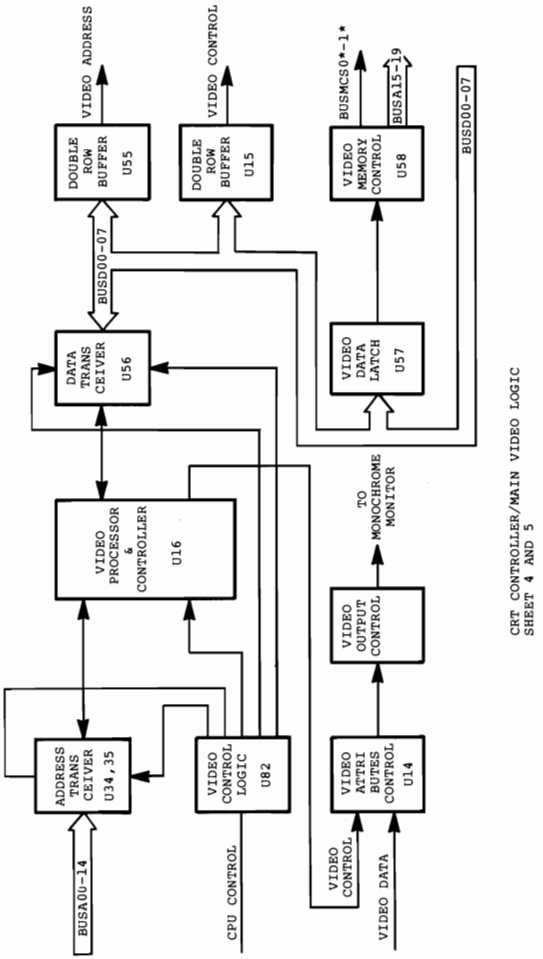


Figure 7-8. CRT Controller/Main Video Logic

7.1.4.1 VIDEO SYSTEM THEORY OF OPERATION

The CPU may access the CRT9007 registers by driving PCS2* active low. A PAL10L8 conditions PCS2* with CPUA00 and CPUDE@* to generate a chip select to the VPAC on even addresses only while data is valid. The PCS2* signal is also conditioned with CPUBHE*, CPUDEN*, and CPUIOW* to generate the ADDLWE* (ADDress Latch Write Enable) signal on odd addresses. Data from CPUD08-CPUD15 is written to the address latch on the rising edge of ADDLWE*, approximately 30 nsec after the rising edge of CPUIOW* (the propagation delay through the PAL10L8). The logic allows writing to both the 9007 and the address control register at the same time.

Data and addresses are buffered through 74F series octal buffers with control signals generated in the PAL10L8. The data buffer, a 74F245, is enabled when either VIDCS* (the VPAC chip select) is active low, or both VIDHOLD and VIDHLDA are active high, indicating a CRT9007 DMA cycle is in progress. When PCS2* is active, the data buffer's direction is controlled by CPUA06. When low, data is transferred from the CPU to the CRT9007; when high, data is transferred from the CRT9007 to the CPU on data lines CPUD00-CPUD07. During a VPAC DMA cycle, the data buffer is enabled with the transfer direction from the data bus to the CRT9007. VA00-VA06 are bidirectional address lines and are buffered through a 74F245 whose enable signal is derived from PCS2* active low or VIDHOLD and VIDHLDA active high. Direction for the 74F245 as well as the 74F244 enable (buffering VA07-VA13) is generated from the HIP (Hold In Progress, active high when VIDHOLD and VIDHLDA are active) signal. Addresses are transferred to the CRT9007 when HIP is low.

All DMA cycle timing is derived from VIDCCLK* (the VIDeo Character CLocK), which in turn is derived from VIDDCLK (the VIDeo Dot CLocK). Bit 6 in the address control register selects how many dot clocks constitute a character clock (hence the number of dots across a character, either 8 or 10).

In the 10 dot-per-character mode, the counter is initialized with a value of 06H. When the counter counts up to a value of 0AH, a "0" is clocked into 1/2 of a 74S74 flip flop on the next rising dot clock edge, forcing the VIDLDSH (VIDeo LoaD/SHift) signal low for use by the CRI9021. The inverted value of the counter's Qc output (delayed by four 74S gate delays to make it coincident with VIDLDSH) is used to generate VIDCCLK*. When a count of 0AH is decoded, a "0" is

clocked into the flip flop, forcing VIDLDSH low. Qc rising edge (one state after VIDLDSH goes low) presets the 74S74, forcing VIDLDSH high. When a count of 0FH is reached, the RC* (Ripple Clock) output of the 74LS669 counter goes low, and forces the counter to reload the initial count value on the next clock. The 8 dot-per-character mode is identical except that the counter is loaded with 08H (VIDCCLK* period becomes two states shorter).

Delay logic (in the form of a 6-shift register) delays two of the attribute signals (BLC and BKC) as well as the composite sync signal. The attribute signals need two CCLK delays because the 9021 adds these delays to all attribute inputs except BLC and BKC. The delay of the composite sync signal was required because the 9007 offsets the "real" sync signals (vertical and horizontal sync) from the composite sync signal by two character times. Both the monochrome graphics adapter and the color video adapter require all timing to line up.

During a video DMA cycle, BUSA15 thru BUSA19, BUSMCS0*, and BUSMCS1* are driven to states defined by the address control register (see below) through a 74LS244 driver. BUSA00 and BUSBHE* are driven low through bidirectional drivers in an 82S153 integrated field logic device to enable 16-bit data transfers to the CRT9007 and the CRT9212s. BUSMR* is also driven through a bidirectional driver in the 82S153. Its timing is derived from VIDCCLK* and DLYCCLK* (VIDCCLK* delayed by about 100 nsec) so that CPUMR* goes active low 115 nsec after VIDCCLK* rising edge and stays low until the next VIDCCLK* rising edge.

Scan line data is output by the CRT9007 in a serial fashion with the LSB output first. A 74LS378 is used to convert the data from serial to parallel for use by the character generator. Each bit is output on CCLK* rising edge on SLD (Scan Line Data) as framed by SLG* (Scan Line Gate, active low). The CRT9021 has an on-chip shift register to perform the same function.

A flexible means for transporting video signals from the monochrome system to the color monitor and from the high resolution graphics option board to the monochrome monitor is provided. Two single-bit data buses, AGVID (Alphanumerics/Graphics VIDeo) and AINT (Alphanumerics INTensity) form the bidirectional data path. VIDOUTSEL (VIDeo OUT SELect) controls the monochrome monitor which will display character video or high resolution graphics video (see Address Control Register, below). Both types of

video are passed through a 74LS159 multiplexer with VIDOUTSEL acting as the select input. The VIDEOUT and INTOUT outputs from the CRT9021 are also routed to a pair of 74LS125 gates which are enabled by the bus signal G/A* (Graphics/Alphanumerics, high for graphics, low for alphanumerics). When no graphics board is present, this signal is pulled up.

7.1.4.2 ADDRESS CONTROL REGISTER

Note: The following register definition describes production level boards (Rev 3).

Bit 7							Bit 0
VIDOUTS	CLKCNT	CLKSPD	A19	A18	A17	A16	A15

The address control register is a write-only register that appears at all odd bytes in the space shared with the CRT9007 (which is located at all even bytes) in the block mapped into the system peripheral space defined by the CPU signal PCS2*.

A15-A19 The value of these bits is output to the address bus during video DMA cycles to select the 32K byte page of display RAM.

CCKCNT This bit selects which count value is loaded into the video clock generator. When this bit is zero, the clock generator is loaded with a "6" (for 10 dot-per-character normal video), and when high, the counter is loaded with an "8" (for 8 dot-per-character color and graphic video).

CLKSPD This bit selects the dot clock frequency. When it is a "0", 22.4 MHz is selected (normally for 8 dots-per-character), and when it is a "1", 28 MHz is selected (normally for 10 dots-per-character). Note that when either the monochrome graphics adapter or the color graphics adapter is installed, this bit should be set to a "0".

VIDEOUTSel This bit selects the source of video information to be output to the monochrome video connector. When this bit is a "1", video from the onboard video system is output to the monochrome video connector. When this bit is a "0", video from a card in the expansion cage is selected.

7.1.4.3 CHARACTER ATTRIBUTES BYTE

Bit 7							Bit 0
REVID	INT	BLINK	MS1	MS0	BLANK	BKC	BLC

This byte is located on the odd byte of each character word in the character block defined above (bits 0-5 of the address control register).

REVID This bit, when set, will display the character in reverse video.

INT This bit, when set, will display the character in full intensity.

BLINK This bit, when set, will cause the character to blink.

MS1-MS0 These bits are programmed to control character attributes as shown below:

MS1	MS0	Character Attribute Selected
0	0	Wide graphics mode*
1	0	Thin graphics mode*
0	1	Normal character mode
1	1	Normal character mode with underline

*For more information on graphics modes, see CRT9021 specification.

BLANK This bit, when set, will blank the character position.

BLC-BKC These bits are programmed to control cursor attributes as shown below:

BKC	BLC	Cursor Appearance
0	0	Blinking underline cursor
1	0	Blinking reverse video block
0	1	Underline cursor
1	1	Reverse video block

7.1.5 Character Generator (Sheet 6)

As mentioned earlier, the character generator is RAM based. Two uPD4016 2K x 8 static NMOS RAM devices form the 4K byte block. Addresses are supplied by two mutually exclusive sources. During video display, the least significant three bits (CGRA01-CGRA03) from the scan line decoder (the fourth bit CGRA00 is used by the 82S153 to select one of the two RAMs), and 8 latched bits from the CRT9212 connected to the lower data bus form the 11-bit character generator address. During a CPU access to the character generator (indicated by CGRCS* Character Generator RAM Chip Select going active low), these outputs are disabled and buffered CPUA01-CPUA12 are sent to the RAM address bits instead. Because any CPU access takes precedence over a fetch from the video system, it is highly recommended that any access to the character generator (read or write) should wait for a horizontal or vertical retrace when the video is blanked. Objectional "hash" will occur otherwise. The 82S153 selects which RAM will output or receive data as determined by BUSMR* and BUSMW* by pulsing the OE* (Output Enable, active low) or WE* (Write Enable, active low) of the correct RAM device. One RAM is dedicated to odd addresses and the other to even addresses.

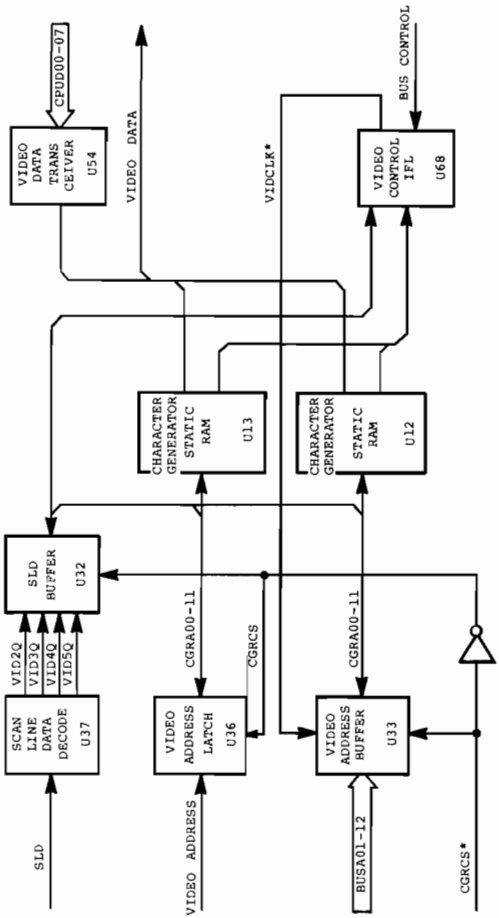


Figure 7-9. Character Generator

7.1.6 Boot ROM/Interrupt Controller (Sheet 7)

7.1.6.1 Boot ROM

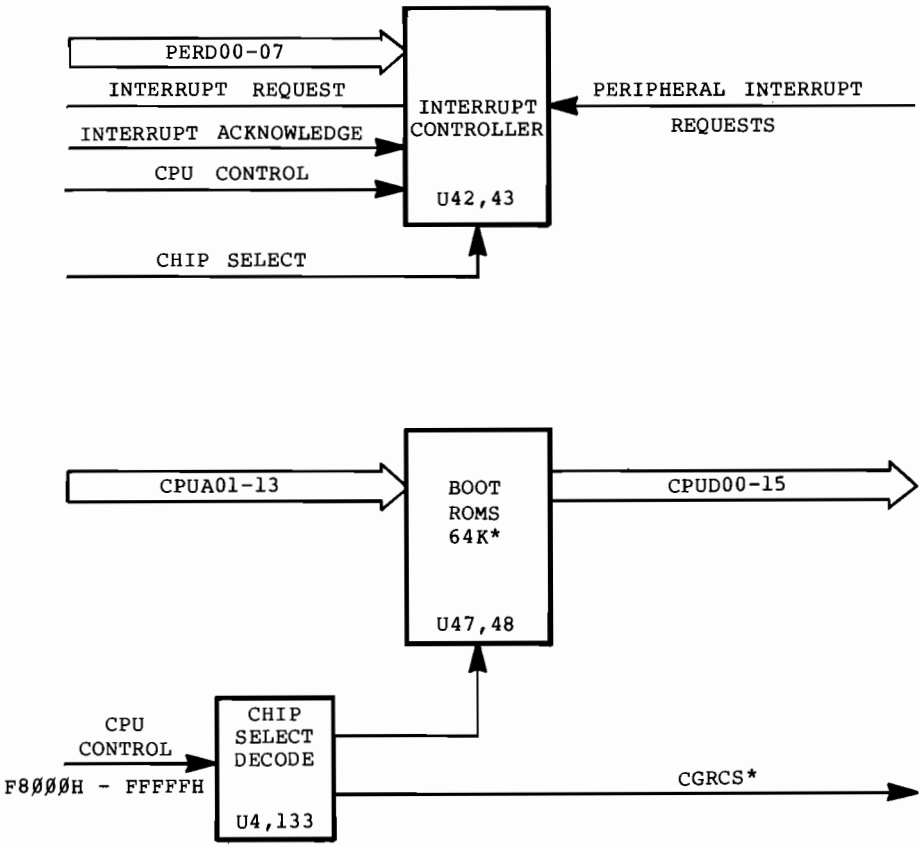
The boot ROM (Read Only Memory) section consists of two ROM devices. Device pinouts must be compatible with the TMS2532 (Texas Instruments). One of the ROMs provides CPUD00 -CPUD07 and the other provides CPUD08 - CPUD15. They respond to all accesses in CPU (Central Processing Unit) memory space from FC000H to FFFFFH. The decode is done in two stages:

1. UCS* (Upper memory Chip Select, active low from F8000H to FFFFFH in CPU memory space) is qualified with CPUALE (CPU Address Latch Enable, active high) to provide a chip select that is valid when all bus address bits are valid.

2. The decoded space is then divided (by CPUA14) into 16K byte spaces so that it may be shared with the character generator.

7.1.6.2 Interrupt Controller

The interrupt controller section consists of two Intel 8259A priority interrupt control devices. They are configured as slave devices to the 80186's internal master interrupt controller (set for cascade mode). Communication with the CPU occurs in one of two forms. The CPU may write commands or check status by accessing the space decoded by PCS0P6* (Peripheral Chip Select 0, Port 6, active low at peripheral addresses 60H to 6FH) for controller 0 or PCS0P7* (Peripheral Chip Select 0, Port 7, active low at peripheral addresses 70H to 7FH) for controller 1. Address assignments for 8259A registers are given in Figure 7-11. All interrupts for the Model 2000 microcomputer are generated on the rising edge of the interrupt input. If the input is high prior to the interrupt, it must go low and remain low for at least 100 nsec to insure recognition. If the interrupt level is unmasked, the interrupt controller will then signal the CPU by activating the INT (INTerrupt output, active high) line. In response, the CPU will pulse either INTA0* or INTA1* (INTerrupt Acknowledge 0 or 1, active low) twice. On the second pulse, the addressed controller is expected to place the vector corresponding to the active interrupt on the preipheral data bus. Interrupt input assignments are given in Figure 7-11. For more information on programming and interfacing with the 8259A, see Intel literature.



INTERRUPT CONTROLLER BOOT ROM
SHEET 7

Figure 7-10. Interrupt Controller/Boot ROM

ADDRESS	READ/WRITE	FUNCTION
0060H	Read	Read OCW2 and OCW3 (Controller 0)
0062H	Read	Read OCW1 (Controller 0)
0060H	Write	Write ICW1 (Controller 0)
0062H	Write	Write ICW2 - ICW4 (Controller 0)
0070H	Read	Read OCW2 and OCW3 (Controller 1)
0072H	Read	Read OCW1 (Controller 1)
0070H	Write	Write ICW1 (Controller 1)
0072H	Write	Write ICW2 - ICW4 (Controller 1)

Figure 7-11. Interrupt Controller Register Assignments

Name	Location		Source	Edge/Level
MEMINT00	8259A	0	Main Logic Board parity error	
TMOINT01	8259A	0	Memory/Peripheral acknowledge timeout	
SERINT02 interrupt	8259A	0	Onboard Serial transmit/receive	
BUSINT03	8259A	0	Reserved for second serial channel (on motherboard) SDLC-4 channel board	
FLDINT04	8259A	0	Onboard floppy disk controller interrupt	
BUSINT05	8259A	0	Reserved for Network Interface (on motherboard)	
HDCINT06	8259A	0	Hard disk controller interrupt (on motherboard)	
BUSINT07	8259A	0	Reserved for second hard disk (on motherboard)	
KBDINT10	8259A	1	Keyboard interrupt	
VIDINT11	8259A	1	CRT 9007 interrupt	
RATINT12	8259A	1	Mouse interrupt (on motherboard)	
LPRINT13	8259A	1	Line printer interrupt	
MCPINT14	8259A	1	Onboard math co-processory interrupt	
MEMINT15	8259A	1	Add-on memory parity error (on motherboard)	
DMEINT16	8259A	1	DMA programming error	
BUSINT17	8259A	1	External HD I/O	

Figure 7-12. Interrupt Controller Input Assignments

7.1.7 Clock/PLL (Sheet 8)

The phase lock loop (PLL) circuit is part of the frequency synthesizer for BUSDOTCLK. The BUSDOTCLK signal must be locked (synchronized) to CLK16M. The frequency of BUSDOTCLK is selectable via CLKSP0 to 28.00 MHz (high res display mode) or 22.40 MHz (normal display mode).

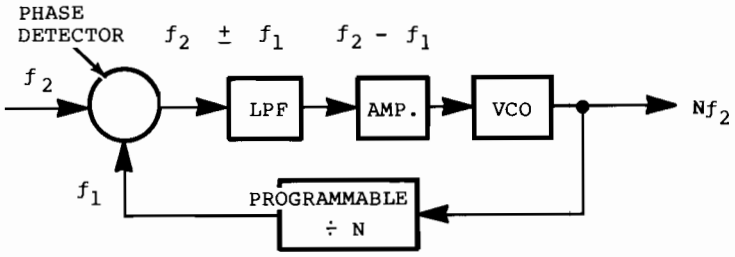


Figure 7-13. Block Diagram

7.1.7.1 General Frequency Synthesis Theory

The block diagram above shows the basic operating principle of the frequency synthesizer. The input frequency is generated by a stable source such as a crystal oscillator. The input frequency f2 is compared at the phase detector whose output consists of f2 ± f1. The low pass filter selects f1 - f2. This signal is amplified and fed to the voltage-controlled oscillator. This drives f1 toward f2 so they lock together, and only a phase difference exists between f1 and f2 which gives sufficient signal to f1 to keep it locked to f2. To vary the output frequency, the value of N is changed in the programmable divider.

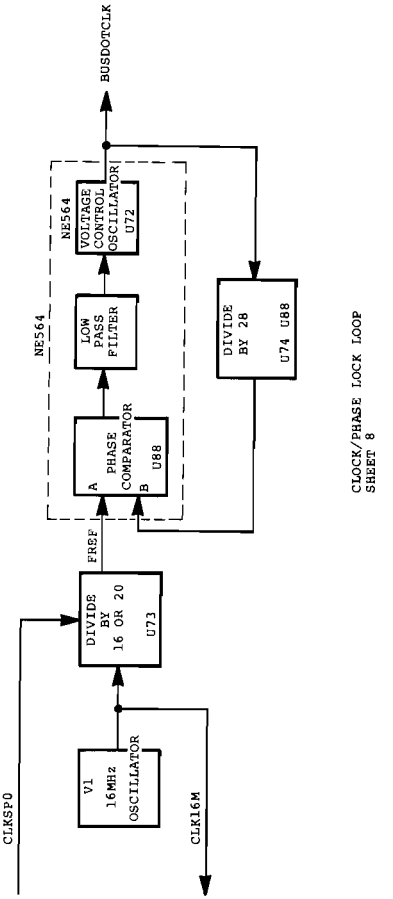


Figure 7-14. Block Diagram Clock/PPL (Sheet 8)

7.1.7.2 Model 2000 PLL Frequency Theory of Operation

The reference frequency f2 is generated by a 16 MHz crystal oscillator (CLK16M) which is divided by either 16 (divide by 8 x 2) or 20 (divide by 10 x 2), depending on the status of CLKSP0. The divide by 2 allows f2 to have a 50% duty cycle into the PLL. This provides reference frequencies of 1.0 MHz and 0.8 MHz respectively for f2. The VCO output frequency fo (BUSDOTCLK) is divided by 28 (divide by 14 x 2) and input to the phase detector (f1). The phase detector will output an error voltage (f2 - f1) to the VCO to lock f1 to f2. Due to the fixed divider in the feedback leg (divide by 28), the VCO output frequency equation becomes:

f0 = 16 MHz x 28/16 or 20

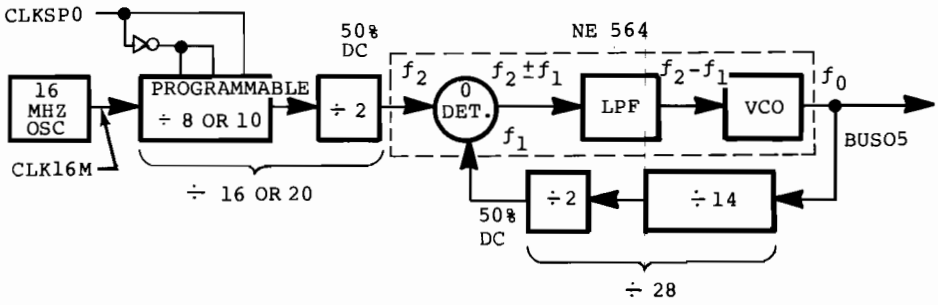


Figure 7-15. Model 2000 PLL Block Diagram

7.1.7.3 Theory of Operation - NE/SE564 Phase Locked Loop

The NE564 is a monolithic phase locked loop with a post detection processor. The use of Schottky clamped transistors and optimized device geometries extends the frequency of operation to greater than 50 MHz. It is used in the Model 2000 as a modulator with a controllable frequency deviation.

The output voltage of the PLL can be written as shown in the following equation:

$$V_0 = \frac{(f_{in} - f_o)}{K_{vco}}$$

where K_{vco} = conversion gain of the VCO

f_{in} = frequency of the input signal

f_o = free running frequency of VCO

The process of recovering FSK signals involves the conversion of the PLL output into logic compatible signals. For high data rates, a considerable amount of carrier will be present at the output of the PLL due to the wideband nature of the loop filter. To avoid the use of complicated filters, a comparator with hysteresis or Schmitt trigger is required. With the conversion gain of the VCO fixed, the output voltage as given by the above equation varies according to the frequency deviation of f_{in} from f_o. Since this differs from system to system, it is necessary that the hysteresis of the Schmitt trigger be capable of being changed so that it can be optimized for a particular system. This is accomplished in the 564 by varying the voltage at pin 15 which results in a change in the hysteresis of the Schmitt trigger.

For FSK signals, an important factor to be considered is the drift in the free-running frequency of the VCO itself. If this changes due to temperature (according to the equation above), it will lead to a change in the dc levels of the PLL output and consequently to errors in the digital output signal. This is especially true for narrow band signals where the deviation in f_{in} itself may be less than the change in f_o due to temperature. This effect can be eliminated if the dc or average value of the signal is retrieved and used as a reference to the comparator. In this manner, variations in the dc levels of the PLL output do not affect FSK output.

Due to its inherent high frequency performance, an emitter-coupled oscillator is used in the VCO. Variation of the phase detector output voltage changes the frequency of the oscillator. The frequency of the oscillator has a negative temperature coefficient due to the positive temperature coefficient of the monolithic resistor. To

compensate for this, a current I_T with negative temperature coefficient is introduced to achieve a low frequency drift with temperature.

The phase comparator consists of a double-balanced modulator with a limiter amplifier to improve AM rejection. Schottky-clamped vertical PNPs are used to obtain TTL level inputs. The loop gain can be varied by changing the current at pin 2 which effectively changes the gain of the differential amplifiers.

The free-running frequency of the VCO is shown by the following equation:

$$f_{op} = \frac{1}{25R_c(Cl + C_s)}$$

R_c = 100 ohms

C_1 = external capacitor in farads

C_s = stray capacitance

The loop filter is explained by the following equation:

$$F(s) = \frac{1}{1 + xRC_3}$$

$R = R_{12} = R_{13} = 1.3$ kohm (INTERNAL)

By adding capacitors to pins 4 and 5, two poles are added to the loop transfer function at $w = \frac{1}{RC_3}$

7.1.7.4 Adjustment Procedure

Remove jumper E4-E5 and set R19 for a voltage of 0.0 V at pin 2 of the NE564. Connect a frequency counter to pin 6 of U89 and adjust C64 for an output frequency of 25.2 MHz. Set R19 for a voltage of 1.30 V at pin 2 of the NE564. Replace the E4-E5 jumper and the PLL should lock at either 28.0 MHz or 22.4 MHz, depending on the status of CLKSP0.

7.1.8 Timing and Control Circuits (Pages 9 & 10)

The onboard 256K memory timing and control circuit is designed to be a high performance, zero wait state system. It generates a 280 nsec memory cycle for 64K DRAMs (Dynamic Random Access Memories) as well as refreshing the array and checking parity. It is able to inhibit the refresh logic whenever necessary, and store the "missed" refreshes.

7.1.8.1 Memory Control Overview

The memory control circuit takes the timing signals generated by the timing circuit and generates buffered (and in some cases terminated) control signals. Data in and out as well as addresses are also buffered in this circuit. Parity is generated and checked here also.

7.1.8.2 Memory Timing Circuit

A memory cycle is started by the leading edge of either a CPUMR* (Central Processing Unit Memory Read) or a CPUMW* (CPU Memory Write), framed by either a CPUMCS0* (CPU Middle Chip Select area 0, active in CPU memory space from 00000H to 1FFFFH) or CPUMCS1* (CPU Middle Chip Select area 1, active in CPU memory space from 20000H to 3FFFFH), all active low. This condition is reflected by SMC (Start Memory Cycle) being active low.

The leading edge of SMC starts the memory timing chain. It also clocks a 74S112 flip-flop which generates the leading edge of T00 (all timing taps are active low and are denoted Tnnn where nnn is the time in nsec). When the T00 leading edge propagates through a ten-tap, 40 nsec per tap delay line to T80, the T00 flip-flop is cleared, generating an 80 nsec pulse width for all taps in the chain.

The leading edge of SMC also clocks another 74LS112 which generates RASTAP*. This allows a cycle to start as soon as possible (without waiting for the delay through the delay line and additional logic). RASTAP* is then routed to the control circuit to output RAS* to the correct RAM bank. RASTAP* is cleared by the leading edge of T160 (or master reset) generating a 160 nsec RAS* low time.

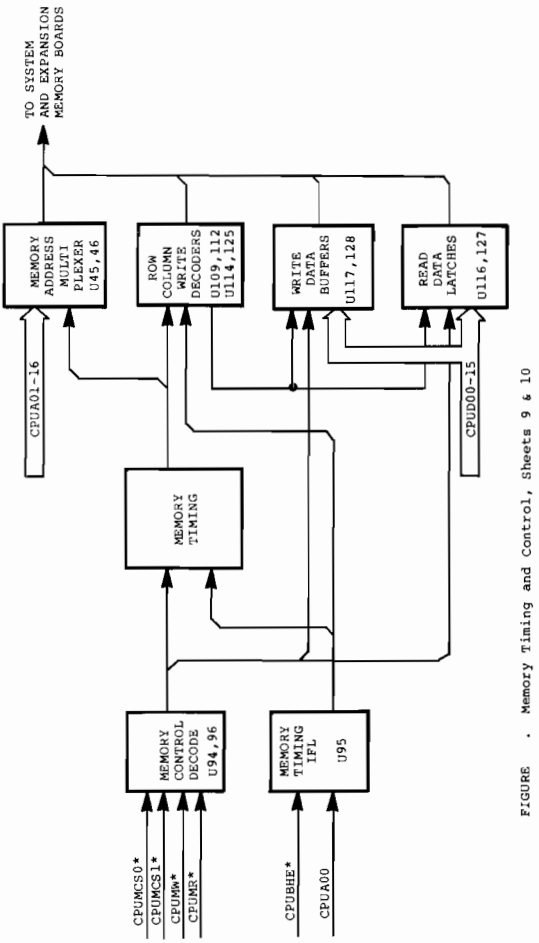


FIGURE . Memory Timing and Control, Sheets 9 & 10

Figure 7-16. Memory Timing and Control

The T40 tap is used to generate both T40AMUX* (T40 Address Multiplex, T40 renamed) and AMUX (Address Multiplex). Both signals are used in memory control address generation. T40AMUX* is delayed by six 74LS04 inverters tied in series (approximately 25 nsec total delay) to generate AMUXDLY* (AMUX Delay, active low). The leading edge of this signal sets a 74S112 to generate CASTAP*. CASTAP* is then routed to the control circuit to output CAS* to the correct RAM bank. The flip-flop is cleared by the leading edge of T200 (or master reset), generating a CAS* pulse of about 135 nsec. The leading edge of T40AMUX* also sets a 74S112 flip-flop to generate WRTAP*. WRTAP* is also routed to memory control to output WR* to the correct RAM bank. It is cleared by T240 (or master reset) to generate a 200 nsec WR* pulse.

An 82S153 IFL (Integrated Field programmable Logic device) is used to generate the correct gating signals for memory control as well as two other miscellaneous signals (ENPARITY, ENable PARITY latch; and BUSRFSH*, the logical OR of CPURD* and CPUWR* to indicate to a bus memory controller slot exists for a hidden refresh). The active conditions for RASEN0*, RASEN1*, CASENL*, and CASENU* are given in Figure

CPUMCS0*	CPUMCS1*	CPUA00	CPUBHE*	RASEN0*	RASEN1*	CASENL*	CASENU*
1	1	X	X	1	1	1	1
X	X	1	1	1	1	1	1
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0
1	0	0	0	1	0	0	0
1	0	0	1	1	0	0	1
1	0	1	0	1	0	1	0

Figure 7-17. RAM ControllerIFL Output Definitions

7.1.8.3 Parity Testing

Parity inputs from memory control, PARU and PARL (PARity Upper and PAR Lower) are ORed together to test for a "1". This signal is then gated with ENPARITY (generated in the IFL, active high which indicates a read from 00000H -3FFFFH). If no parity error exists, a "1" is clocked through a 74LS74 latch during DATALATCH time.

The latch is set to "1" by SMC* to ensure a known state at the start of each memory cycle. The inverted sense output of the latch is buffered through a 74LS38 open-collector buffer to generate MEMINT00 (MEMory INTerrupt controller 0, level 0, active low). The interrupt controller will latch the rising edge to signal the error condition to the CPU.

7.1.8.4 Refresh Control

Refresh cycles are always "tacked" on to the end of a CPU memory access. Memory accesses are stretched by not pulling down on CPUARDY* (CPU Asynchronous ReaDY, active low) until the refresh cycle is finished. If no refresh cycle is required on the current cycle, CPUARDY* is pulled low as soon as the access is decoded to provide a no-wait-state access. The refresh logic is completely disabled during BUSRFINH* (BUS ReFResh INHibit, active low) so that devices accessing memory with fixed access times are not disturbed by the refresh logic.

Refreshes are timed by output 1 of the 8253-5 counter/timer chip (see RS-232 interface document) at a 15 usec interval. Each rising edge of the timer output increments a 74LS193 four-bit binary up/down counter. The count is decoded as non-zero by a 74S260. If the count value is greater than 8, a NMI (Non-Maskable Interrupt) is generated so that the refresh may be serviced before memory is lost.

Before a refresh cycle is run, a memory cycle must be run to arbitrate the refresh request. The refresh cycle is run on the subsequent memory access. At 200 nsec into a non-inhibited memory access (the trailing edge of T120), the state of the refresh count decoder (zero, or non-zero) is clocked into a 74LS74 "D" latch. The latch's output creates both active low and active high senses of RFRQ (ReFresh ReQuest). BUSRFINH* deactivates the latch so that another arbitration cycle must be run after an inhibited cycle. The trailing edge of NC0MC1 (active high for either CPUMCS0* or CPUMCS1*) while RFRQ is active clears the MEMRDY (MEMory ReaDY) latch so that CPUARDY* will not be pulled low at the start of the next cycle.

The next non-inhibited memory cycle is run normally until T120 when the latch that drives ENRASCAS* (ENable RAS CAS address buffers, active low) is set, deactivating the signal. The trailing edge of T120 (at 200 nsec) clocks RFRQ* through another 74LS74 latch to create a non-overlapping ENREFAD* (ENable REFresh ADdress buffers,

active low). With the proper address buffers activated, a pseudo memory (refresh) cycle may be run. At T280 time, the RRFSH* (Run ReFreSH) goes active low and starts a T00 pulse through the timing chain. So that the refresh cycle is a RAS only cycle, CAS is inhibited by deactivating CASENU* and CASENL* in the 82S153 IFL and totally inhibiting WRTAP*.

The DECRCNT* (DECrement Refresh CouNT, active low) signal performs two functions: (1) it decrements the refresh counter, and (2) it increments the refresh address counters (in the memory control circuit, described below). It goes active at the leading edge of T40AMUX during a refresh cycle. Refreshes continue until a zero refresh count is decoded at the trailing edge of T120. This sets RFRQ inactive. At T240, both ENREFAD* and MEMRDY change states, with ENREFAD* going inactive and MEMRDY going active. MEMRDY active signals the CPU that the cycle is complete. The last operation of a refresh cycle is to set ENRASCAS* active by clocking the inactive state of RFRQ at the leading edge of T280.

7.1.8.5 Memory Control

The DRAM array has a common data in/data out bus. Data into the memory array is buffered by 74LS244 octal buffers enabled by MEMWR* (MEMory WRite, active low during a write to the CPU memory space from 00000H to 3FFFFH) to enable memory data onto the CPU data bus. Data to be output to the CPU data bus is buffered by 74F373 octal latches which hold data valid during extended refresh cycles. The latches are enabled for output by MEMRD* (MEMory ReaD, active low during a read from the CPU memory space from 00000H to 3FFFFH). The latches are clocked by DATALATCH (active low) which is the logical combination of a CAS* to either RAM bank.

Parity is both generated and checked by two 74S280s. On a write operation, data is summed eight bits at a time, an additional "1" is added on the I input, and odd parity is written to the appropriate parity RAM for the selected bank(s). On a read, data is again summed and added to the previously stored parity on the I input. The parity sum plus the active high odd sum bit will always be odd. If even parity is decoded, the error is indicated to the memory timing circuit for reporting to the CPU.

Addresses to the memory array may be from one of two mutually exclusive sources. CPU addresses A01-A16 (CPUA00 is used to select the low eight bits of a word address) are multiplexed through a pair of 74F258 multiplexers. During RAS* time, AMUX is low, and A01-A08 are output to the memory array. When RAS* hold time is satisfied, AMUX switches to a high state and selects A09-A16 to be output. Non-refresh cycles are defined by ENRASCAS* active low, which enables the 74F258s for output. During refresh cycles, ENREFAD* is active low, enabling a 74F244 to output the refresh address (stored by both halves of a 74LS393 counter and incremented by DECRCNT*). All addresses are series terminated by 33 ohm resistors to minimize ringing and overshoot.

A set of discrete F family logic gates is used to generate and buffer control signals for the RAM array. The array is divided into both odd and even byte banks and low and high address banks (at the 128K byte boundary as defined by CPUMCS0* and CPUMCS1*). Both the RAS* and WR* signals follow the address boundaries while CAS* follows the byte boundaries. All control signals are series terminated by 33 ohm resistors to minimize ringing and overshoot.

7.1.9 Floppy Disk Controller (Sheet 11)

The Model 2000 Floppy Disk Controller (FDC) circuitry is located on the Main Logic PCB Assembly (P.N. 889B001). It consists of an Intel 8272 FDC, an FDC9216 Floppy Disk Data Separator (FDDS, write precompensation control logic, drive select logic, and other support logic).

The FDC is capable of controlling two thinline Floppy Disk Drives (FDD) using double-side, double-density 5-1/4" flexible diskettes. This provides a formatted memory capacity of more than 635 kbytes per drive for double-density recording.

7.1.9.1 Data Bus Interface

All peripheral control devices on the Main Logic PCB, with the exception of the Video Control circuitry, communicate with the CPU over a bidirectional 8-bit data bus (PERD00-07). This interface is represented on the FDC schematic (sheet 11 of the Main Logic PCB schematic).

The signal CPUDT/R* controls the direction of data flow to and from the peripheral devices through the DIR input on the octal bus transceiver (74LS245). To prevent data bus contention between peripheral devices, the transceiver is enabled by the logical AND of peripheral chip select PCS0* and CPU DMA acknowledge (BUSDMACK0*) which is then ANDed with DMA interrupt acknowledge (INTAK*).

7.1.9.2 FDC Port Specifications

I/O mapping of the peripheral devices places the 8272 at Base I/O port PCS0, port 3, which is the chip select input to the 8272 (PCS0P3*). This signal must be low (positive logic 0) during any read or write operations to the FDC.

There are two registers in the 8272 which are accessible by the CPU -- a Status register and a Data register. The Main Status register is an 8-bit register which contains status information of the FDC that may be accessed at any time. Access to this register is accomplished by a READ instruction to address 0030H. A WRITE instruction to this register is illegal. The Data register is an 8-bit register that stores data, commands, parameters, and FDD status information. It is actually several registers in a stack where only one register is presented to the Peripheral Data Bus at a time. Data is read from or written to this

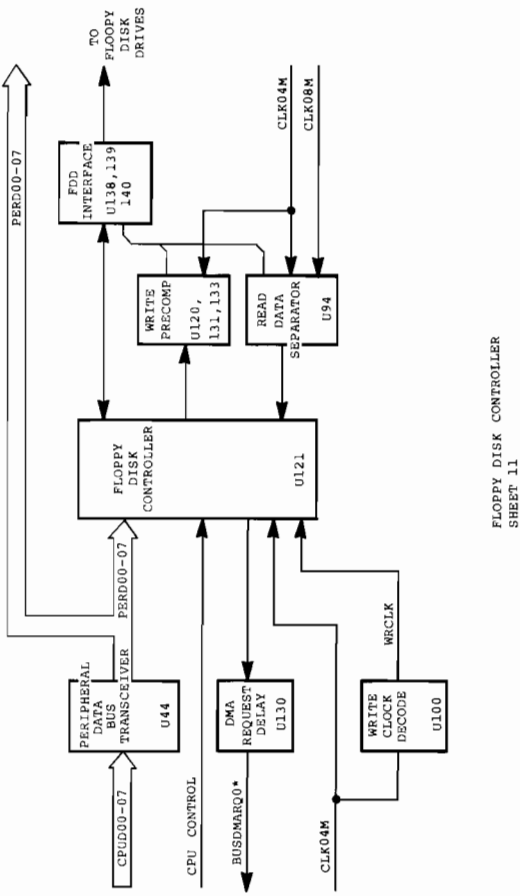


Figure 7-18. Floppy Disk Controller

register by a READ or WRITE instruction to address 0032H to obtain results after executing a command or to program the 8272.

One other operation that is required is a terminal count strobe (TC). This strobe terminates a DMA transfer or the execution phase of an instruction cycle in programming the 8272. The terminate transfer strobe (FLDTC) is executed by a READ or WRITE instruction to address 0004H.

The following table summarizes this information.

FDC PORT SPECIFICATIONS

Register	Instruction	Address	Bits
Status	RD	0030H	D0-D7
	WR	illegal	
Data	RD/WR	0032H	D0-D7
TC	RD/WR	0004H	xx

(xx = don't care)

7.1.9.3 DMA Request and Acknowledge

The 8272 is used in the DMA mode in conjunction with the DMA routing controller IFL (82S153) and the data latch (U49). DMA requests from the FDC (DRQ) are delayed by U130 (74LS74) to satisfy timing constraints before being sent to the DMA routing controller (BUSDMARQ0*). DMA acknowledge is decoded from CPUA05 and CPUA06 through Base I/O port 1 (PCS1*) by U98 (75LS139, sheet 2 of Main Logic schematic) and output to the FDC (BUSDMACK0*).

7.1.9.4 FDD Read Data Sequence

When the FDC receives the first READ command from the CPU, it selects the drive and issues the head load signal (HDL). A high (logic 1) on HDL activates the motor-on (MTRON) signal to the disk drive. Before any data transfer can begin there must be a delay (approximately 250 msec) to allow the drive motor to reach its operating speed. This delay is accomplished by using the internal head load timer in the 8272 as a motor start-up timer. The HDL signal is also used to activate the activity light on the disk drive (FLDINUSE* if used by Tandon drives only).

Once the FDD has been activated and the 8272 has been placed in the Read Data Mode, the head is positioned at the required track on the diskette. The data is then read from the sector(s) and is presented to the Floppy Disk Data Separator (9216) as a composite serial clock/data stream. If the recording format used is single density, the signal will be an FM (Frequency Modulation) encoded signal. If the recording format used is double-density, the signal will be an MFM (Modified Frequency Modulation) encoded signal. Typical FM and MFM encoded signals are shown in Figures 7-19 and 7-20. The FDDS derives a clock signal from the composite signal and regenerates the clock (DW) and the data (SEPD*) signals.

As data is being transferred between the FDC and the CPU, the FDC must be serviced by the CPU every 54 µsec in the FM mode and every 26 µsec in the MFM mode for 5-1/4" disk drives. The FDC will terminate the Read command if the transfer times are longer than those specified.

When the Read Data command has been terminated, the HDL signal will go low, after the specified Head Unload time has elapsed as determined by the 8272 programming. The falling edge of the HDL starts the motor-on timer (74LS123) which maintains the MTRON signal to the disk drives. This allows the drive motor(s) to continue running for a period of approximately 3 seconds so that subsequent drive accesses may be initiated without having to wait for the motor start-up time. This delay decreases the access time between the FDC and the Disk Drives. This is especially valuable when a diskette is copied from one drive to another.

7.1.9.5 FDD Write Data Sequence

The Write Data sequence is similar to the Read Data sequence in that, when the WRITE command is first issued by the CPU, there is a delay for motor start-up time before the head is positioned at the required track. This delay is not required if the motor is already up to speed when the command is issued which may be determined by reading the motor-on status port located on the Two-Sided media input (TS) of the FDC.

When the head is in position, the FDC takes data from the CPU on a byte-by-byte basis from the Peripheral Data Bus (PERD00-07) and outputs it to the FDD. Data is written into each sector until the Write operation has been completed.

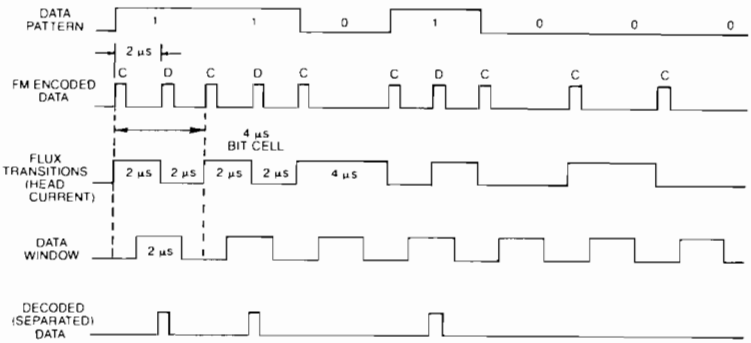


Figure 7-19. FM Encoding Scheme

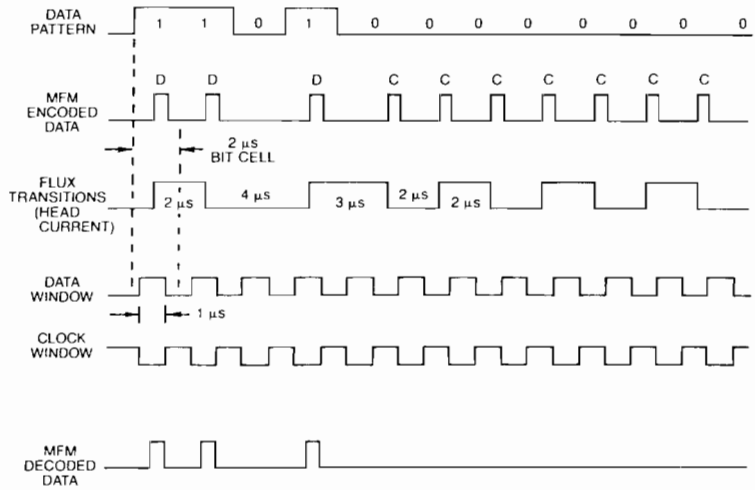


Figure 7-20. MFM Encoding Scheme

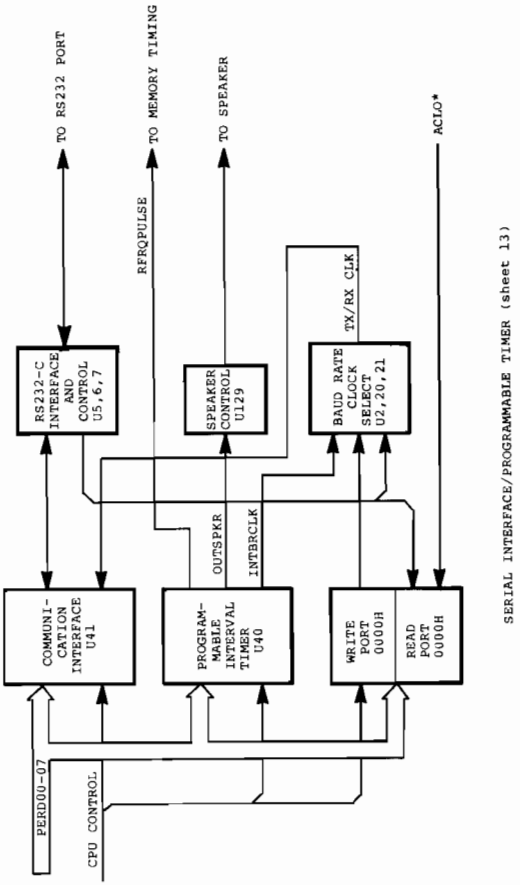


Figure 7-21. Serial Interface/Programmable Timer

Once completed, a Terminal Count (TC) is issued by the CPU and the Write command is terminated. Again, this sequence follows that of the Read Data sequence by starting the motor-on time when HDL goes inactive (low).

Data transfer rates in the Write Data mode must also meet specific requirements to prevent the 8272 from terminating the command. Data transfers from the CPU to the 8272, when using 5-1/4" disk drives, may not exceed 62 µsec for RM mode or 30 µsec for MFM mode.

When writing data on inner tracks, it is necessary to shift the bit positions so that they appear to be at their nominal positions when reading data from those sectors. This is accomplished by using write precompensation which is a means of causing the flux transitions to be written early or late from their nominal positions. The direction of this shift is determined by the FDC according to the data pattern to be written. Precompensation for Model 2000 FDC is controlled by U131 (74LS195) and U133 (74LS02). The clock rate for write precompensation is selectable depending on the requirements of the disk drives used. The default rate is 250 nanoseconds (jumper E7 to E8) or 125 nanoseconds (jumper E6 to E7), if required.

All read and write operations must have the write clock (WRCLK) input to the 8272 enabled. WRCLK for the Model 2000 FDC is a 1 MHz clock with a 250 nanosecond pulse width generated from the 4 MHz clock (CLK04M) through a 4-bit binary counter (74LS161). This allows the Model 2000 to read single or double density diskettes, but to write only to double density diskettes.

7.1.9.6 FDC/FDD Interface

Requirements for the Floppy Disk Controller to Floppy Disk Drive interface are met by using 7416 open-collector drivers and 74LS14 Schmitt-trigger receivers with terminated inputs. The drive select decoder is a 74LS145 lamp/display driver which has the drive capability required for this interface. FDC connector pin assignments are shown in the Table 7-1.

FDC INTERFACE

CONNECTOR PIN ASSIGNMENTS

Pin Number	Signal Name
2	NC
4	FLDINUSE*
6	NC
8	FLDIDX*
10	FLDDS0*
12	FLDDS1*
14	NC
16	FLDMTRON*
18	FLDDIR*
20	FLDSTP*
22	FLDWRDAT*
24	FLDWE*
26	FLDTRK0*
28	FLDWRPRT*
30	FLDRDDAT*
32	FLDSDSEL*
34	FLDRDY*

NOTE: All odd numbered pins are connected to ground.
NC = No connection.

7.1.9.7 Drive Select Decode

Since the 8272 FDC is an "intelligent" controller, it utilizes a polling mode. This mode is automatically entered between commands and step pulses during the SEEK command, where it monitors the READY lines from all "four" disk drives. Since the Model 2000 is configured with only two drives, it is necessary to decode the drive select so that the motor on timer can time out after the last I/O operation to the disk drives.

7.1.9.8 READ/WRITE and SEEK Control

During a READ or WRITE operation, the 8272 sets the RS/SEEK output low (logic 0) which enables two receivers on U135 (74LS241). In this mode, the FDC can read the write protect status (WRPRT) of the diskette installed in the drive(s) and the FDD fault status bit. The input of the receiver of the FDD has been tied low to prevent the FDC from seeing a fault condition that would result from a floating input, since the disk drives used do not use the fault line.

When a SEEK command has been issued by the FDC, the RW/SEEK output is set high (logic 1). This enables two drivers and two receivers on the 74LS241. The drivers control the FDD head direction (DIR) and step pulses (STP) which are output to the disk drive(s). The receivers monitor track 0 status (TRK00) and the two-sided media input (TS) to the 8272 which is used as a motor on status port.

7.1.9.9 FDC Reset Control

The reset input to the 8272 is under software control for programming flexibility. A reset is output to the FDC (FDCRST*) by the 74LS273 (sheet 13 of Main Logic schematic) when a WRITE instruction to address 0000H is executed to set to a low state (logic 0) bit 5 of the data byte written.

7.1.10 Parallel/Keyboard Interface (Sheet 12)

The Printer Interface operation depends on the 8255-A Programmable Peripheral Interface for its operation. The 8255-A is mapped at 050H to 05FH in the peripheral address space. It is located at even bytes only, and register mapping is shown in the table below.

Address	R/W	Operation
0050H	R	Port A - > Data Bus
0052H	R	Port B - > Data Bus
0054H	R	Port C - > Data Bus
0056H	R	Illegal Condition
0050H	W	Port A < - Data Bus
0052H	W	Port B < - Data Bus
0054H	W	Port C < - Data Bus
0056H	W	Control < - Data Bus

Table 7-1. Register Mapping

7.1.10.1 Printer Port

For unidirectional printer port operation, Port A and the upper half of Port C are programmed for Mode 1 operation (for more information on 8255A-5 programming, see Intel Microprocessor and Peripheral Handbook, 1983). Port B and the lower half of Port C are programmed as input and output respectively.

To output a byte of data to the printer, the following sequence should occur. After programming the 8255A-5 for the proper operating modes, a "1" should be written to Port C bit 0 to enable the printer bus buffer for output, and a "00" should be written to Port C bits 1 and 2 to enable printer status for output on the Port B data bus (see Table 7-2 for bit assignments). After determining that the printer is ready to accept data, a byte is written to Port A. Hardware in the 8255A-5 will generate a low-going pulse on Port C bit 7 (Output Buffer Full). This pulse is fed into a 74LS123 one-shot to generate a fixed length pulse of about 1.5 µsec which is the specified length for line printer strobe. The line printer acknowledge is dual-routed to the line printer status port as well as to Port C bit 6

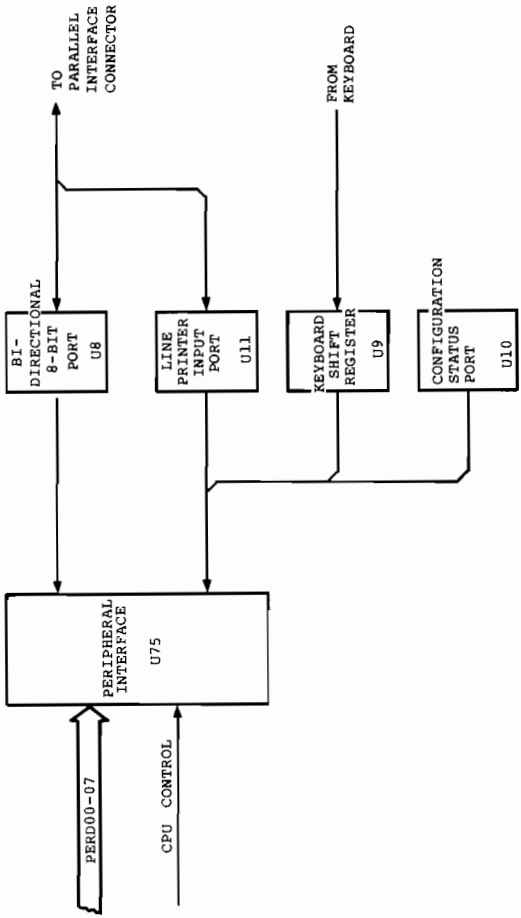


Figure 7-22. Parallel/Keyboard Interface

(ACKnowledge). A rising edge on the ACK* input of the 8255A-5 will cause an interrupt. Any read operation to the 8255A-5 will clear the interrupt.

Bit	Assignment
0	Auxiliary input 0 (currently unused)
1	Auxiliary input 1 (currently unused)
2	Auxiliary input 2 (currently unused)
3	LPRACK*
4	LPRFLT* (Line printer fault)
5	LPRSEL* (Line printer select)
6	LPRPAEM (Line printer paper empty)
7	LPRBSY (Line printer busy)

Table 7-2. Port B Bit Assignments

For bidirectional printer port operaton, the Port A/upper half of Port C combination must be programmed for Mode 2 operation. Port C bit 0 must be programmed for the direction of transfer ("0" for input from port, "1" for output to port). In this mode, Port C bits 4 - 7 take on new meanings. Bit 5 becomes IBFa (Input Buffer Full for Port A, active when the buffer contains unread data), bit 6 becomes ACKa (ACKnowledge output for Port A, same function as for unidirectional mode), and bit 7 becomes OBFa (Output Buffer Full output for Port A, also same as unidirectional mode).

7.1.10.2 Keyboard Interface

The keyboard interface is enabled for parallel input by setting Port C, bits 1 and 2 to "01". This enables the 74LS323 serial-to-parallel converter for output onto the Port B data bus. Data is shifted in serial fashion into the 74LS323 on KBDDAT on each KBDCLK rising edge. Data transfer is terminated with an End-of-Data pulse on KBDDAT (rising edge) while KBDCLK is low. This clocks a 74LS74 low, generating both KBDBSY* on its Q output and KBDINT10 on its Q* output. A read to address 0052H in CPU peripheral space (Port A read) will preset the 74LS74, thus removing KBDBSY* and KBDINT01.

Keyboard power is enabled through bit 0 at address 0000H in CPU peripheral space. This bit is cleared at reset, removing Vcc from the keyboard. When this bit is set to

"1", the logic level is translated to about +12 Vdc by a 751488 level shifter. This in turn drives the gate of an IRFD110 HEXFET, allowing current to pass from drain to source and on to the keyboard Vcc input. Driving -12 Vdc into the gate of the HEXFET (logic "0" translated by the 751488) turns the transistor and the keyboard off.

7.1.10.3 Revision Port

To read the revision port, Port C bits 1 and 2 must be programmed to a "10". This enables the 74LS244 buffer for output onto the Port B data bus. The revision port is encoded with an 8-bit number reflecting the current revision level of the main logic board. Each PCB update will increment this 8-bit value by one.

7.1.11 Serial Interface/Programmable Timer (Page 13)

7.1.11.1 Serial Interface

The serial interface relies on the 8251A Universal Synchronous/Asynchronous Receiver/Transmitter for its operation. The 8251A is used as a peripheral device and is programed by the CPU to operate using virtually any serial data transmission technique presently in use. The USART accepts data characters from the CPU in parallel format and then converts them into a continuous data stream for transmission. Simultaneously, it can receive serial data streams and convert them into parallel data characters for the CPU. The 8251A is clocked at the rate of 2.00 MHz. The 8251A is mapped at 0010H - 001FH in the CPU peripheral address space at even locations only. Register addresses are given in Table 7-3.

Address	Read/Write	Operation
0010H	R	8251A Data -> Data Bus
0010H	W	Data Bus -> 8251A Data
0012H	R	8251A Status -> Data Bus
0012H	W	Data Bus -> 8251A Control

Table 7-3. 8251A Address Assignments

7.1.11.2 Counter/Timer Chip (Page 13)

The 8253-5 is a programmable counter/timer chip which is responsible for generating three timing signals:

1. Periodic speaker output

2. Baud rate clock for the 8251A

3. Refresh timing pulses for the dynamic RAM array

Ihe 8253-5 is mapped at 0040H - 004FH in the CPU peripheral address space at even addresses only. The register assignments are shown in Table 7-4.

Address	Read/Write	Operation
0040H	W	Load Counter 0
0042H	W	Load Counter 1
0044H	W	Load Counter 2
0046H	W	Write Mode Word
0040H	R	Read Counter 0
0042H	R	Read Counter 1
0044H	R	Read Counter 2
0046H	R	No operation

Table 7-4. 8253-5 Address Assignments

The clock for channel 0 is 1.00 MHz, channel 1 and channel 2 are 2.00 MHz. These clocks are derived from the 8.00 MHz clock from the CPU and are divided by 2 four times to generate 4.00 MHz, 2.00 MHz, 1.00 MHz, and 500 KHz by a 74LS161 binary counter.

7.1.11.3 RS-232 Operation (Page 13)

For asynchronous RS-232 operation, the baud rate clock for both transmit and receive is derived from the 8253-5 clock 1 output. To select the internally derived clock (external synchronous operation is outlined below), port 00H bit 1 is set to "1". This routes the 8253-5 clock 1 output to both the transmit and receive clock inputs on the 8251A. Bit assignments for port OOH are shown in Table 7-5.

Bit	Assignment	Function	Active Level
0	KBEN	Keyboard Enable	active high
1	EXTCLK	External baud rate clock	active high
2	SPKRGATE	Enable periodic speaker output	active high
3	SPKRDATA	Direct output to speaker	
4	RFSHEN	Enable refresh and baud rate clocks	active high
5	FDCRESET*	Reset 8272	active low
6	TMRIN0	Enable 80186 timer 0	active high
7	TMRIN1	Enable 80186 timer 1	active high

NOTE: Following a reset, all bits at port 00H are "0".

Table 7-5. Port 00H Bit Assignments

Inputs for the 8251A are taken from J1 after being level-shifted from +12 Vdc levels and inverted by 751489 interface chips. These inputs include: receive data, clear to send, and data set ready (all active low). Outputs from the 8251A which are inverted and level-shifted to +12 Vdc are: transmit data, request to send, and data terminal ready (all active low). Two active high outputs RxRDY and TxRDY) are ORed together to form SERINT02 (SERial INTerrupt controller 0, level 2). RxRDY goes active high when a full character is received. This bit is reset by a read to the data port. In a similar manner, TxEMP goes active high when the transmit buffer is empty while the transmitter is enabled or remains active high while the transmitter is disabled. It is reset by a write to the 8251A data port if the transmitter is enabled.

Synchronous operation is identical to asynchronous operation except that the transmit and receive clocks are supplied by the remote device. Like the data interface, these clocks are level-shifted by the 751489 inverting buffers. To route the external clocks to the 8251A, port 00H bit 1 must be set to "1".

Speaker Port

The speaker port has two modes of operation: periodic and direct. @or periodic mode, SPKRGATE and SPKRDATA must be set to "11" (bits 2 and 3 at port 00H, respectively). This enables output 0 of the 8253-5 to produce a 50% duty cycle square wave of programmed period. For direct mode, SPKRGATE should be set to "0". Then the speaker may be set and reset directly by SPKRDATA. Data from either source is buffered by a 75477 open collector high current buffer before being output to the AC-coupled speaker.

Refresh Clock

The output counter 2 is routed to the dynamic memory control logic and is used to indicate when it is time to do another refresh operation. This counter should be programmed for a pulse on terminal count and a 15 µsec period. Bit 4 at port 00H enables this output as well as clock 1 (the baud rate clock) when it is active high.

VCC AND GND LIST

DEVICE	REF. DESIGNATOR	+5 V	GND	+12 V	-12 V
7416	UI38,140	14	7		
7438	UI9	14	7		
74F00	UII2	14	7		
74F02	UI09	14	7		
74F04	U89,97	14	7		
74F08	UI06,123	14	7		
74F32	U25,101,107,114,125,108	14	7		
74F64	U96	14	7		
74F138	U99	16	8		
74F161	U61,74	16	8		
74F244	U28,35	20	10		
74F245	U34,52,53,56,65,66,80	20	10		
74F258	U45,46	16	8		
74F373	UII6,127	20	10		
74LS00	U4,91	14	7		
74LS02	UI33	14	7		
74LS04	U23,120,122,137,141	14	7		
74LS08	U20,86	14	7		
74LS14	UI39	14	7		
74LS30	UII9	14	7		
74LS32	U2,21,85,136	14	7		
74LS38	U38,87	14	7		
74LS74	U3,84,88**,90,92,118,130	14	7		
74LSI23	U24,132	16	8		
74LSI25A	U22,27,83	14	7		
74LSI38	U67,71	16	8		
74LSI39	U98	16	8		
74LSI61A	U73,100,104	16	8		
74LSI93	U94	16	8		
74LSI95	UI3I	16	8		
74LS241	UI35	20	10		
74LS244	UI0,11,17,33,58,78,81,105, 117,128,32	20	10		
74LS245	U8,44,50,51,54	20	10		
74LS273	U49,70,79	20	10		
74LS323	U9	20	10		
74LS373	U63,64,77	20	10		
74LS374	U36,57	20	10		
74LS393	U29	14	7		
74S00	UI	14	7		
74S74	U69	14	7		
74SII2	UII3,124	16	8		
74SI39	U26	16	8		
74SI57	UI8	16	8		
74S260	U93	14	7		
74S280	UII5,126	14	7		
75477	UI29	8	4		
80186	U76	9,43	26,60		
8251A	U41	26	4		
8253-5	U40	24	12		
8255A-5	U75	26	7		
8259A-2	U42,43	28	14		
8272	UI2I	40	20		
82SI53	U62,68	20	10		
CRT9007	UI6	21	40		
CRT9021	UI4	8	20		
CRT9212	UI5,55	8	23		
FDC9216	UI34	8	4		
MC1488	U5		7	14	1
MC1489	U6,7	14	7		
NE564	U72**		8		
PAL10L8	U82	20	10		
PAL16L8A	U95,102,103*	20	10		
PAL20L8	UI03*	24	12		
PD4016	UI2,13	24	12		
SPARE	U3I	20	10		
SPARE	UI42	20	10		
SPARE	UI43	20	10		
74LSI45	U30	16	8		
74LSI74	U60	16	8		
74LS378	U37	16	8		
74S04	U39	14	7		

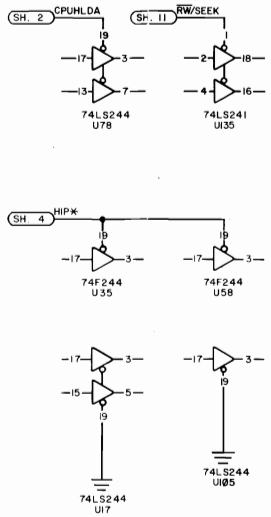
* UI03 MAY USE A PALI6L8A OR PAL20L8 DEPENDING UPON PROGRAM REQUIREMENTS (SEE SHEET 3).

** U72 AND U88 ARE LOCATED IN AN ISOLATED Vcc AND GND AREA (SEE SHEET 7).

SPARE GATES LIST

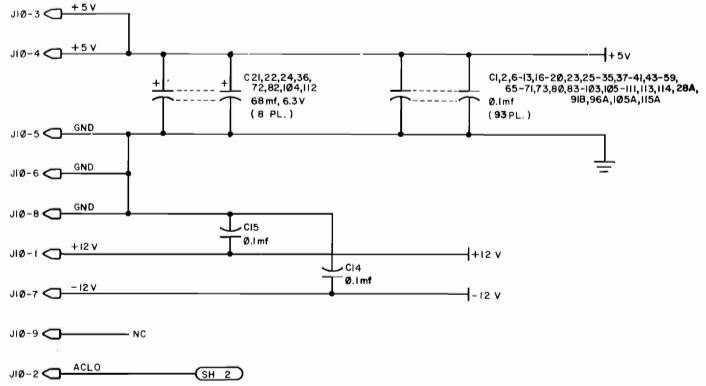
DEVICE	REF. DESG.	GATES NOT USED
7416	UI38	1-6
7438	UI9	1-6
74F00	UI08	1-3,11-13
74F02	UI09	4-6
74F08	UI06	4-6,8-13
74F32	U25	11-13
74F32	UI07	1-3,8-10
74LS00	U4	11-13
74LS00	U91	4-6
74LS02	UI33	8-10
74LS04	UI20	3-6,12,13
74LS04	UI41	3-6,10,11
74LS08	U20	1-3
74LSI4	UI39	1,2
74LS32	U2	1-3
74LS32	U85	4-6,8-10
74LS32	UI36	1-6
74LS38	U38	1-6,8-10
74LS38	U87	8-10
74LS74	UII8	8-13
74LSI23	UI32	1-4,13-15
74LSI25A	U22	11-13
74LSI25A	U83	1-6
74S00	UI	1-3
74SI57	UI8	9-14
74S260	U93	1-3,5,12,13
MC1489	U7	11-13

SPARE BUFFERS



REFERENCE DESIGNATORS

LAST USED	NOT USED
UI43	UIII
YI	
RP5	
CRI	
Q2	
JII	
R59	RI7
CII6	
L I	



DC POWER SCHEMATIC

⚠ CONFIGURATION STATUS PORT: THE MAIN LOGIC BOARD HAS AN 8-BIT PORT THAT INDICATES THE CONFIGURATION STATUS OF THE PRINTED CIRCUIT BOARD WITH RESPECT TO SOFTWARE. THE INPUT STRAPPING TO THIS REGISTER (UI0) MUST BE INCREMENTED BY ONE FOR EACH REVISION OF THE PC BOARD THAT DIRECTLY AFFECTS PROGRAMMING. THE HEX CODE FOR EACH PC BOARD CONFIGURATION CHANGE APPEARS IN THE CONFIGURATION STATUS SCHEDULE AT RIGHT (SEE SHEET 12).

Main Logic Board Schematic 80000203A, Model 2000 Computer
Page 1 of 13

VCC AND GND LIST

DEVICE	REF. DESIGNATOR	+5V	GND	+12V	-12V
7416	U138,140	14	7		
7438	U19	14	7		
74F00	U112	14	7		
74F02	U109	14	7		
74F04	U89,97	14	7		
74F08	U106,123	14	7		
74F32	U25,101,107,114,125,108	14	7		
74F64	U96	14	7		
74F138	U99	16	8		
74F161	U61,74	16	8		
74F244	U28,35	20	10		
74F245	U34,52,53,56,65,66,80	20	10		
74F258	U45,46	16	8		
74F373	U116,127	20	10		
74LS00	U4,91	14	7		
74LS02	U133	14	7		
74LS04	U23,120,122,137,141	14	7		
74LS08	U20,86	14	7		
74LS14	U139	14	7		
74LS30	U119	14	7		
74LS32	U2,21,85,136	14	7		
74LS38	U38,87	14	7		
74LS74	U3,84,88**,90,92,118,130	14	7		
74LS123	U24,132	16	8		
74LS125A	U22,27,83	14	7		
74LS138	U67,71	16	8		
74LS139	U98	16	8		
74LS161A	U73,100,104	16	8		
74LS193	U94	16	8		
74LS195	U131	16	8		
74LS241	U135	20	10		
74LS244	U18,11,17,33,58,78,81,105, 117,128,32	20	10		
74LS245	U8,44,50,51,54	20	10		
74LS273	U49,70,79	20	10		
74LS323	U9	20	10		
74LS373	U63,64,77	20	10		
74LS374	U36,57	20	10		
74LS393	U29	14	7		
74S00	U1	14	7		
74S74	U69	14	7		
74S112	U113,124	16	8		
74S139	U26	16	8		
74S157	U18	16	8		
74S260	U93	14	7		
74S280	U115,126	14	7		
75477	U129	8	4		
80186	U76	9,43	26,60		
8251A	U41	26	4		
8253-5	U40	24	12		
8255A-5	U75	26	7		
8259A-2	U42,43	28	14		
8272	U121	40	20		
82S153	U62,68	20	10		
CRT9007	U16	21	40		
CRT9021	U14	8	20		
CRT9212	U15,55	8	23		
FDC9216	U134	8	4		
MC1488	U5		7	14	1
MC1489	U6,7	14	7		
NE564	U72**		8		
PAL10L8	U82	20	10		
PAL16L8A	U95,102,103*	20	10		
PAL20L8	U103*	24	12		
PD4016	U12,13	24	12		
SPARE	U31	20	10		
SPARE	U142	20	10		
SPARE	U143	20	10		
74LS145	U30	16	8		
74LS174	U60	16	8		
74LS378	U37	16	8		
74S04	U39	14	7		

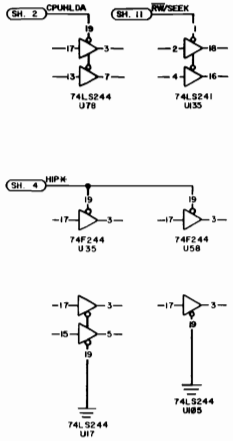
* U103 MAY USE A PAL16L8A OR PAL20L8 DEPENDING UPON PROGRAM REQUIREMENTS (SEE SHEET 3).

** U72 AND U88 ARE LOCATED IN AN ISOLATED Vcc AND GND AREA (SEE SHEET 7).

SPARE GATES LIST

DEVICE	REF. DESG.	GATES NOT USED
7416	U138	1-6
7438	U19	1-6
74F00	U108	1-3,11-13
74F02	U109	4-6
74F08	U106	4-6,8-13
74F32	U25	11-13
74F32	U107	1-3,8-10
74LS00	U4	11-13
74LS00	U91	4-6
74LS02	U133	8-10
74LS04	U120	3-6,12,13
74LS04	U141	3-6,10,11
74LS08	U20	1-3
74LS14	U139	1,2
74LS32	U2	1-3
74LS32	U85	4-6,8-10
74LS32	U136	1-6
74LS38	U38	1-6,8-10
74LS38	U87	8-10
74LS74	U118	8-13
74LS123	U132	1-4,13-15
74LS125A	U22	11-13
74LS125A	U83	1-6
74S00	U1	1-3
74S157	U18	9-14
74S260	U93	1-3,5,12,13
MC1489	U7	11-13

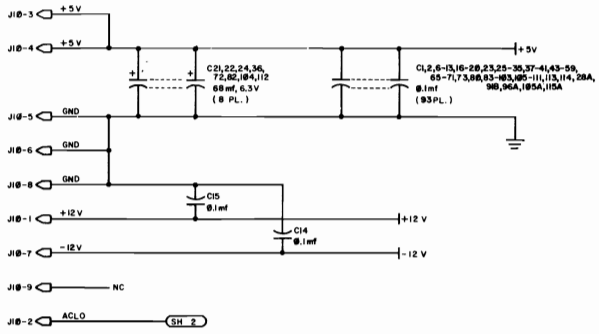
SPARE BUFFERS



REFERENCE DESIGNATORS

LAST USED	NOT USED
U143	U111
Y1	
RP5	
CR1	
Q2	
J11	
R68	R17
C116	
L1	

LTR	REVISION DESCRIPTION		DATE	APPROVED
PP1			5/25/83	
PP2			6/27/83	
REV. A	RELEASED FOR PRODUCTION		11/11/83	
A-1	CORRECT U63,64,77(SH2) & U141(SH9)	IE	2/28/84	
REV. B	REVISED PER TCO NO. 2278 (SH8)	IE	4/7/84	
B-1	REVISED PER TCO NO. 2323 (SH9)	IE	5/1/84	
C	CORRECTED SH5 U67 P1,2,3 & U58 P13 & 15 HAT		10/18/84	



DC POWER SCHEMATIC

Ø3	REV. B	REVISED PER TCO NO. 2278	4/ 7/84
Ø3	REV. A	RELEASED FOR PRODUCTION	11/11/83
Ø3	PP3.5	LIMITED PRODUCTION RELEASE	9/ 1/83
Ø3	PP3	PRE-PROTOTYPE	8/22/83
Ø2	PP2	PRE-PROTOTYPE	6/27/83
Ø1	PP1	PRE-PROTOTYPE	
HEX CODE	PCB REV LTR.	DESCRIPTION	DATE

CONFIGURATION STATUS ⚠

⚠ CONFIGURATION STATUS PORT: THE MAIN LOGIC BOARD HAS AN 8-BIT PORT THAT INDICATES THE CONFIGURATION STATUS OF THE PRINTED CIRCUIT BOARD WITH RESPECT TO SOFTWARE. THE INPUT STRAPPING TO THIS REGISTER (U18) MUST BE INCREMENTED BY ONE FOR EACH REVISION OF THE PC BOARD THAT DIRECTLY AFFECTS PROGRAMMING. THE HEX CODE FOR EACH PC BOARD CONFIGURATION CHANGE APPEARS IN THE CONFIGURATION STATUS SCHEDULE AT RIGHT (SEE SHEET 12).

REF: DRILL PLAN 17Q0245 REV. B

FOR PRODUCTION

DRAFT	DATE 7/83	TITLE: SCHEMATIC- MAIN LOGIC BOARD PROJECT J-507
CHECK	DATE 11/11/83	
DESIGN	DATE	
APPD.	DATE 11/11/83	
APPD.	DATE 11-11-83	

tandy

DWG NO 8000203 SIZE D

SCALE N/A SHEET 1 OF 15

VCC AND GND LIST

DEVICE	REF. DESIGNATOR	+5 V	GND	+12 V	-12 V
7416	U138,140	14	7		
7438	U19	14	7		
74F00	U112	14	7		
74F02	U109	14	7		
74F04	U89,97	14	7		
74F08	U106,123	14	7		
74F32	U25,101,107,114,125,108	14	7		
74F64	U96	14	7		
74F138	U99	16	8		
74F161	U61,74	16	8		
74F244	U26,35	20	10		
74F245	U34,52,53,56,65,66,80	20	10		
74F258	U45,46	16	8		
74F373	U116,127	20	10		
74LS00	U4,91	14	7		
74LS02	U133	14	7		
74LS04	U23,120,122,137,141	14	7		
74LS08	U20,86	14	7		
74LS14	U139	14	7		
74LS30	U119	14	7		
74LS32	U2,21,85,136	14	7		
74LS38	U38,87	14	7		
74LS74	U3,84,88**,90,92,118,130	14	7		
74LS123	U24,132	16	8		
74LS125A	U22,27,83	14	7		
74LS138	U67,71	16	8		
74LS139	U98	16	8		
74LS161A	U73,100,104	16	8		
74LS193	U94	16	8		
74LS195	U131	16	8		
74LS241	U135	20	10		
74LS244	U18,11,17,33,58,78,81,85, 117,128,32	20	10		
74LS245	U8,44,50,51,54	20	10		
74LS273	U49,70,79	20	10		
74LS323	U9	20	10		
74LS373	U63,64,77	20	10		
74LS374	U36,57	20	10		
74LS393	U29	14	7		
74S00	U1	14	7		
74S74	U69	14	7		
74S112	U113,124	16	8		
74S139	U26	16	8		
74S157	U18	16	8		
74S260	U93	14	7		
74S280	U115,126	14	7		
75477	U129	8	4		
80186	U76	9,43	26,60		
8251A	U41	26	4		
8253-5	U40	24	12		
8255A-5	U75	26	7		
8259A-2	U42,43	28	14		
8272	U121	40	20		
82S153	U62,68	20	10		
CRT9007	U16	21	40		
CRT9021	U14	8	20		
CRT9212	U15,55	8	23		
FDC9216	U134	8	4		
MC1488	U5		7	14	1
MC1489	U6,7	14	7		
NE564	U72**		8		
PAL10L8	U82	20	10		
PAL16L8A	U95,102,103*	20	10		
PAL20L8	U103*	24	12		
PD4016	U12,13	24	12		
SPARE	U31	20	10		
SPARE	U142	20	10		
SPARE	U143	20	10		
74LS145	U58	16	8		
74LS174	U60	16	8		
74LS378	U37	16	8		
74S04	U39	14	7		

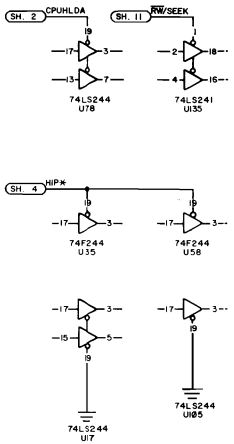
* UI03 MAY USE A PAL16L8A OR PAL20L8 DEPENDING UPON PROGRAM REQUIREMENTS (SEE SHEET 3).

** U72 AND U88 ARE LOCATED IN AN ISOLATED Vcc AND GND AREA (SEE SHEET 7).

SPARE GATES LIST

DEVICE	REF. DESG.	GATES NOT USED
7416	U138	1-6
7438	U19	1-6
74F00	UI08	1-3,11-13
74F02	UI09	4-6
74F08	UI06	4-6,8-13
74F32	U25	11-13
74F32	UI07	1-3,8-10
74LS00	U4	11-13
74LS00	U91	4-6
74LS02	U133	8-10
74LS04	U120	3-6,12,13
74LS04	U141	3-6,10,11
74LS08	U20	1-3
74LS14	U139	1,2
74LS32	U2	1-3
74LS32	U85	4-6,8-10
74LS32	U136	1-6
74LS38	U38	1-6,8-10
74LS38	U87	8-10
74LS74	UI18	8-13
74LS123	UI32	1-4,13-15
74LS125A	U22	11-13
74LS125A	U83	1-6
74S00	U1	1-3
74S157	UI8	9-14
74S260	U93	1-3,5,12,13
MC1489	U7	11-13

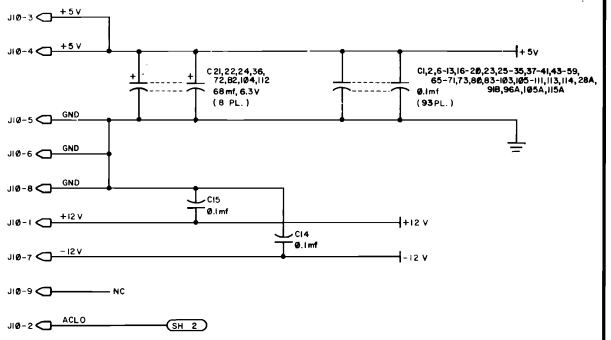
SPARE BUFFERS



REFERENCE DESIGNATORS

LAST USED	NOT USED
UI43	UIII
YI	
RP5	
CR1	
Q2	
JII	
R60	RI7
CII6	
L1	

REVISION				
LTR	DESCRIPTION		DATE	APPROVED
PP1			5/25/83	
PP2			6/27/83	
REV. A	RELEASED FOR PRODUCTION		11/11/83	
A-1	CORRECT U63,64,77(SH2) & UI4(SH9)	BE	2/28/84	
REV. B	REVISED PER TCO NO. 2278 (SH8)	BE	4/7/84	
B-1	REVISED PER TCO NO. 2323 (SH9)	BE	5/1/84	
C	CORRECTED SH5 U67 PI.2,3 & U58 PI3 & I5 HAT		8/10/84	
D	REVISED PER TCO'S NO. 11954, 11582, 11583 & 11584	km	9/19/84	



DC POWER SCHEMATIC

Ø7	REV. D	REVISED PER TCO NO. 1582 VIDEO UNDERLINE	9/19/84
Ø4-Ø6	——	NOT USED	——
Ø3	REV. B	REVISED PER TCO NO. 2273	4/ 7/84
Ø3	REV. A	RELEASED FOR PRODUCTION	11/11/83
Ø3	PP3.5	LIMITED PRODUCTION RELEASE	9/ 1/83
Ø3	PP3	PRE-PROTOTYPE	8/22/83
Ø2	PP2	PRE-PROTOTYPE	6/27/83
Ø1	PP1	PRE-PROTOTYPE	
HEX CODE	PCB REV. LTR.	DESCRIPTION	DATE

CONFIGURATION STATUS ⚠

⚠ CONFIGURATION STATUS PORT: THE MAIN LOGIC BOARD HAS AN 8-BIT PORT THAT INDICATES THE CONFIGURATION STATUS OF THE PRINTED CIRCUIT BOARD WITH RESPECT TO SOFTWARE. THE INPUT STRAPPING TO THIS REGISTER (UI0) MUST BE INCREMENTED BY ONE FOR EACH REVISION OF THE PC BOARD THAT DIRECTLY AFFECTS PROGRAMMING. THE HEX CODE FOR EACH PC BOARD CONFIGURATION CHANGE APPEARS IN THE CONFIGURATION STATUS SCHEDULE AT RIGHT (SEE SHEET 12).

REF. DRILL PLAN 1700245 REV. B

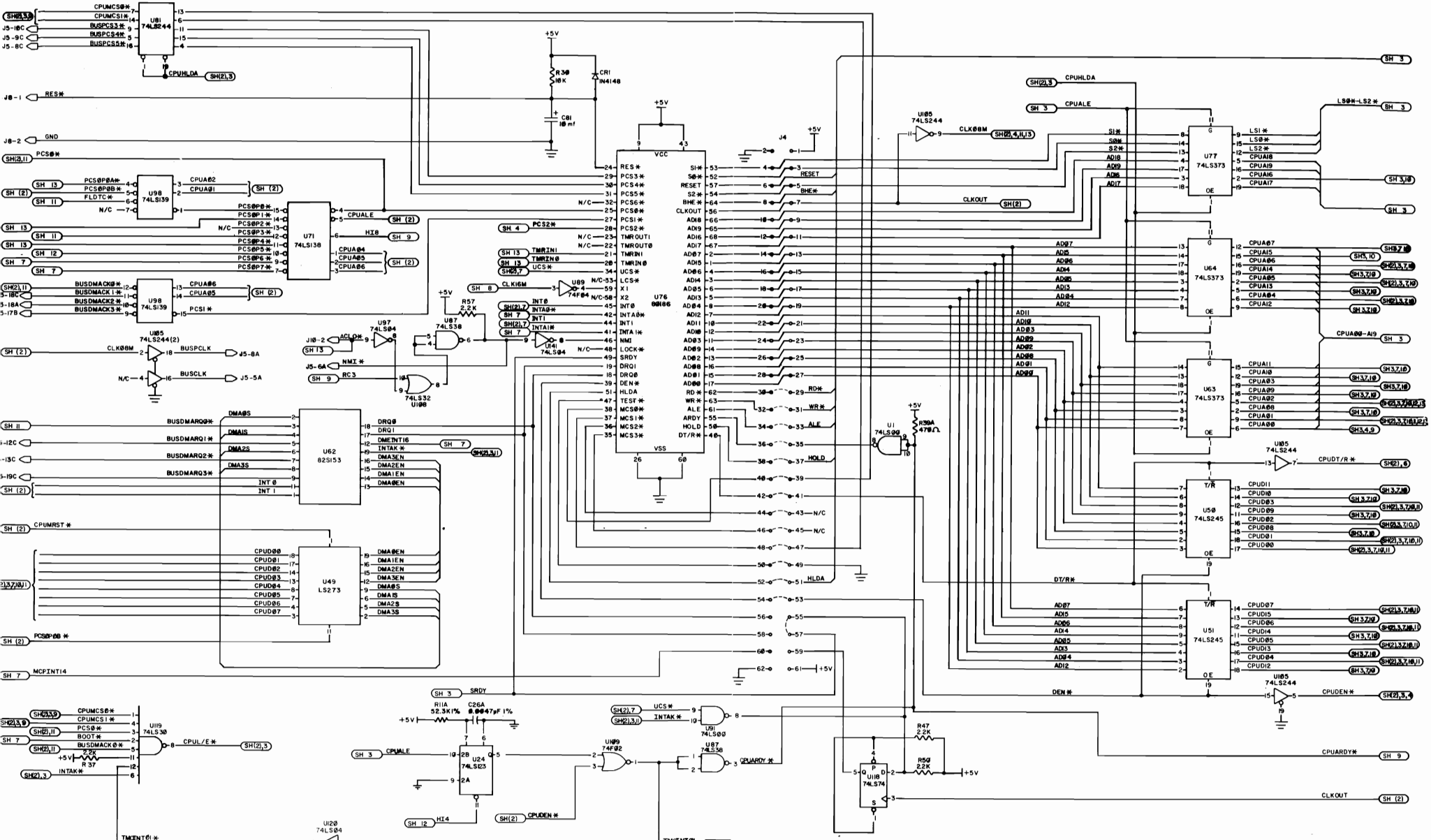
DRAFT	D.CRONCH, K.NEWTON	DATE	7/83
CHECK		DATE	
DESIGN		DATE	
APPD		DATE	
APPD		DATE	

TITLE: **SCHEMATIC- MAIN LOGIC BOARD PROJECT J-507**

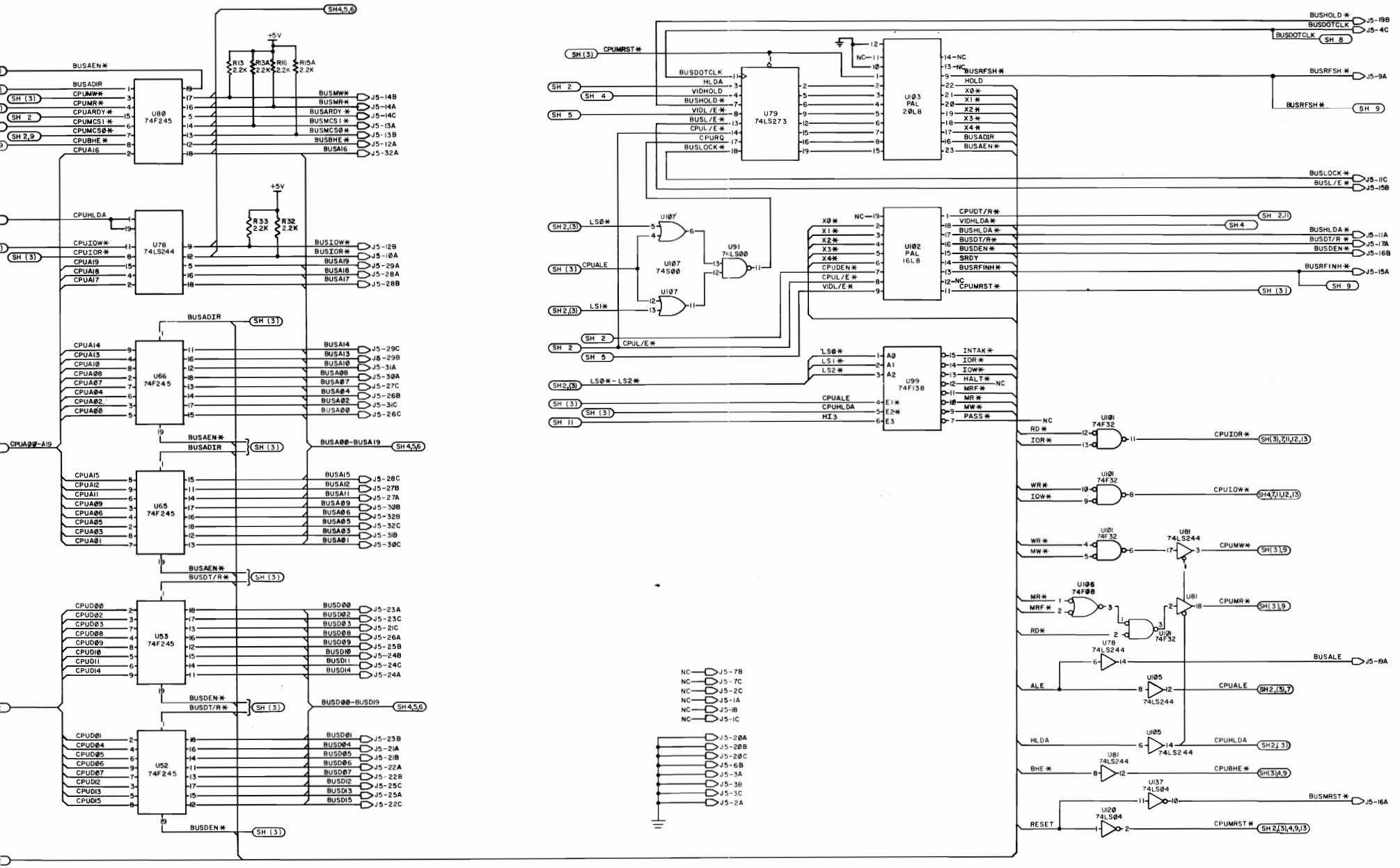
tandy

DWG NO 8000203 SIZE D

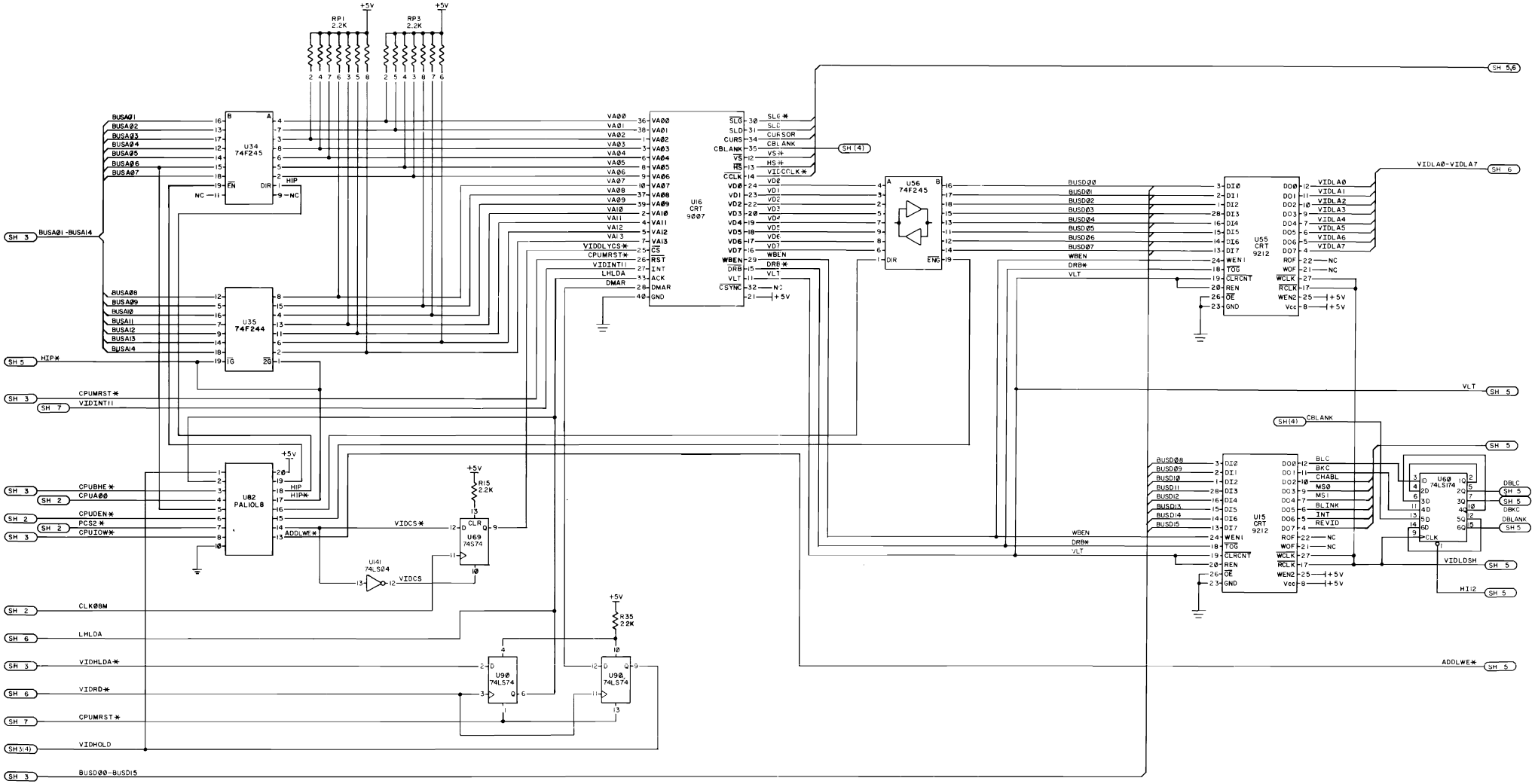
SCALE N/A SHEET 1 OF 13



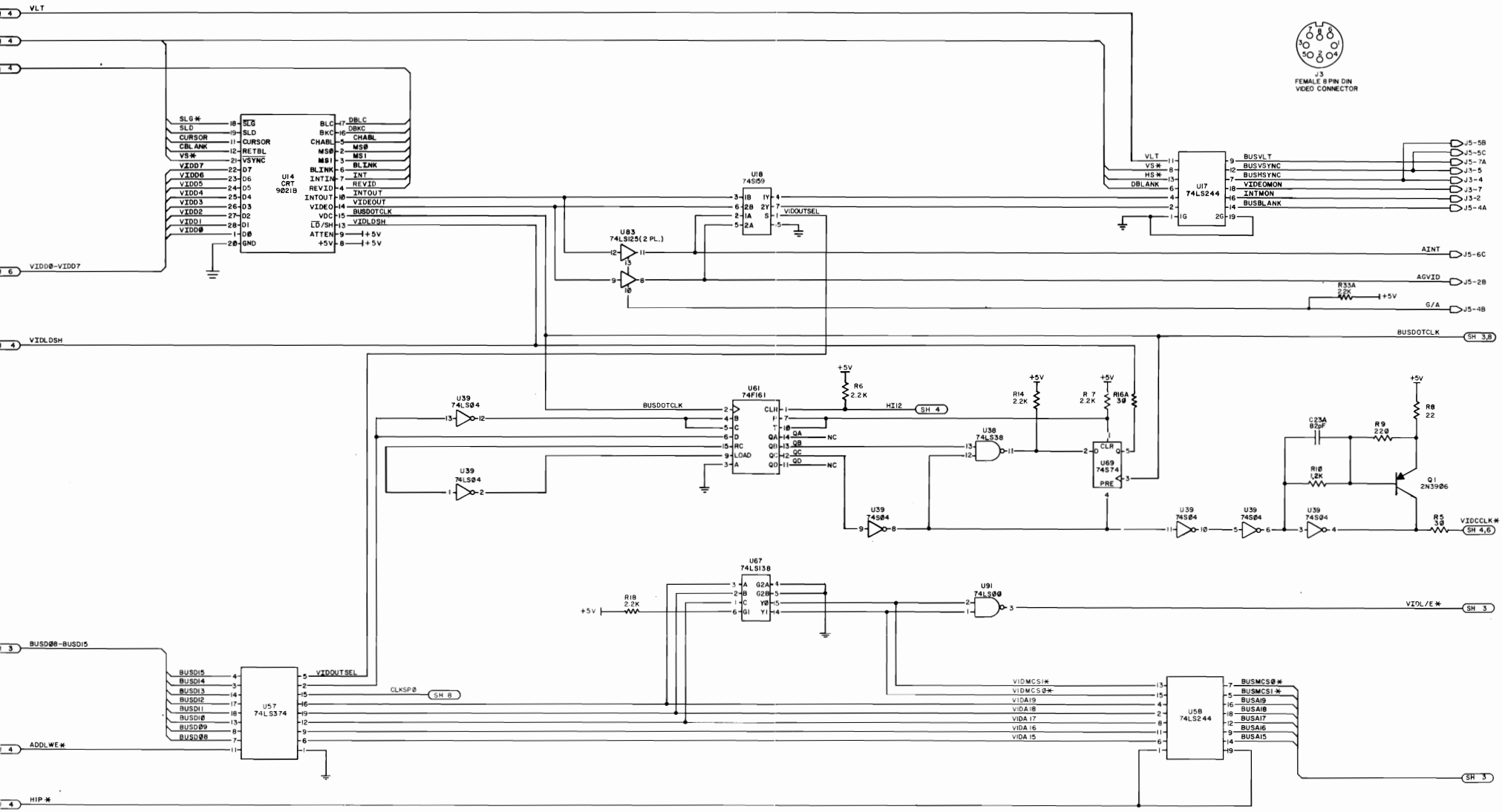
Main Logic Board Schematic 80000203A, Model 2000 Computer
Page 2 of 13



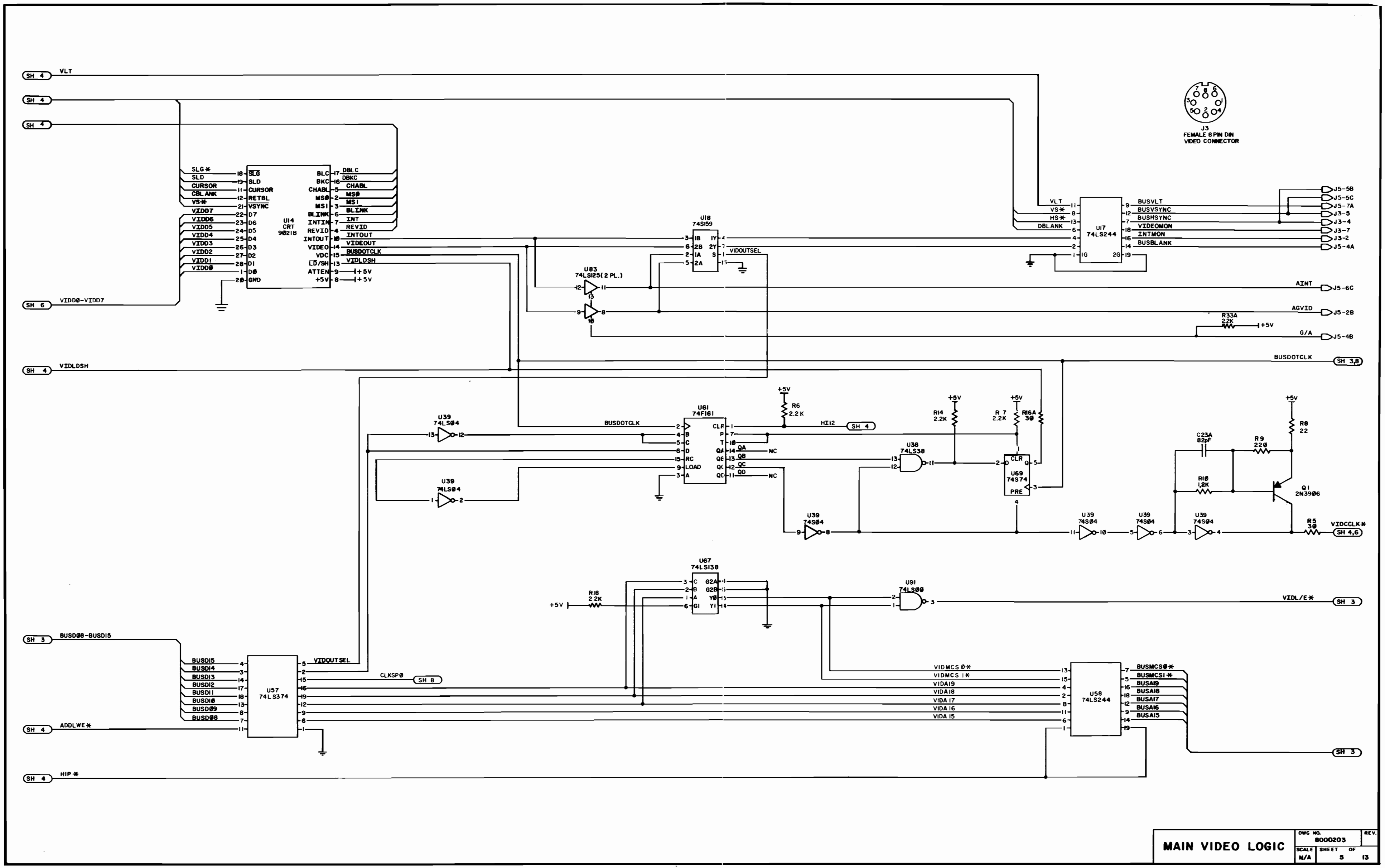
Main Logic Board Schematic 80000203A, Model 2000 Computer
Bus Interface **Page 3 of 13**

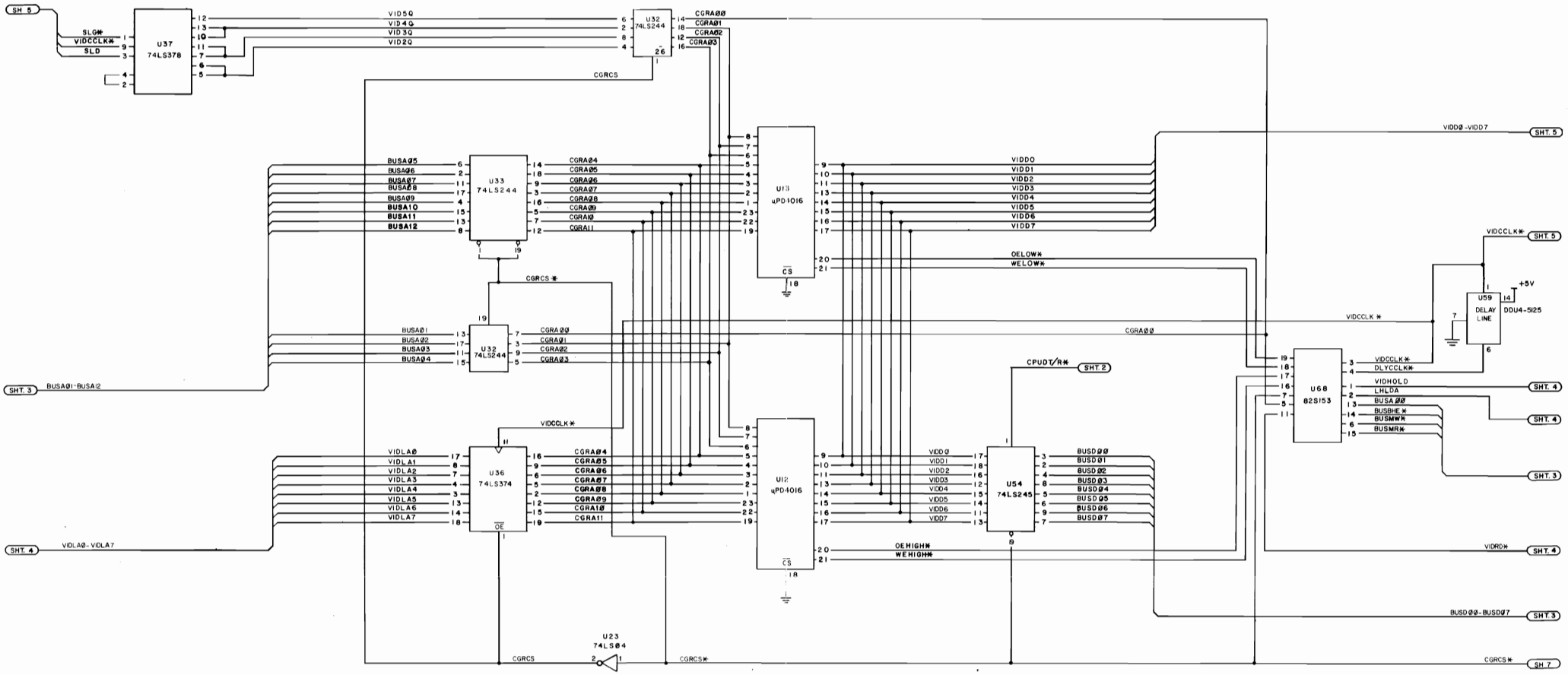


Main Logic Board Schematic 80000203A, Model 2000 Computer
CRT Controller/Main Video Logic Page 4 of 13

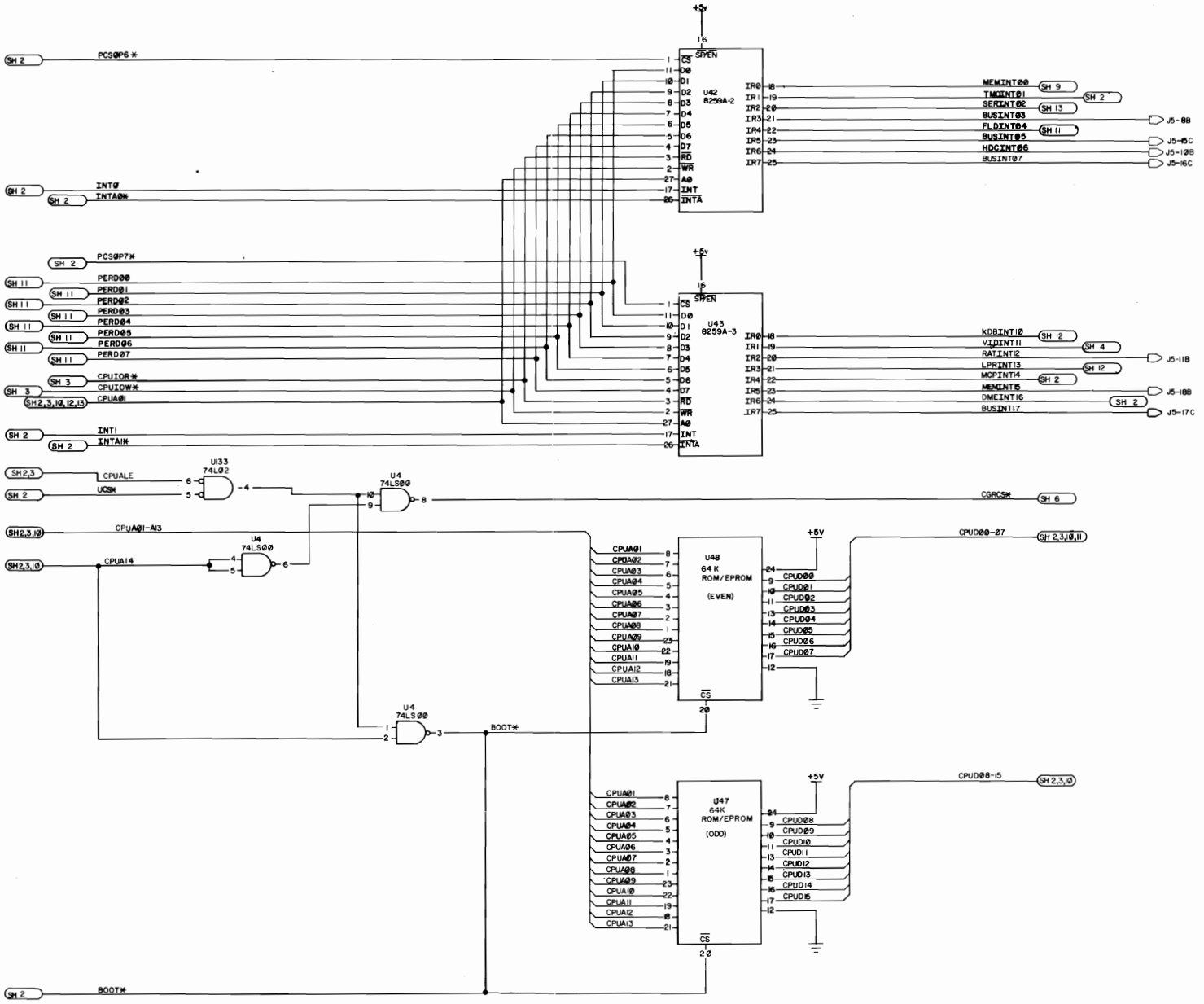


Main Logic Board Schematic 80040203A, Model 2000 Computer
Main Video Logic Page 5 of 13

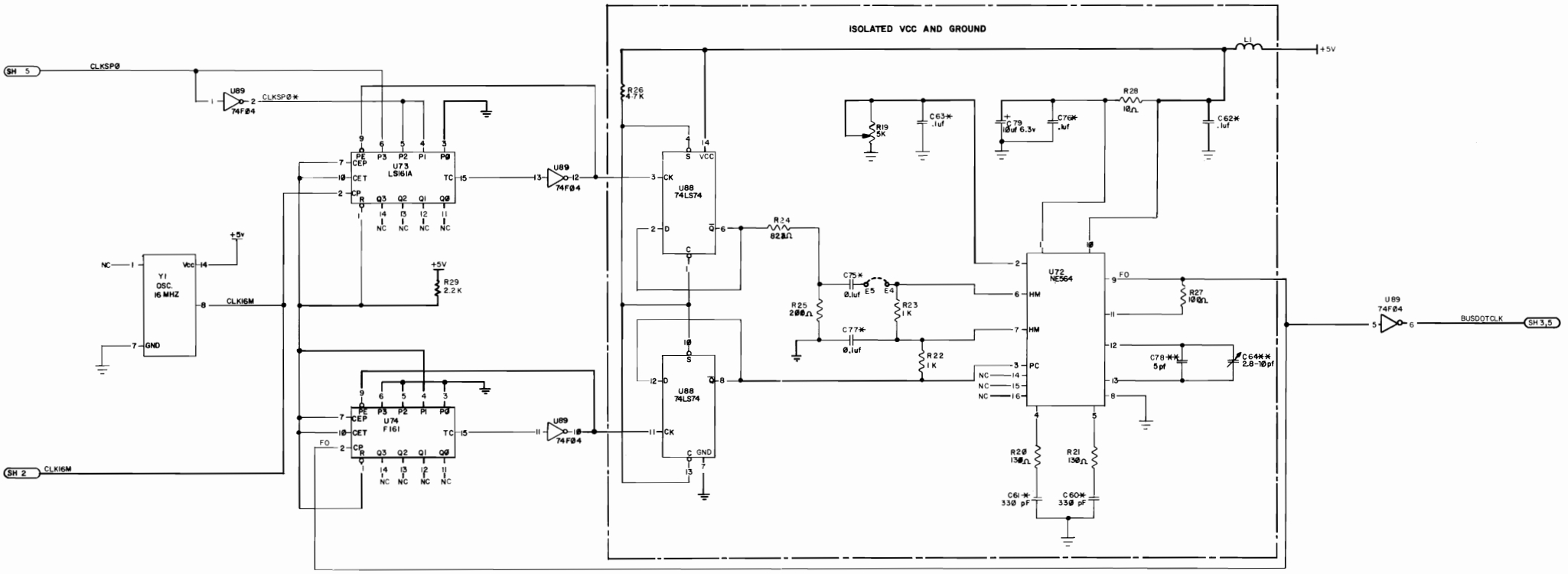

MAIN VIDEO LOGIC
DWG NO. 8000203
SCALE N/A
SHEET 5 OF 13
U14 CRT 9021B
U18 74S159
U83 74LS125 (2 PL.)
U17 74LS244
U61 74F161
U39 74LS04
U38 74LS38
U69 74S74
U67 74LS138
U91 74LS00
U57 74LS374
U58 74LS244
Q1 2N3906
J3 FEMALE 8 PIN DIN VIDEO CONNECTOR
VLT
VIDLDSH
VIDD0-VIDD7
BUSD08-BUSD15
ADDLWE*
HIP*
BUSDOTCLK
VIDOUTSEL
CLKSP0
HI12
AINT
AGVID
G/A
VIDL/E*
VIDCCLK*



Main Logic Board Schematic 80000203A, Model 2000 Computer
Character Generator I/F Logic Page 6 of 13



Main Logic Board Schematic 80000203A, Model 2000 Computer
Interrupt Controller/Boot ROM Page 7 of 13



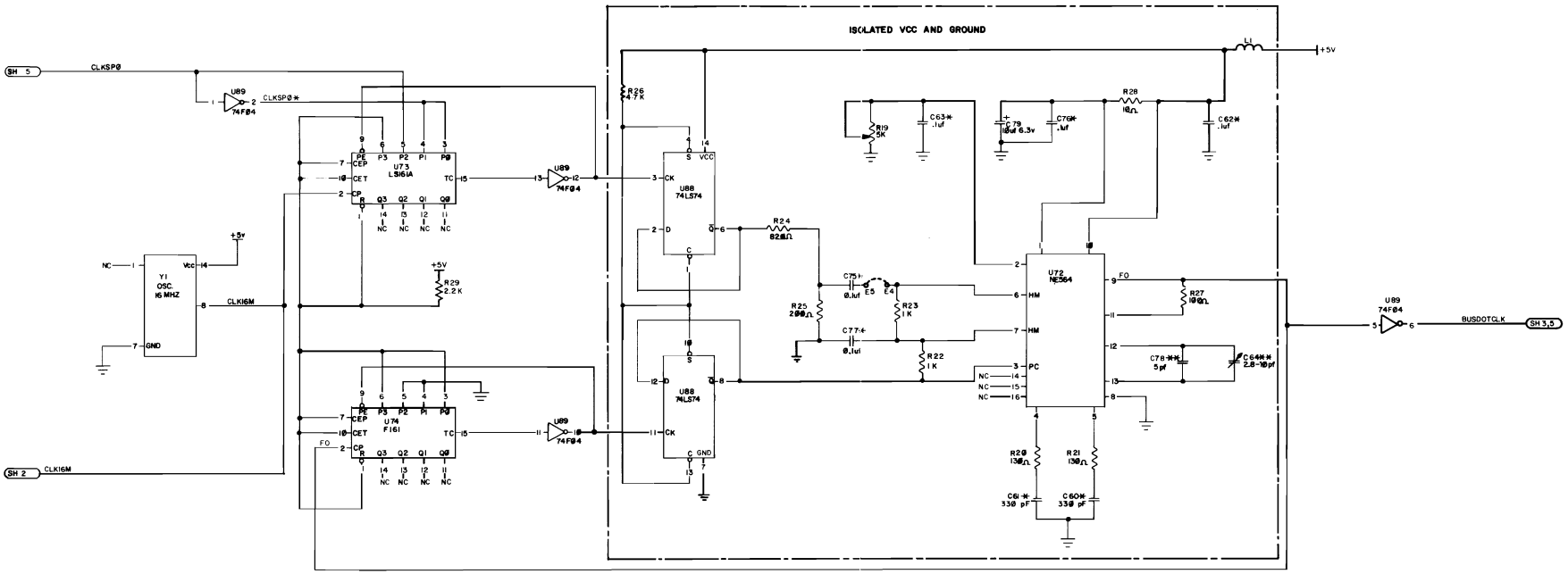
* – MUST BE THOMPSON CSF CAPACITORS

** – MUST BE NPO TEMPATURE COEFFICIENT CAPACITORS

$FO = \frac{CLKI6M \times 28}{16 \text{ or } 18 \text{ or } 20}$

	Fin (MHZ)	
Fout (MHZ)	15.990921	16.000
	27.984111	28.00
	22.387289	22.400

Main Logic Board Schematic 80000203A, Model 2000 Computer
Clock/Phase Lock Loop Page 8 of 13



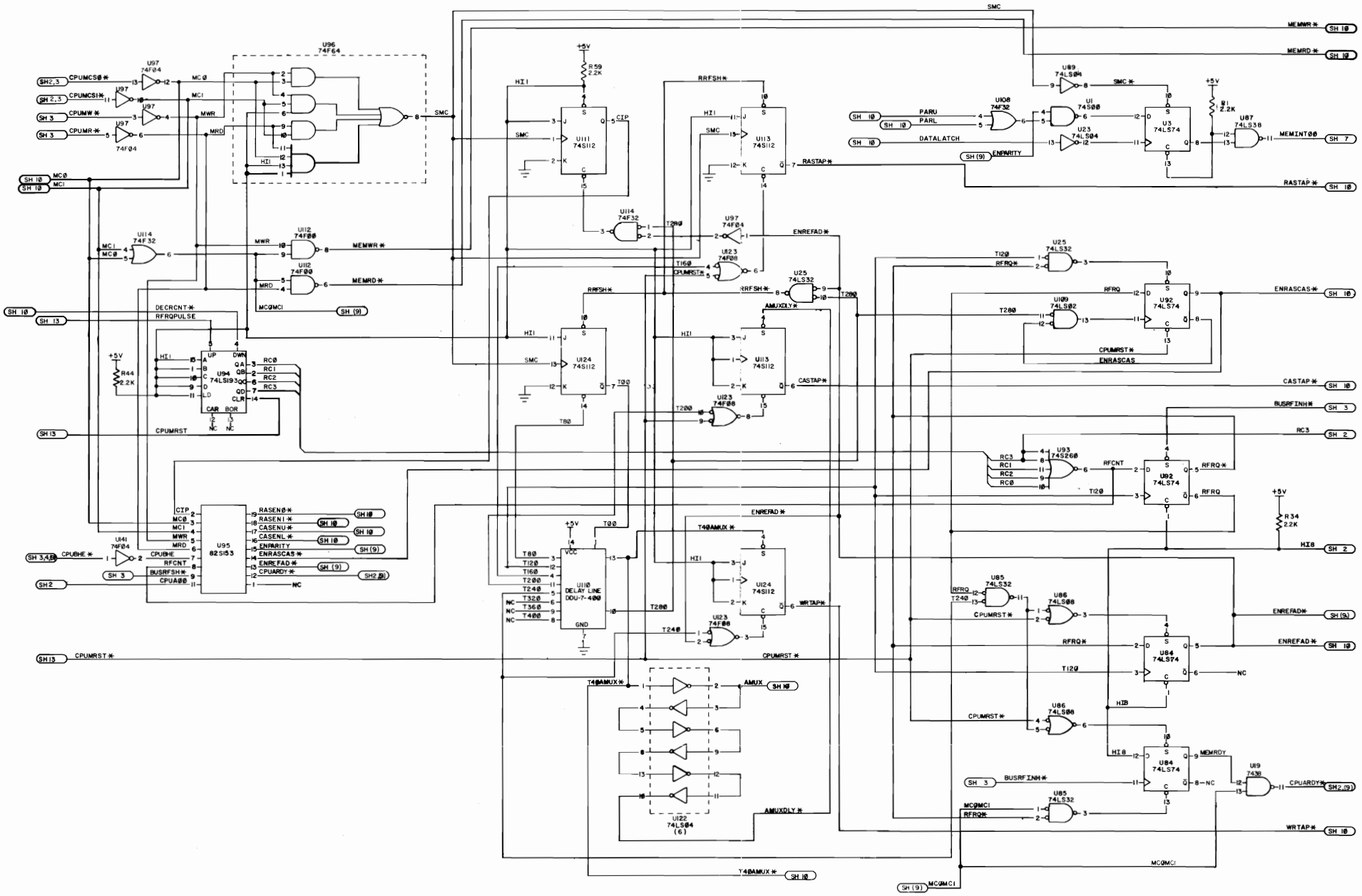
* – MUST BE THOMPSON CSF CAPACITORS

** – MUST BE NPO TEMPATURE COEFFICIENT CAPACITORS

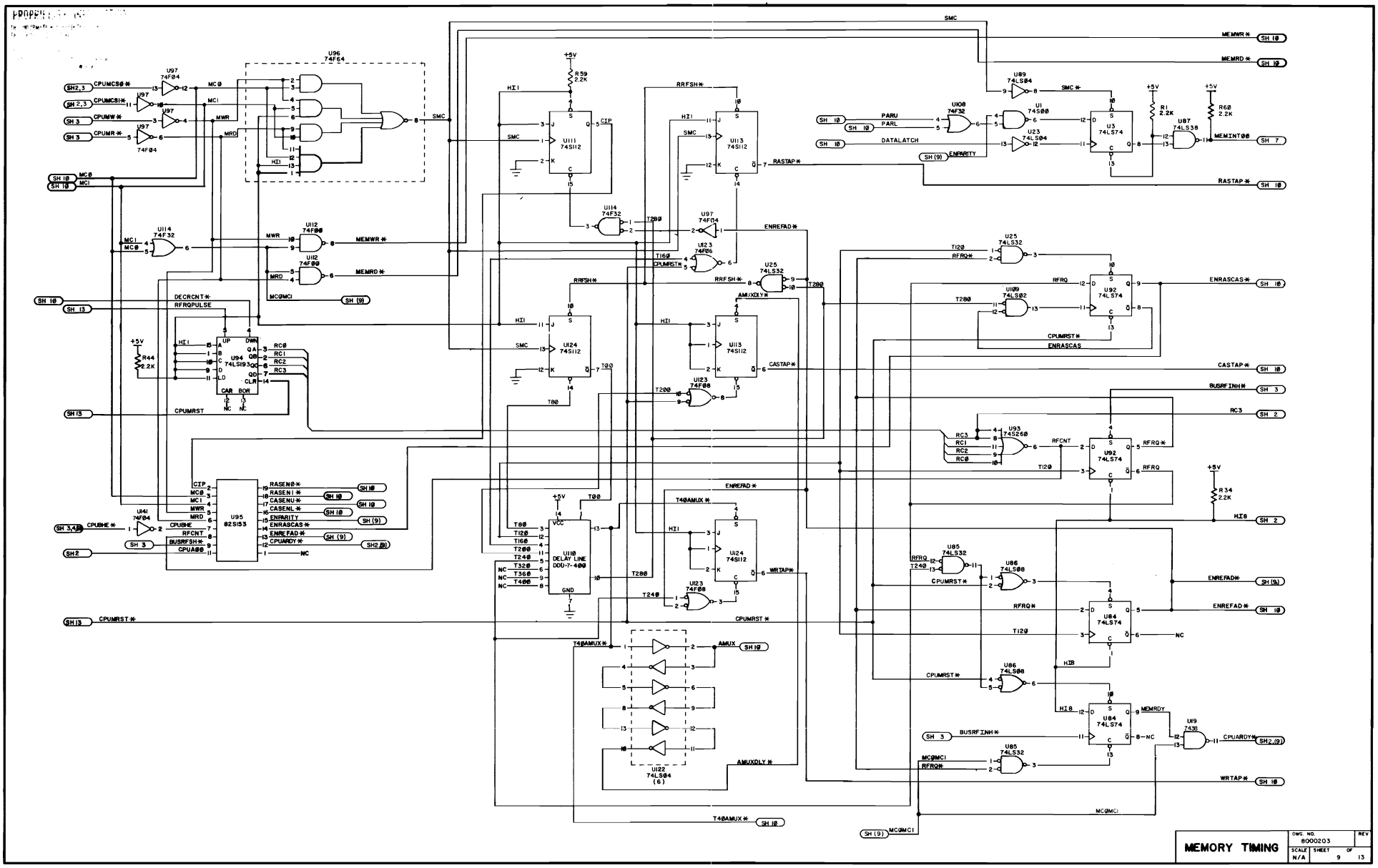
$FO = \frac{CLK16M \times 28}{16 \text{ or } 18 \text{ or } 20}$

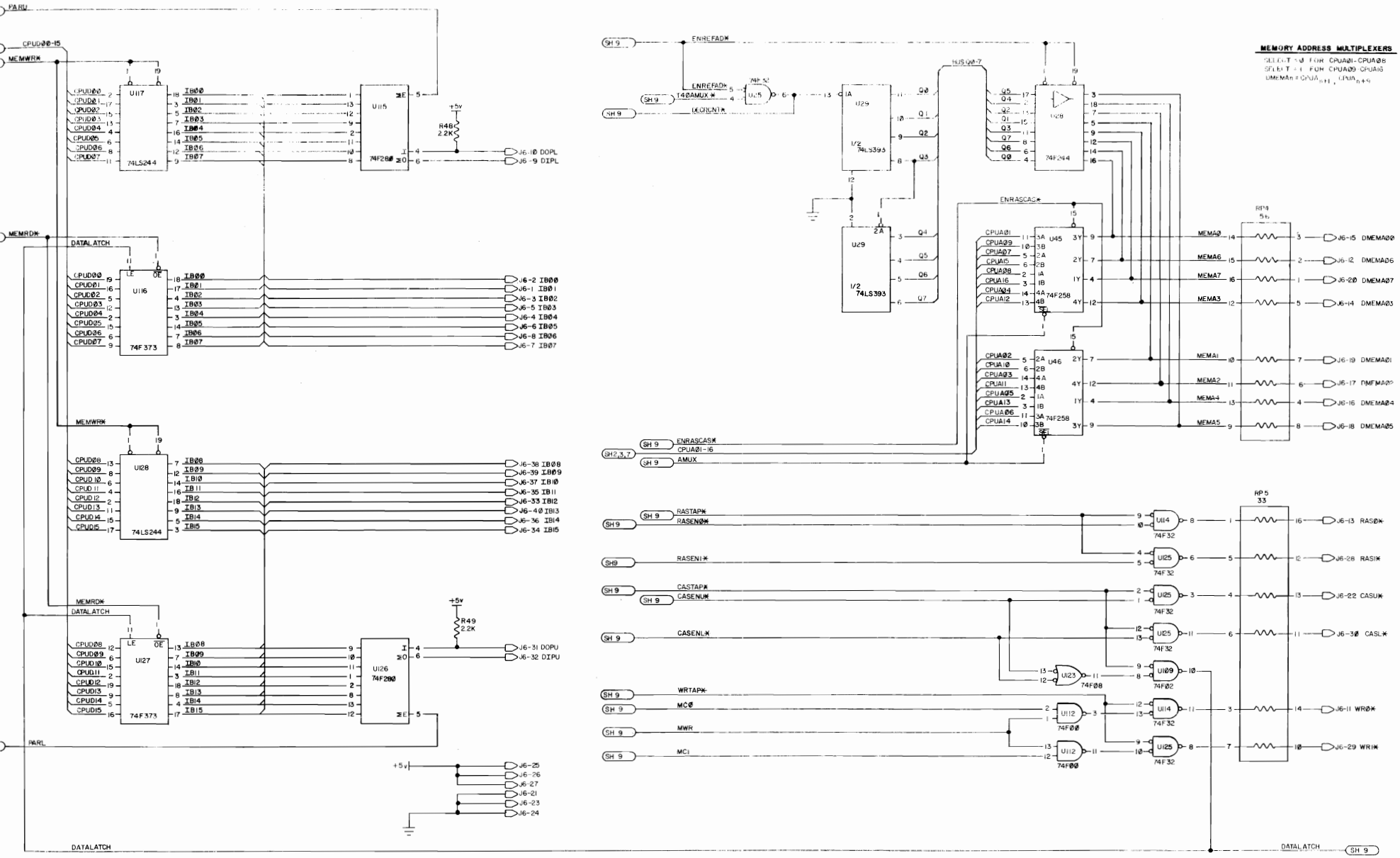
	Fin (MHZ)	
Fout (MHZ)	15.990921	16.000
	27.984111	28.00
	22.387289	22.400

CLOCK/PHASE LOCK LOOP	DWG NO 8000203	SIZE D
	SCALE N.A	SHEET 8 OF 13

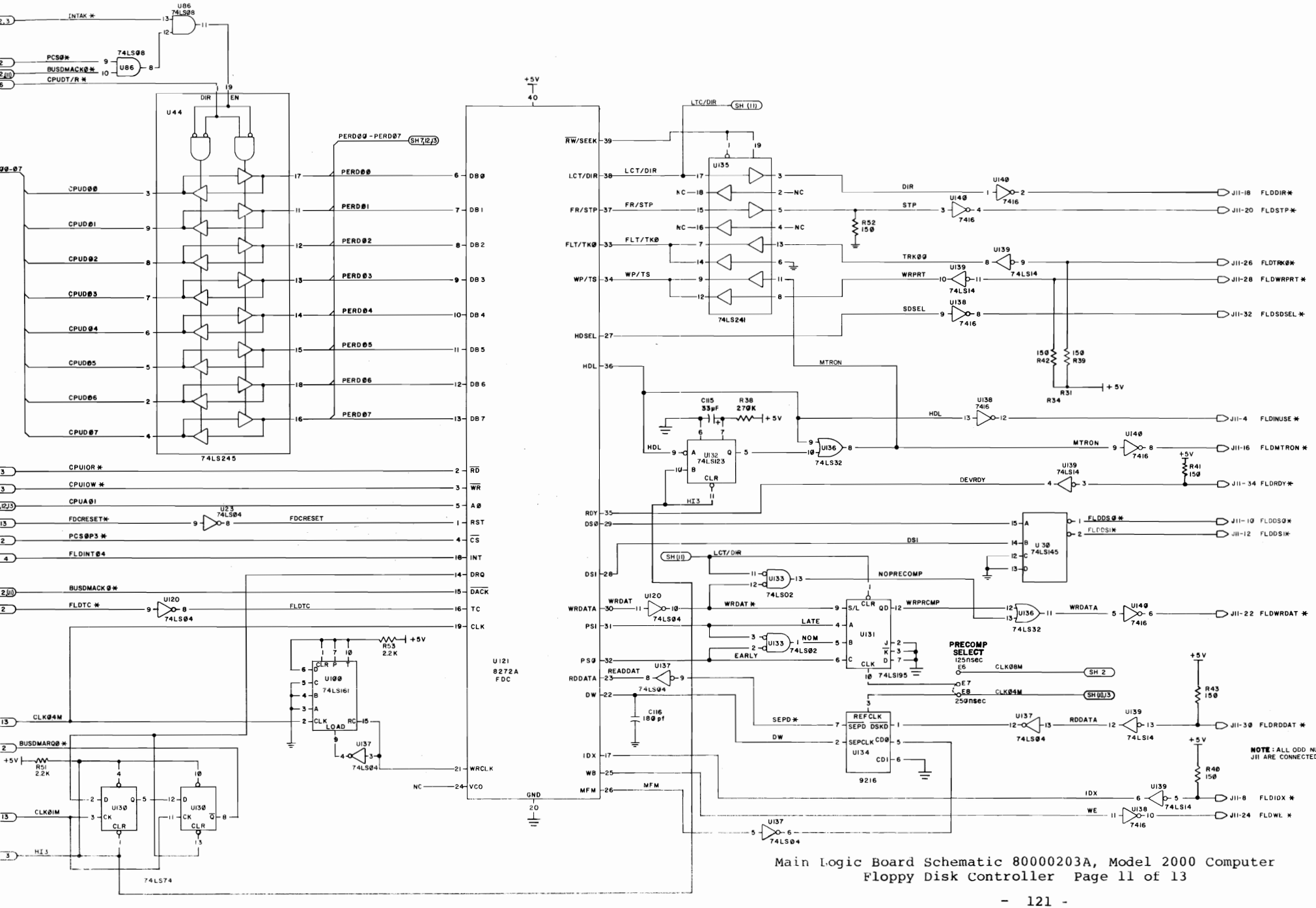


Main Logic Board Schematic 80000203A, Model 2000 Computer
Memory Timing Page 9 of 13

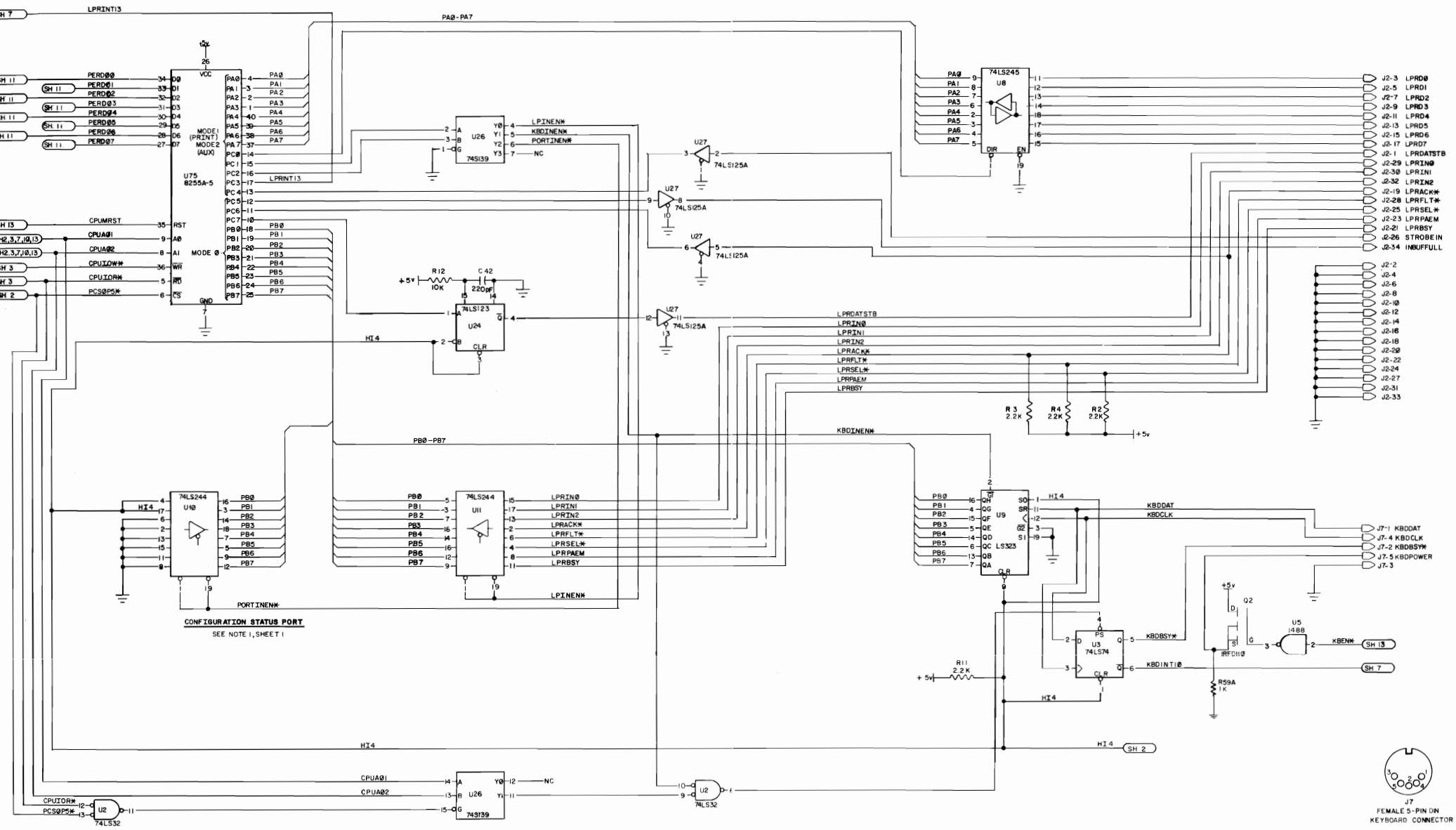

MEMORY TIMING
DWG. NO. 8000203
REV
SCALE N/A
SHEET 9 OF 13



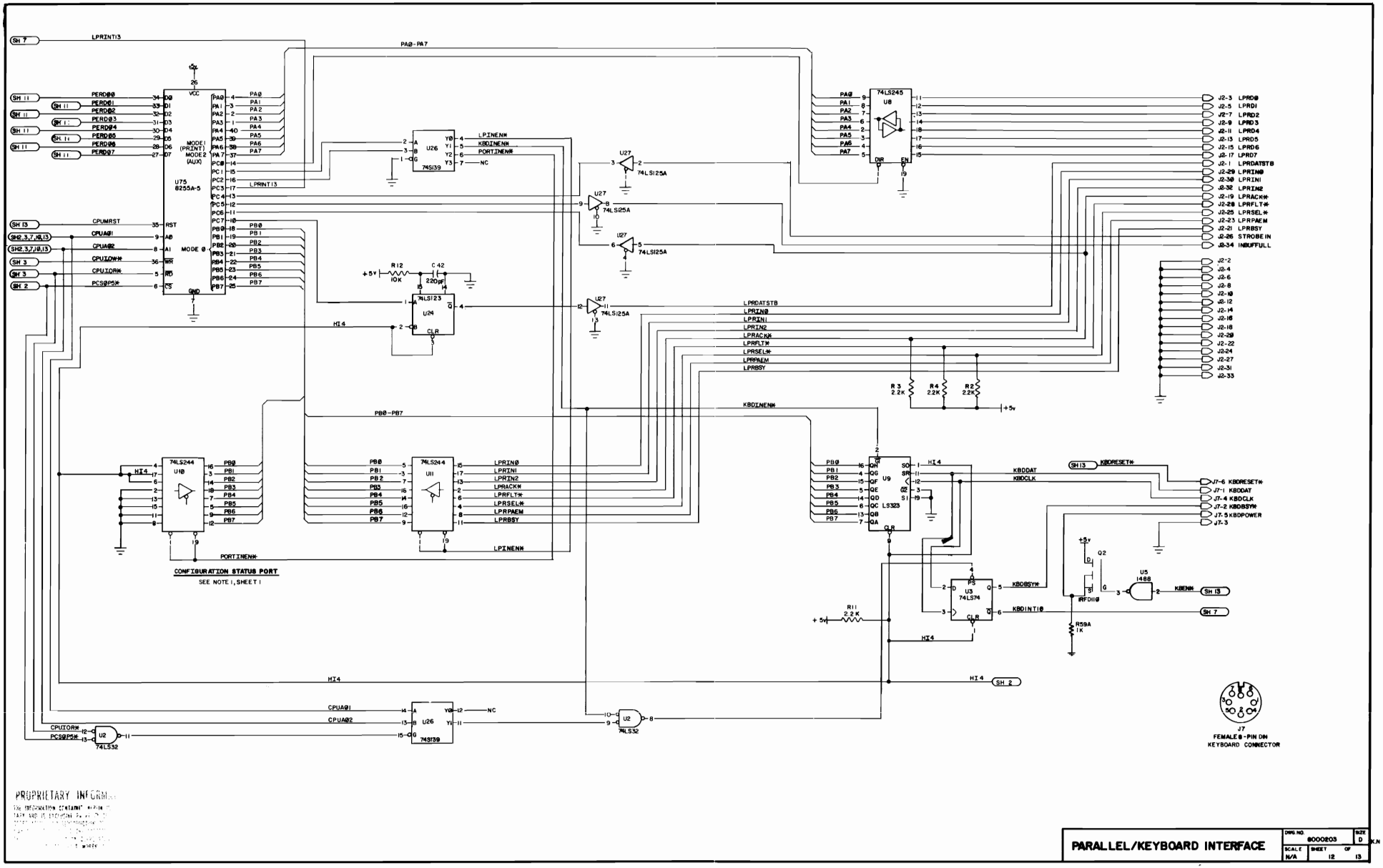
Main Logic Board Schematic 80000203A, Model 2000 Computer
Memory Control Page 10 of 13

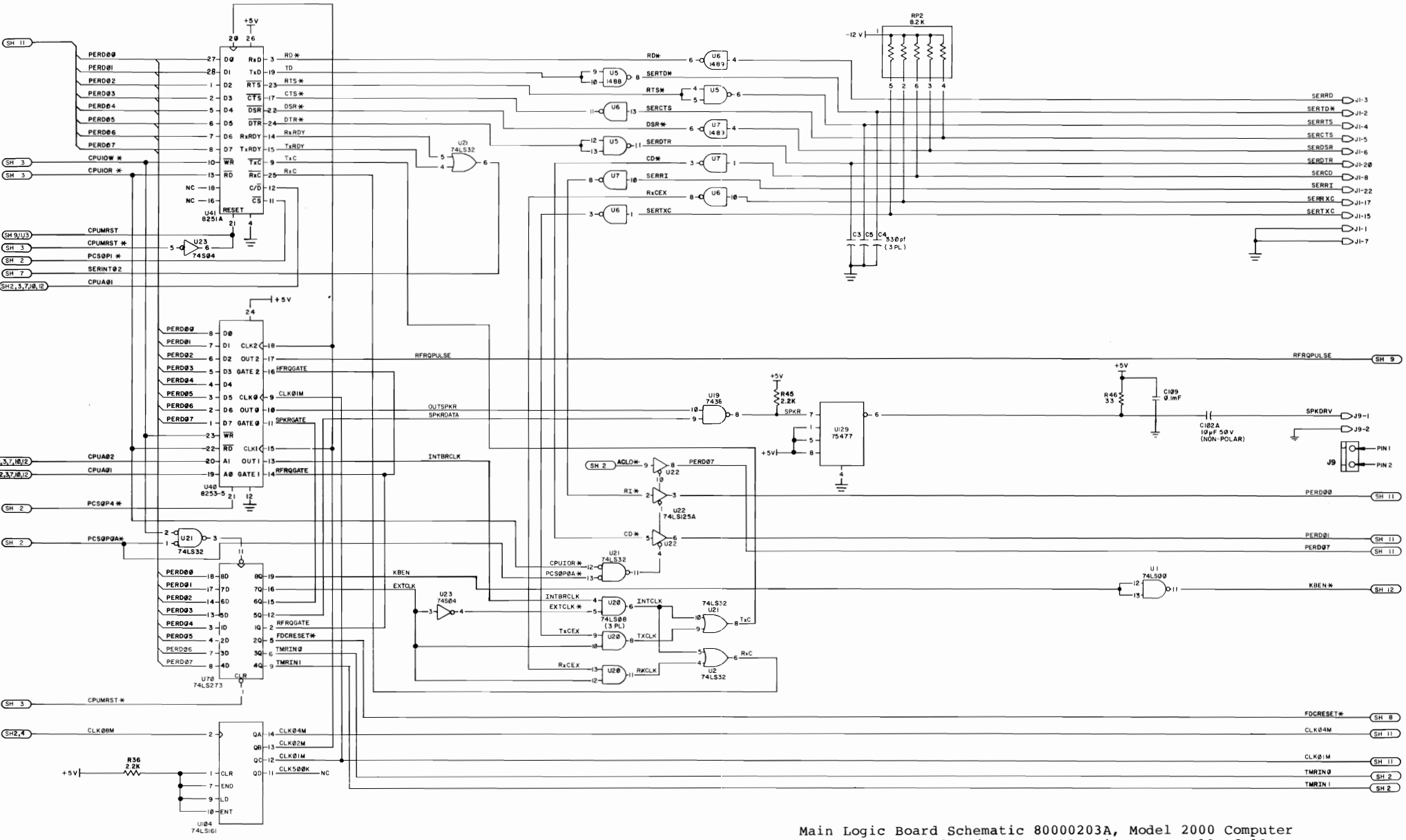


Main Logic Board Schematic 80000203A, Model 2000 Computer
Floppy Disk Controller Page 11 of 13

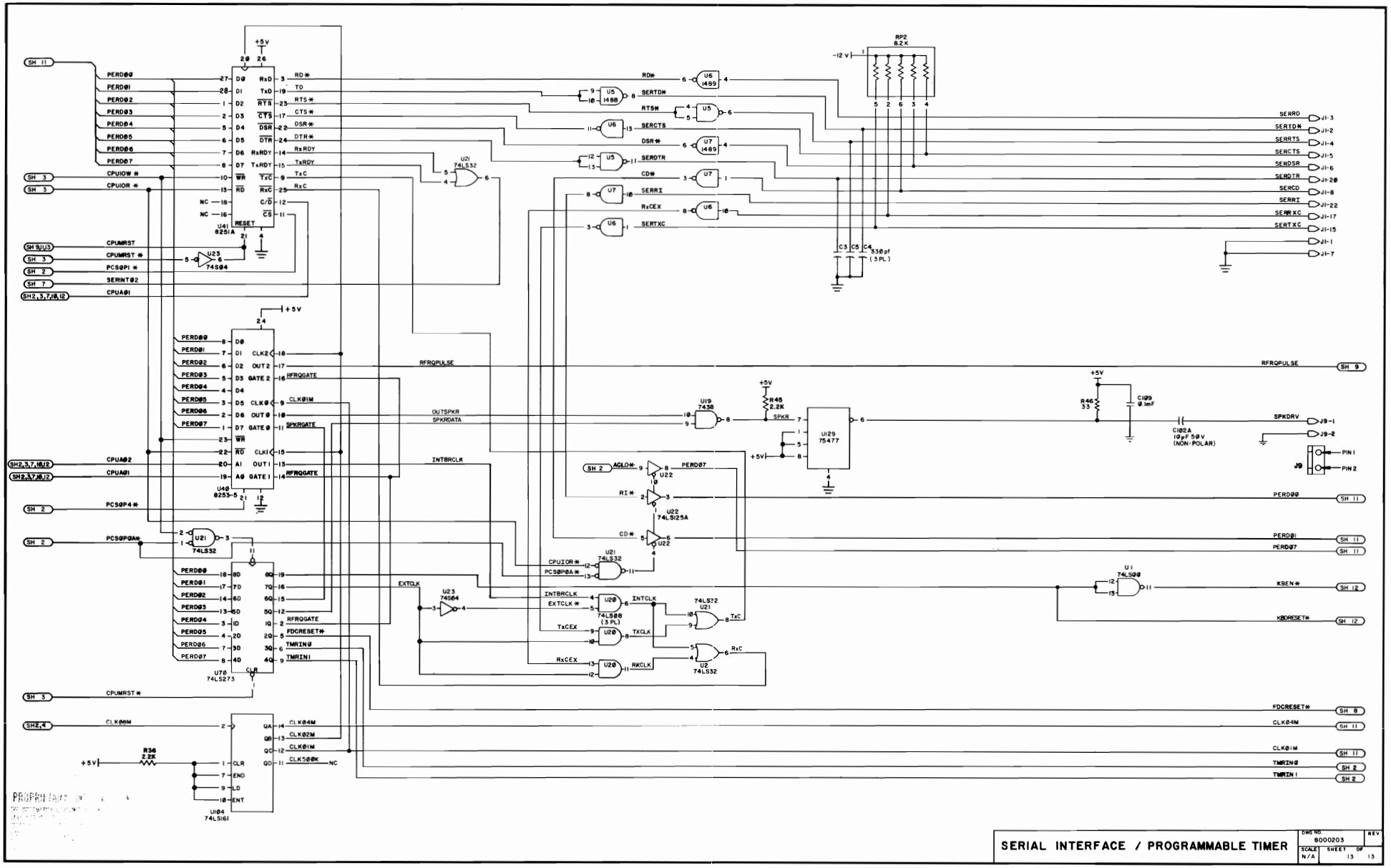


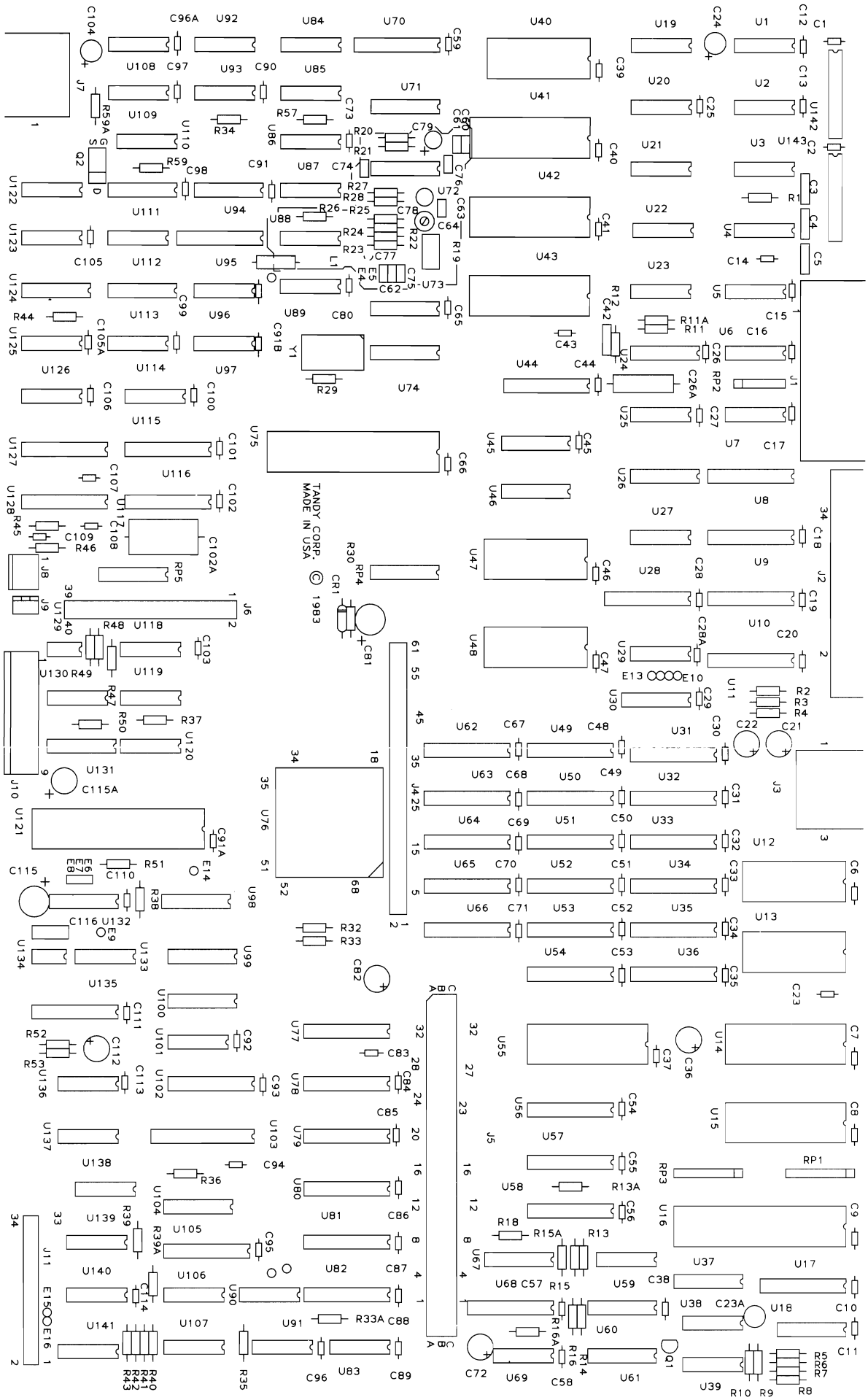
Main Logic Board Schematic 80000203A, Model 2000 Computer
Parallel/Keyboard Interface Page 12 of 13


PARALLEL/KEYBOARD INTERFACE
DWG NO. 8000203
SIZE D
SCALE N/A
SHEET 12 OF 13
J7
FEMALE 8-PIN DIN
KEYBOARD CONNECTOR
CONFIGURATION STATUS PORT
SEE NOTE 1, SHEET 1
U75 8255A-5
74LS245
74LS244
74LS123
74LS125A
74LS139
74LS32
74LS74
LS323
74LS88
PROPRIETARY INFORM

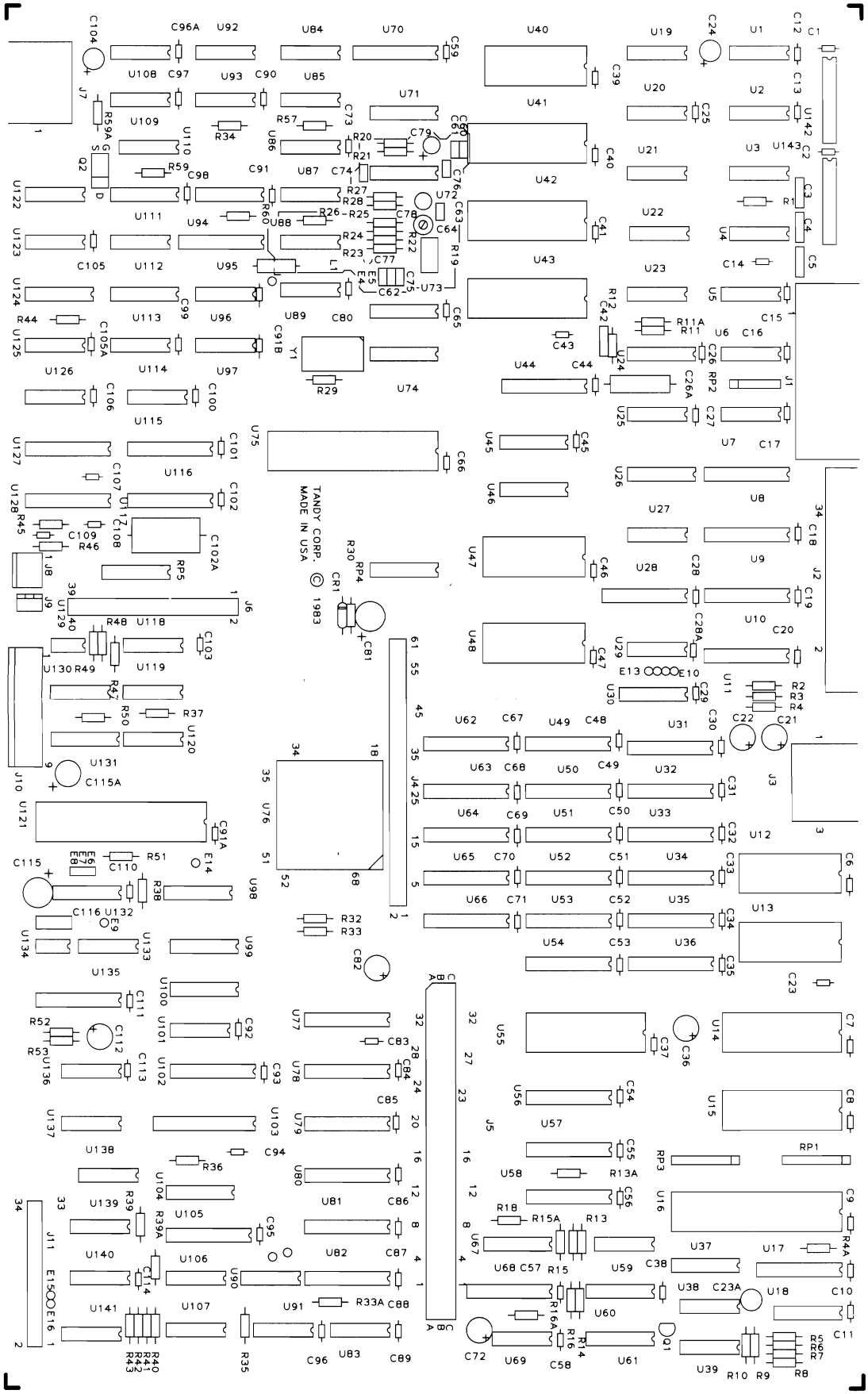


Main Logic Board Schematic 80000203A, Model 2000 Computer
Serial Interface/Programmable Timer Page 13 of 13


SERIAL INTERFACE / PROGRAMMABLE TIMER
DWG NO. 8000203
REV
SCALE N/A
SHEET 13 OF 13
PROPRIETARY



Component Layout 1700245, Main Logic Board 8898800A
Model 2000 Computer Assembly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MADE IN USA
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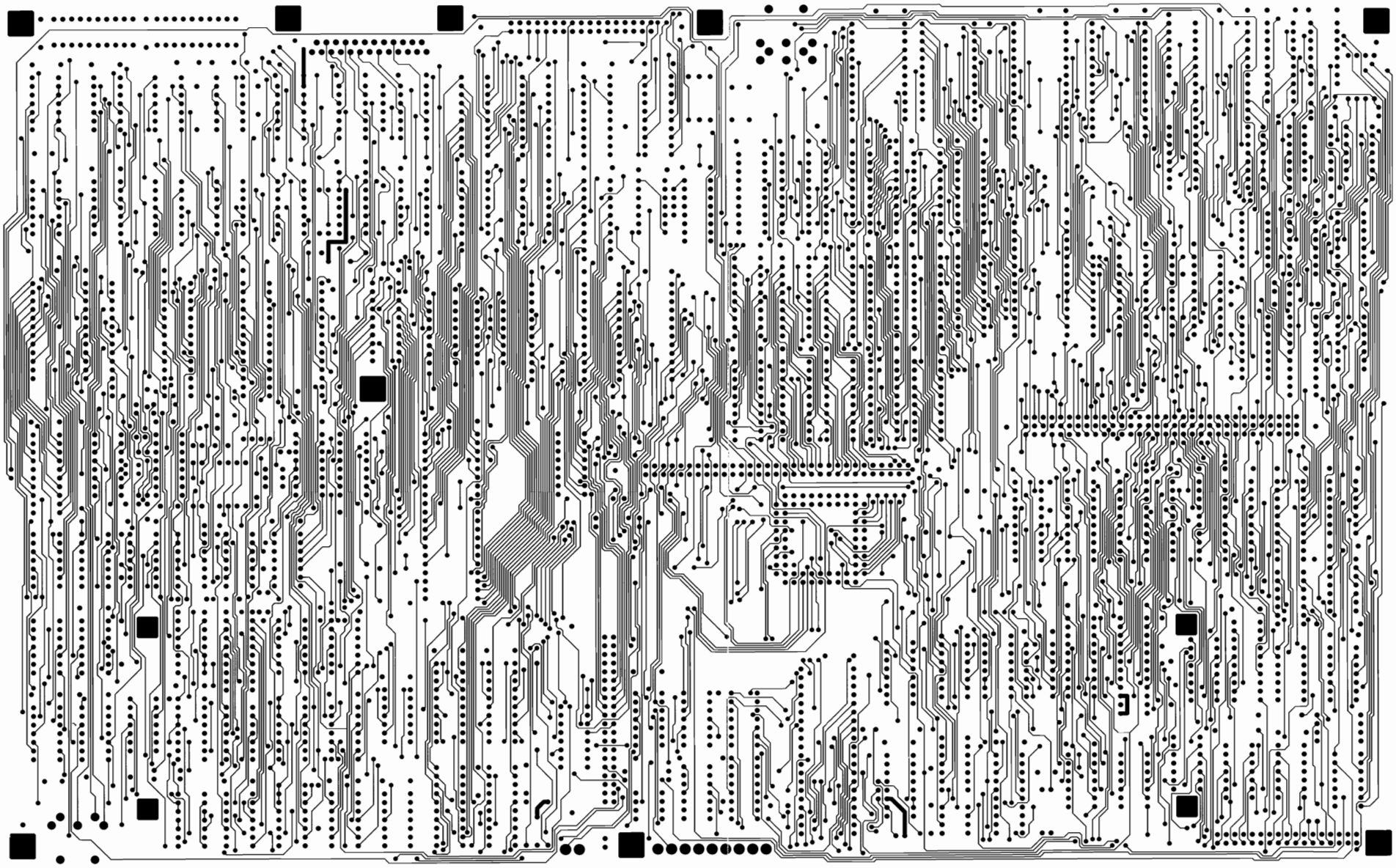
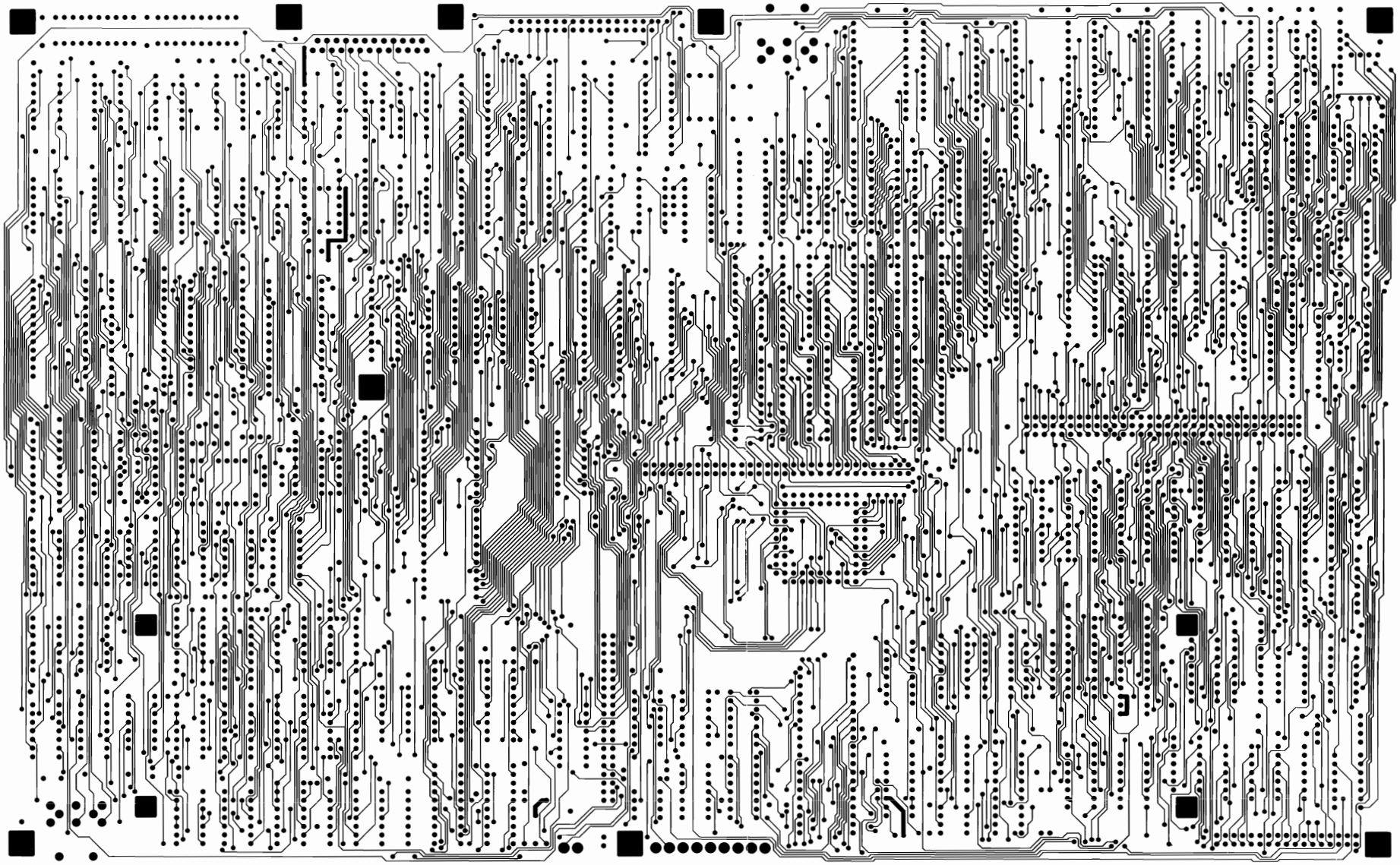
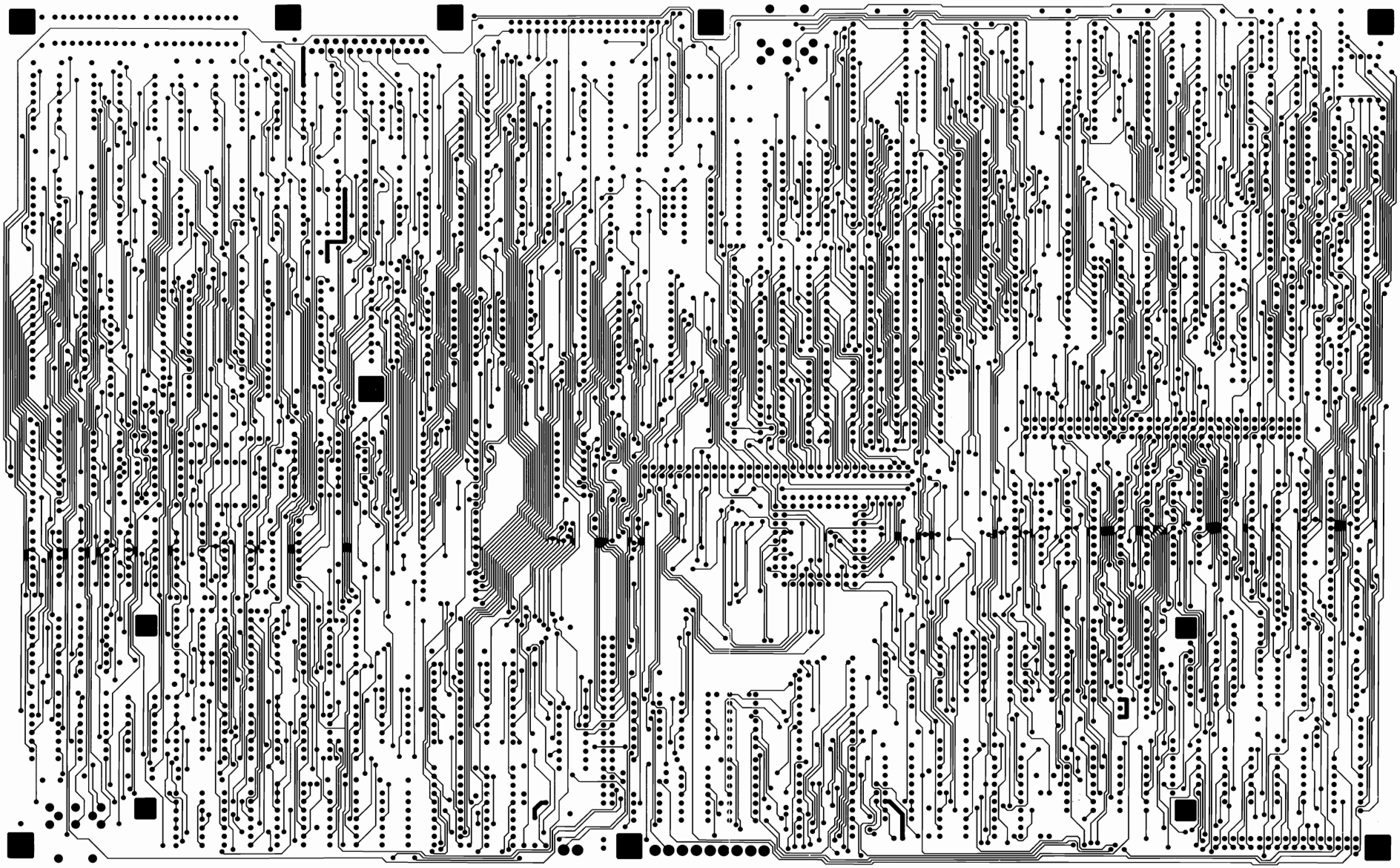


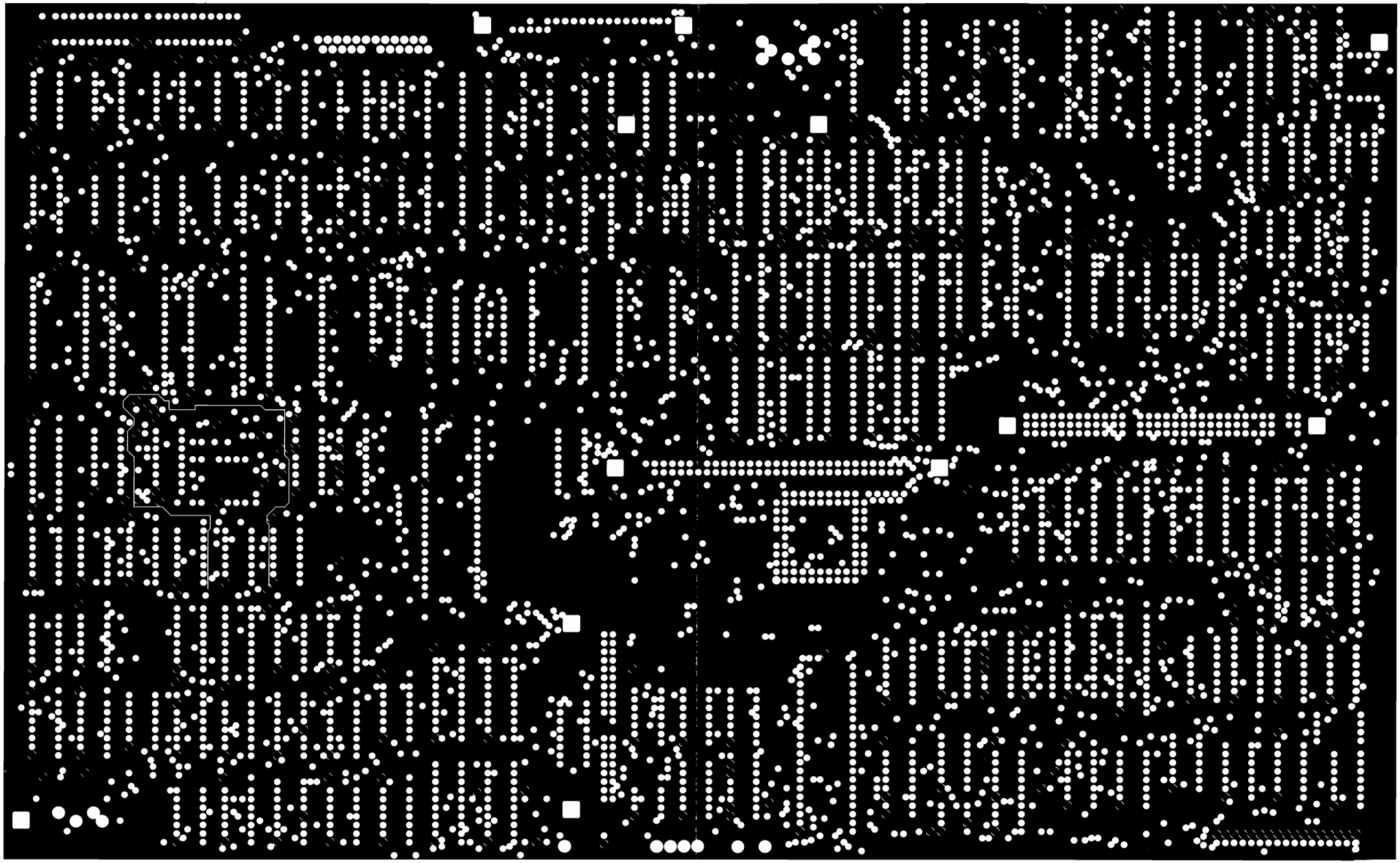
Circuit Trace 1700245, Component Side
Main Logic PCB Assembly 8898800A



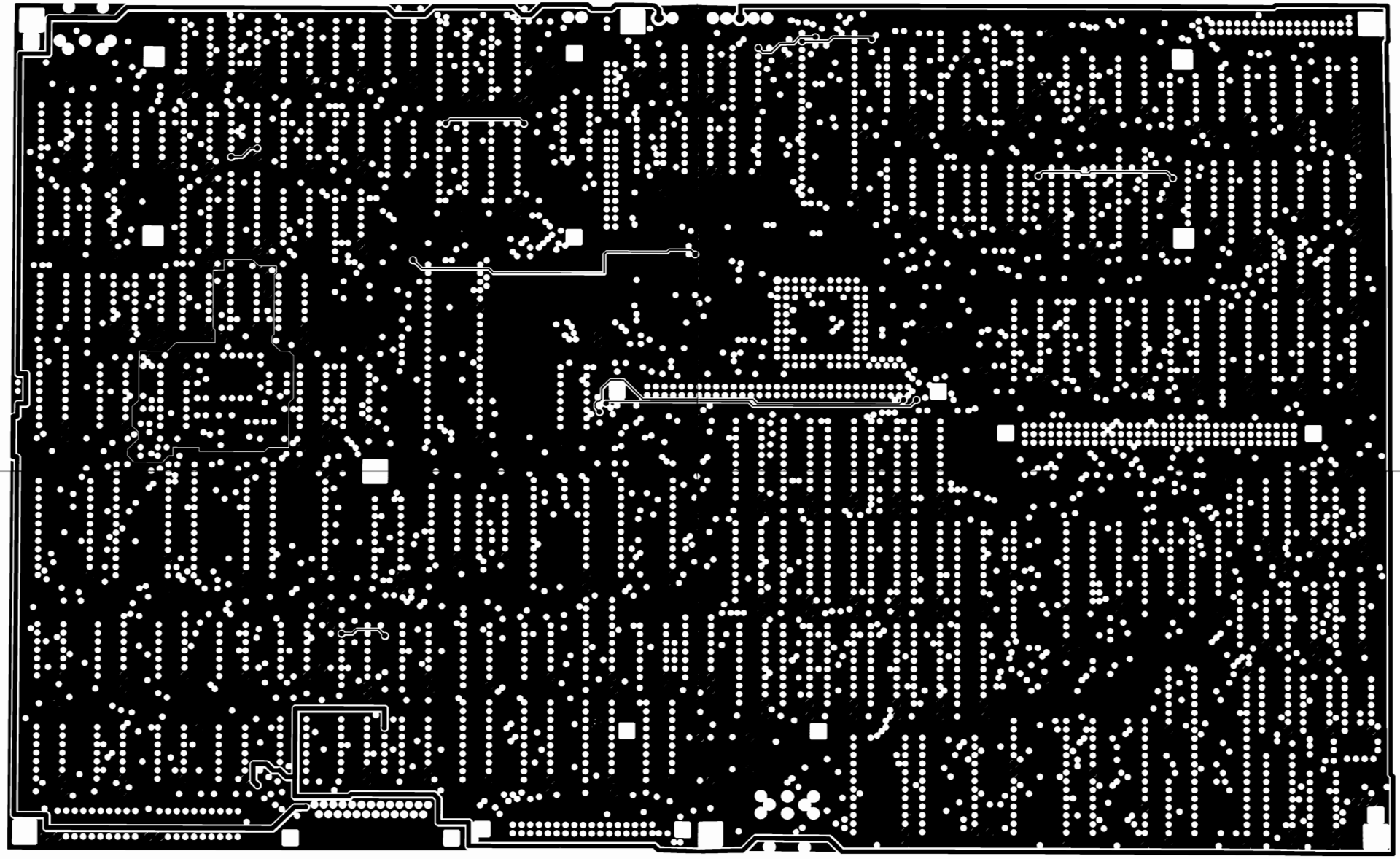
TANDY CORP.
MODEL J-507 MAIN BD.
REF. DWG. NO. 1700245
LAYER 1 ARTWORK REV B



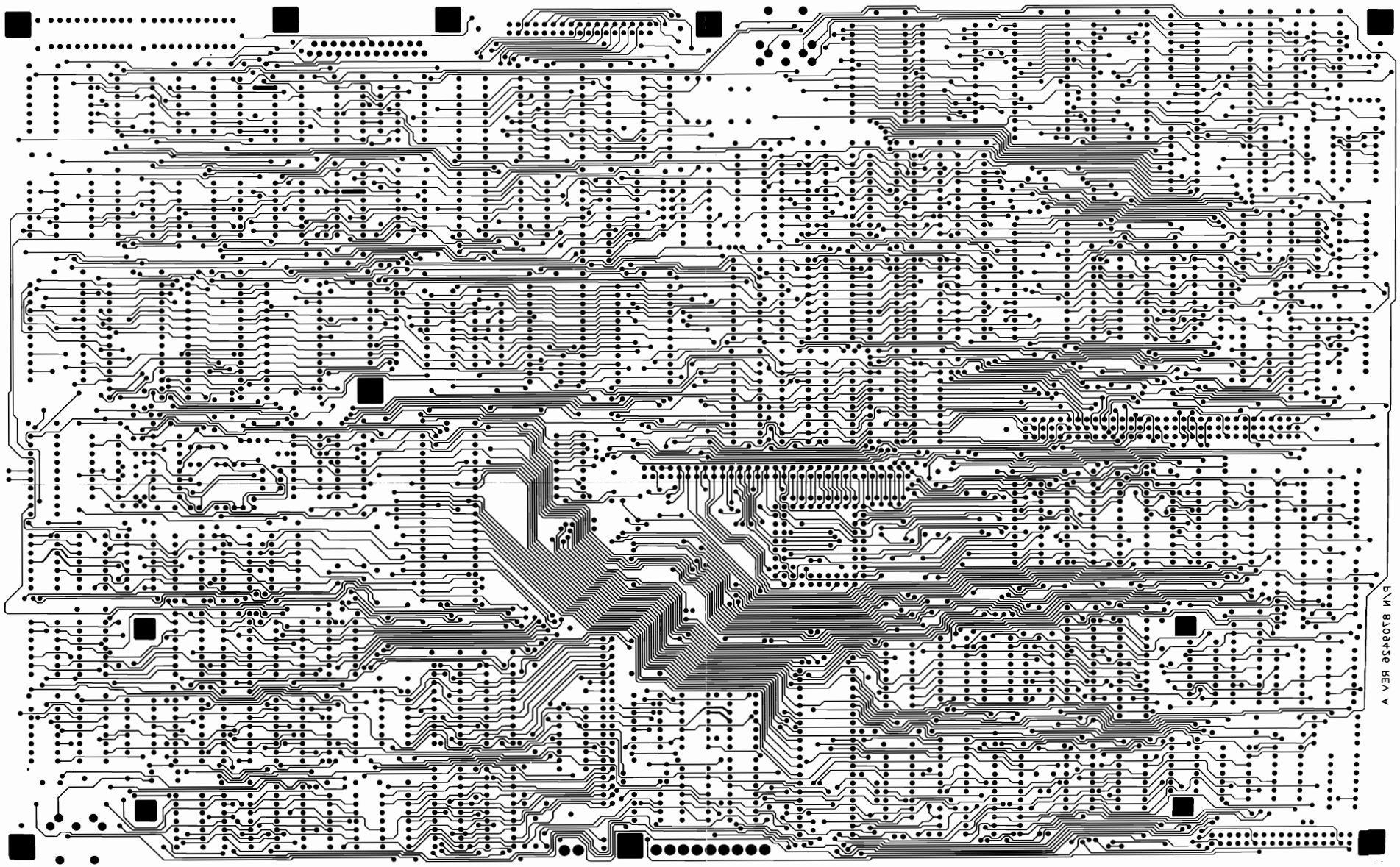
TANDY CORP.
MODEL J-507 MAIN BD.
REF. DWG. NO. 1700245
LAYER 1 ARTWORK REV D



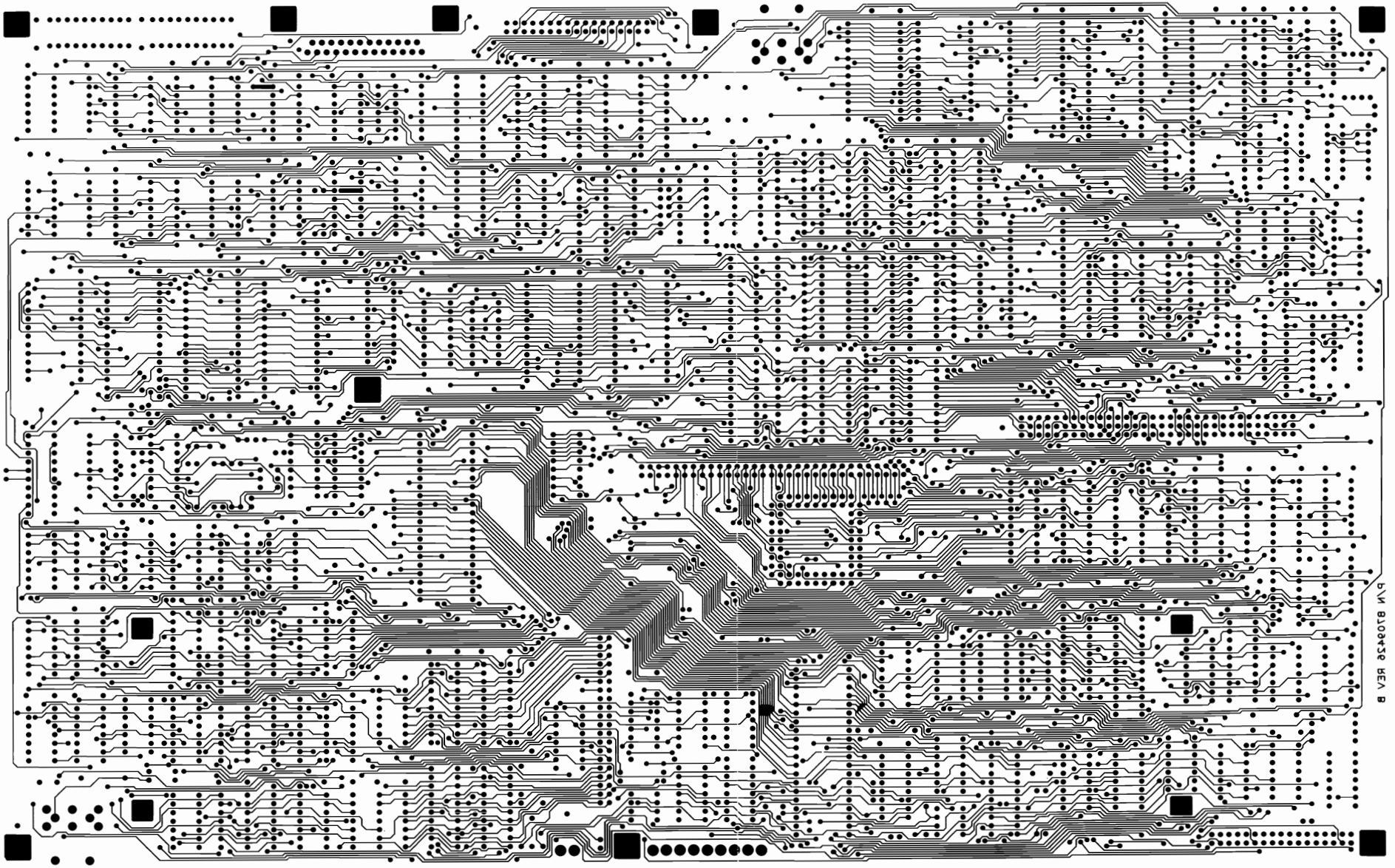
Circuit Trace 1700245, Ground Plane, Component Side
Main Logic PCB Assembly 8898800A



Circuit Trace 1700245, Power Plane, Solder Side
Main Logic PCB Assembly 8898800A



Circuit Trace 1700245, Solder Side
Main Logic PCB Assembly 8898800A



TANDY CORP.
MODEL J-507 MAIN BD.
REF. DWG. NO. 1700245
LAYER 4 ARTWORK REV D

Parts List

Main Logic PCB 8898800A, Model 2000

Item	Sym	Description	Part Number
1	1	Main Logic PCB	8709426
2	1	Socket, 8-Pin DIP (U134)	8509011
3	5	Socket, 20-Pin DIP (U62,68, U82,95,102,103)	8509009
4	5	Socket, 24-Pin DIP (U12,13, U40,47,48)	8509001
5	6	Socket, 28-Pin DIP (U14,15, U41-43, 55)	8509007
6	3	Socket, 40-Pin DIP (U16,75, U121)	8509002
7	1	Socket, 68-Pin Jedec A (U76)	8509017
8	1	Connector, 8-Pin DE8 (J3)	8519203
9	1	Header, 2-Pin (J8)	8519208
10	1	Connector, 9-Pin (J10)	8519191
11	1	Connector, 96-Pin Euro (J5)	8519182
12	1	Connector, Dual 17-Pin (J11)	8519120
13	1	Header, Dual 20-Pin (J6)	8519202
14	1	Connector, 25-Pin (J1)	8519190
15	1	Connector, 5-Pin DIN	8519085
16	1	Connector, 31-Pin (J4)	8519226
17	1	Connector, 34-Pin (J2)	8519198
18	1	Connector, 2-Pin (J9)	8519193
	C1	Capacitor, 470 mfd, 16V Elec Axial	
	C2	Not Used	
	C3	Capacitor, 330 pfd, Dipped Mica 5%	8341337
	C4	Capacitor, 330 pfd, Dipped Mica 5%	8341337
	C5	Capacitor, 330 pfd, Dipped Mica 5%	8341337
	C6	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C7	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C8	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C9	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C10	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C11	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C12	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C13	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C14	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C15	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C16	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C17	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C18	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C19	Capacitor, .1 mfd, 50V Mono Axial	8374104

Parts List

Main Logic PCB 8898800A, Model 2000

Item	Sym	Description	Part Number
	C20	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C21	Capacitor, 68 mfd, 6.3V Tantalum	
	C22	Capacitor, 68 mfd, 6.3V Tantalum	
	C23	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C23a	Capacitor, 82 pfd, 50V Ceramic	
	C24	Capacitor, 68 mfd, 6.3V Tantalum	
	C25	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C26	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C26a	Capacitor,	
	C27	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C28	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C29	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C30	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C31	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C32	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C33	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C34	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C35	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C36	Capacitor, 68 mfd, 6.3V Tantalum	
	C37	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C38	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C39	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C40	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C41	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C42	Capacitor, 220 pfd, Dipped Mica 5%	8341227
	C43	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C44	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C45	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C46	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C47	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C48	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C49	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C50	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C51	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C52	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C53	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C54	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C55	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C56	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C57	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C58	Capacitor, .1 mfd, 50V Mono Axial	8374104

Parts List

Main Logic PCB 8898800A, Model 2000

Item	Sym	Description	Part Number
	C59	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C60	Capacitor, 470 pfd, 50V Cer Disk	
	C61	Capacitor, 470 pfd, 50V Cer Disk	
	C62	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C63	Capacitor, .1 mfd, 50V	8394104
	C64	Capacitor, 2.8-10 pfd, Trimmer	8360310
	C65	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C66	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C67	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C68	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C69	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C70	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C71	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C72	Capacitor, 68 mfd, 6.3V Tantalum	
	C73	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C74	Capacitor, .1 mfd, 50V	8394104
	C75	Capacitor, .1 mfd, 50V	8394104
	C76	Capacitor, .1 mfd, 50V	8394104
	C77	Capacitor, .1 mfd, 50V	8394104
	C78	Capacitor, 5 pfd, 50V Ceramic	8300054
	C79	Capacitor, 10 mfd, 6.3 Tantalum	
	C80	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C81	Capacitor, 10 mfd, 6.3 Tantalum	
	C82	Capacitor, 68 mfd, 6.3V Tantalum	
	C83	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C84	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C85	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C86	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C87	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C88	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C89	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C90	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C91	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C92	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C93	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C94	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C95	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C96	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C97	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C98	Capacitor, .1 mfd, 50V Mono Axial	8374104

Parts List

Main Logic PCB 8898800A, Model 2000

Item	Sym	Description	Part Number
	C99	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C100	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C101	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C102	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C103	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C104	Capacitor, 68 mfd, 6.3V Tantalum	
	C105	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C106	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C107	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C108	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C109	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C110	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C111	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C112	Capacitor, 68 mfd, 6.3V Tantalum	
	C113	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C114	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C115	Capacitor, 33 mfd, 10V Tantalum	
	C116	Capacitor, 180 pfd, Dipped Mica 5%	8341187
	CR1	Diode, 1N4148	8150148
	Q1	Transistor, 2N3906	8100906
	Q2	Transistor, IRFD110, MOSFET	8110110
	R1	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R2	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R3	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R4	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R5	Resistor, 30 ohm, 1/4W 5%	8207030
	R6	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R7	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R8	Resistor, 22 ohm, 1/4W 5%	8207022
	R9	Resistor, 220 ohm, 1/4W 5%	8207122
	R10	Resistor, 1.2 kohm, 1/4W 5%	8207212
	R11	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R12	Resistor, 10 kohm, 1/4W 5%	8207310
	R13	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R14	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R15	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R16	Resistor, 2.2 kohm, 1/4W 5%	8207222

Parts List

Main Logic PCB 8898800, Model 2000

Item	Sym	Description	Part Number
	R17	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R18	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R19	Potentiometer, 5 kohm, Trimpot	
	R20	Resistor, 130 ohm, 1/4W 5%	8207113
	R21	Resistor, 130 ohm, 1/4W 5%	8207113
	R22	Resistor, 1 kohm, 1/4W 5%	8207210
	R23	Resistor, 1 kohm, 1/4W 5%	8207210
	R24	Resistor, 820 ohm, 1/4W 5%	8207182
	R25	Resistor, 200 ohm, 1/4W 5%	8207120
	R26	Resistor, 4.7 kohm, 1/4W 5%	8207247
	R27	Resistor, 100 ohm, 1/4W 5%	8207110
	R28	Resistor, 10 ohm, 1/4W 5%	8207010
	R29	Resistor, 390 ohm, 1/4W 5%	8207139
	R30	Resistor, 10 kohm, 1/4W 5%	8207310
	R31	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R32	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R33	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R34	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R35	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R36	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R37	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R38	Resistor, 270 kohm, 1/4W 5%	8207427
	R39	Resistor, 150 ohm, 1/4W 5%	8207115
	R40	Resistor, 150 ohm, 1/4W 5%	8207115
	R41	Resistor, 150 ohm, 1/4W 5%	8207115
	R42	Resistor, 150 ohm, 1/4W 5%	8207115
	R43	Resistor, 150 ohm, 1/4W 5%	8207115
	R44	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R45	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R46	Resistor, 33 ohm, 1/4W 5%	8207033
	R47	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R48	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R49	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R50	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R51	Resistor, 2.2 kohm, 1/4W 5%	8207222
	R52	Resistor, 150 ohm, 1/4W 5%	8207115
	R53	Resistor, 2.2 kohm, 1/4W 5%	8207222

Parts List

Main Logic PCB 8898800, Model 2000

Item	Sym	Description	Part Number
	RP1	Resistor Pak, 2.2 kohm, 8-Pin SIP	8290039
	RP2	Resistor Pak, 8.2 kohm, 6-Pin SIP	8290036
	RP3	Resistor Pak, 2.2 kohm, 8-Pin SIP	8290039
	RP4	Resistor Pak, 56 ohm DIP 16-Pin	8290034
	RP5	Resistor Pak, 33 ohm DIP 16-Pin	8290044
	U1	IC, 74S00, Quad 2-Input NAND	8010000
	U2	IC, 74LS32, OR Gate	8020032
	U3	IC, 74LS74, Flip Flop	8020074
	U4	IC, 74LS00, NAND Gate	8020000
	U5	IC, MC1488, Driver	8050188
	U6	IC, MC1489, Receiver	8050189
	U7	IC, MC1489, Receiver	8050189
	U8	IC, 74LS245, Transceiver	8020245
	U9	IC, 74LS323, Storage Register	8020323
	U10	IC, 74LS244, Line Driver	8020244
	U11	IC, 74LS244, Line Driver	8020244
	U12	IC, PD4016, 2K x 8 Static RAM	8041116
	U13	IC, PD4016, 2K x 8 Static RAM	8041116
	U14	IC, CRT9021	8040021
	U15	IC, CRT9212	8040212
	U16	IC, CRT9007	8040007
	U17	IC, 74LS244, Line Driver	8020244
	U18	IC, 74S157, Multiplexer	8010157
	U19	IC, 7438, NAND	8000038
	U20	IC, 74LS08, AND Gate	8020008
	U21	IC, 74LS32, OR Gate	8020032
	U22	IC, 74LS125A, Buffer	8020125
	U23	IC, 74LS04, Hex Inverter	8020004
	U24	IC, 74LS123, Multivibrator	8020123
	U25	IC, 74F32, Quad 2-Input OR	8015032
	U26	IC, 74S139, Dual Decoder	8010139
	U27	IC, 74LS125A, Buffer	8020125
	U28	IC, 74F244, Octal Buffer	8015244
	U29	IC, 74LS393, Counter	8020393
	U31	IC, 74LS244, Line Driver	8020244
	U32	IC, 74LS244, Line Driver	8020244
	U33	IC, 74LS244, Line Driver	8020244
	U34	IC, 74F245, Octal Transceiver	8015245
	U35	IC, 74F244, Octal Buffer	8015244
	U36	IC, 74LS374, Flip Flop	8020374
	U37	IC, 74LS378, Hex Flip Flop	8020378

Parts List

Main Logic PCB 8898800, Model 2000

Item	Sym	Description	Part Number
	U38	IC, 74LS38, Buffer	8020038
	U39	IC, 74S04, Hex Inverter	8010004
	U40	IC, 8253-5, Timer	8040253
	U41	IC, 8251A, Interface	8040251
	U42	IC, 8259A2, Interrupt Controller	8040259
	U43	IC, 8259A2, Interrupt Controller	8040259
	U44	IC, 74LS245, Transceiver	8020245
	U45	IC, 74F258, Multiplexer	8015258
	U46	IC, 74F258, Multiplexer	8015258
	U47	IC, 64K Boot ROM, Low	8040035
	U48	IC, 64K Boot ROM, High	8040035
	U49	IC, 74LS273, Flip Flop	8020273
	U50	IC, 74LS245, Transceiver	8020245
	U51	IC, 74LS245, Transceiver	8020245
	U52	IC, 74F245, Octal Transceiver	8015245
	U53	IC, 74F245, Octal Transceiver	8015245
	U54	IC, 74LS245, Transceiver	8020245
	U55	IC, CRT9212	8040212
	U56	IC, 74F245, Octal Transceiver	8015245
	U57	IC, 74LS374, Flip Flop	8020374
	U58	IC, 74LS244, Line Driver	8020244
	U61	IC, 74F161, Binary 4-Bit Counter	8015161
	U62	IC, 82S153, Logic Array	8040153
	U63	IC, 74LS373, Octal Latch	8020373
	U64	IC, 74LS373, Octal Latch	8020373
	U65	IC, 74F245, Octal Transceiver	8015245
	U66	IC, 74F245, Octal Transceiver	8015245
	U67	IC, 74LS138, Decoder	8020138
	U68	IC, 82S153, Logic Array	8040153
	U69	IC, 74S74, Flip Flop	8010074
	U70	IC, 74LS273, Flip Flop	8020273
	U71	IC, 74LS138, Decoder	8020138
	U72	IC, NE564	8040564
	U73	IC, 74LS161A, Shift Register	8020161
	U74	IC, 74F161, Binary 4-Bit Counter	8015161
	U75	IC, 8255A5, Interface	8040255
	U76	IC, 80186	8040186
	U77	IC, 74LS373, Octal Latch	8020373
	U78	IC, 74LS244, Line Driver	8020244
	U79	IC, 74LS273, Flip Flop	8020273
	U80	IC, 74F245, Octal Transceiver	8015245
	U81	IC, 74LS244, Line Driver	8020244

Parts List

Main Logic PCB 8898800, Model 2000

Item	Sym	Description	Part Number
	U82	IC, PAL10L8	8041108
	U83	IC, 74LS125A, Buffer	8020125
	U84	IC, 74LS74, Flip Flop	8020074
	U85	IC, 74LS32, OR Gate	8020032
	U86	IC, 74LS08, AND Gate	8020008
	U87	IC, 74LS38, Buffer8020038	
	U88	IC, 74LS74, Flip Flop	8020074
	U89	IC, 74F04, Hex Inverter	8015004
	U90	IC, 74LS74, Flip Flop	8020074
	U91	IC, 74LS00, NAND Gate	8020000
	U92	IC, 74LS74, Flip Flop	8020074
	U93	IC, 74S260, Dual 5-Input NOR	8010260
	U94	IC, 74LS193, Clock Counter	8020193
	U95	IC, PAL16L8A	8042168
	U96	IC, 74F64, AND/OR Inverter	8015064
	U97	IC, 74F04, Hex Inverter	8015004
	U98	IC, 74LS139, Demultiplexer8020139	
	U99	IC, 74F138,Demultiplexer	8015138
	U100	IC, 74LS161A, Shift Register	8020161
	U101	IC, 74F32, Quad 2-Input OR	8015032
	U102	IC, PAL16L8A	8042168
	U103	IC, PAL16L8A	8042168
	U104	IC, 74LS161A, Shift Register	8020161
	U105	IC, 74LS244, Line Driver	8020244
	U106	IC, 74F08, Quad 2-Input AND	8015008
	U107	IC, 74F32, Quad 2-Input OR	8015032
	U108	IC, 74F00, Quad 2-Input NAND	8015000
	U109	IC, 74F02, Quad 2-Input NOR	8015002
	U111	IC, 74S112, Flip Flop	8010112
	U112	IC, 74F00, Quad 2-Input NAND	8015000
	U113	IC, 74S112, Flip Flop	8010112
	U114	IC, 74F32, Quad 2-Input OR	8015032
	U115	IC, 74F280, Parity Generator	8015280
	U116	IC, 74F373, Octal Latch	8015373
	U117	IC, 74LS244, Line Driver	8020244
	U118	IC, 74LS74, Flip Flop	8020074
	U119	IC, 74LS30, 8-Input NAND	8020030
	U120	IC, 74LS04, Hex Inverter	8020004
	U121	IC, 8272, FDC	8040272

Parts List

Main Logic PCB 8898800, Model 2000

Item	Sym	Description	Part Number
	U122	IC, 74LS04, Hex Inverter	8020004
	U123	IC, 74F08, Quad 2-Input AND	8015008
	U124	IC, 74S112, Flip Flop	8010112
	U125	IC, 74F32, Quad 2-Input OR	8015032
	U126	IC, 74F280, Parity Generator	8015280
	U127	IC, 74F373, Octal Latch	8015373
	U128	IC, 74LS244, Line Driver	8020244
	U129	IC, 75477, Driver	8040477
	U130	IC, 74LS74, Flip Flop	8020074
	U131	IC, 74LS195, Shift Register	8020195
	U132	IC, 74LS123, Multivibrator	8020123
	U133	IC, 74LS02, Quad NOR	8020002
	U134	IC, FDC9216, Data Separator	8040216
	U135	IC, 74LS241, Octal Buffer	8020241
	U136	IC, 74LS32, OR Gate	8020032
	U137	IC, 74LS04, Hex Inverter	8020004
	U138	IC, 7416, Hex Inverter	8000016
	U139	IC, 74LS14, Hex Inverter	8020014
	U140	IC, 7416, Hex Inverter	8000016
	U141	IC, 74LS04, Hex Inverter	8020004
	Y1	Oscillator, 16 MHz	

7.2 Power Supplies

The Model 2000 Microcomputer uses two different power supplies, depending on the configuration of the features incorporated into the unit. The microcomputer which contains two internal floppy disk drives uses a 95W power supply mounted in the Main Unit assembly contained in a metal enclosure. It supplies voltages for the internal systems of the microcomputer.

7.2.1 Main Power Supply #8790056 (95W)

This power supply operates from a 110-120 Vac, 60 Hz input. It may be converted to operate with a 220-240 Vac source if desired. This conversion must be done by a qualified service technician.

The power supply circuit is protected from abnormally high currents by either a 3 amp (for 120 Vac) or 3 amp (for 240 Vac) fuse mounted on the PC board. The power supply is further protected by a circuit which will shut the power supply down if excessively high current (5.1V = 15 amps, +12 or -12V = 8 amps) or low voltage (below 90 Vac for 110-120 volt operation, or 180 Vac for 220-240 Vac operation) is encountered. A "snubber" circuit protects the power supply against excessive voltage spikes.

The AC input is filtered by an EMI (electro-magnetic interference) filter.

The voltage outputs of the main power supply in the Model 2000 are +5.1 volts, +12 volts, and -12 volts. The outputs are filtered and have over-voltage and under-voltage protection circuits.

7.2.1.1 Technical Specifications

Environment:

Temperature:	Operating	0 to 50C (32-122F)
	Storage	-40 to 85C (-40-185F)
Humidity:	Operating	85% RH @ 35C
	Storage	95% RH @ 35C

Input Voltage:
90 to 135 Vac rms/180 to 270 Vac rms, 47 to 63 Hz

Input Surge Current:
70 amps maximum

Efficiency:
70% minimum at full load with 115 Vac rms input

Output Voltages:
V1, +5.1 Vdc
V2, +12 Vdc
V3, -12 Vdc
V4, +12 Vdc

Output Power:
Continuous 95 watts maximum

Output Current:

		Load	
	Output	Minimum	Maximum
Condition 1	V1	3.5 A	13.25 A
	V2	.25 A	2.1 A
	V3	.005 A	.20 A
	V4	0.0 A	.32 A

Output Ripple Voltage:

V1 (5.1 Vdc)	50 mV p-p
V2 (+12 Vdc)	150 mV p-p
V3 (-12 Vdc)	150 mV p-p
V4 (+12 Vdc)	150 mV p-p

Note: Ripple is the composite 100/120 Hz ripple due to the line, plus the high frequency ripple due to the power oscillator. Common mode noise which may be observed due to oscilloscope connections should be ignored.

Output Voltage Regulation:

After initially setting the output voltages, output voltage tolerances under all conditions of rated line, load, and temperature should remain within the following limits:

V1	(+5.1 Vdc)	+/- 3%
V2	(+12 Vdc)	+/- 5%
V3	(-12 Vdc)	+ 8.3%, -25%
V4	(+12 Vdc)	+/- 10%

Over-Current Protection:

V1: Maximum short circuit current is 15 amps.
V2: Maximum short circuit current is 8 amps.
V3: Maximum short circuit current is 8 amps.
V4: Maximum short circuit current is 8 amps.

No damage will result when any output is short circuited continuously with 50 milliohms or less.

Over-Voltage Protection

The +5.1 Vdc circuit is protected with a "crowbar" circuit with a trip range of 5.8 to 6.8 Vdc.

Hold-Up Time at Continuous Max Load:

Nominal Line	16 msec minimum
Low Line	10 msec minimum

7.2.1.2 Troubleshooting The Power Supply

Equipment Required

1. Isolation transformer, 250 VA minimum rating. Dangerously high voltages are present in this power supply. For the safety of the person doing the testing, use an isolation transformer. The 250 VA rating is necessary to keep the AC waveform from being clipped off at the peaks. These power supplies have peak charging capacitors and draw maximum power at the peak of the AC waveform.

2. Variable Transformer (Variac). Use to vary the input voltage. A 10 amp, 1.4 KVA rating is recommended.

3. Voltmeter for measuring DC voltages to 400 Vdc and AC voltages to 150 Vac. Two digital voltmeters are recommended.

4. Oscilloscope with X10 and X100 probes.

5. Ohmmeter

6. Load board with connector. See Figure 1 for a schematic of the load board.

7. 35 Vdc power supply

	Minimum Load	Ohms	Maximum Load	Ohms
+5 Volt	3.5A	1.4	13.5A	0.38
+12 Volt	0.25 A	48	2.1A	5.7
-12 Volt	0.05A	240	0.2A	60

Table 7-6. Load Board Values, 95W Power Supply

Table 1 lists the resistor values required to simulate the minimum load conditions and the maximum load conditions of the 95W Power Supply. The ohms values are measured at the connector and include interconnecting wiring.

The ohms values may be obtained with adjustable resistors or by paralleling several resistors. Be sure the resistors are rated for the current and power they must handle.

The variable resistors must be measured and set when they are hot.

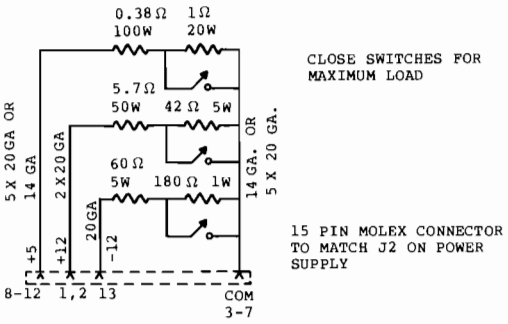


Figure 7-23. Load Box

Figure 7-23 shows recommended resistors and wire sizes for constructing a load box for the 95W Power Supply. The switches can be SPST toggle switches such as Radio Shack's 275-651. All parts can be mounted on an aluminum chassis. Figure 7-24 is a completed load box.

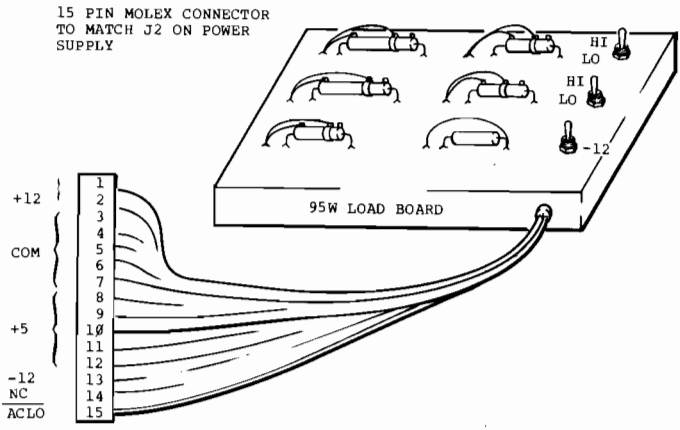


Figure 7-24. Load Box Assembly

Visual Inspection

Remove the power supply from the chassis where it is mounted. Check the power supply for broken, burned, or obviously damaged components. Visually check the fuse. If in doubt, check the fuse with an ohmmeter. Look for overheated or burned areas on the back of the circuit board.

Initial Testing

Connect a +35 volt power source to J3 through two resistors as shown in Figure 7-25. Observe the base of Q15 with the oscilloscope. The waveform should look like Figure 7-26.

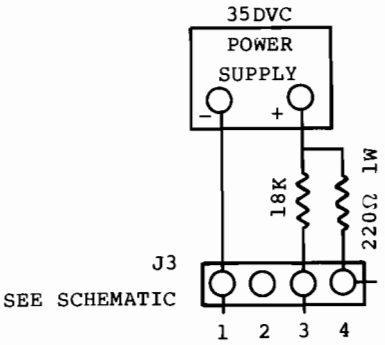


Figure 7-25. Test Circuit

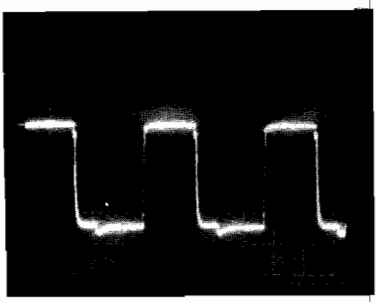
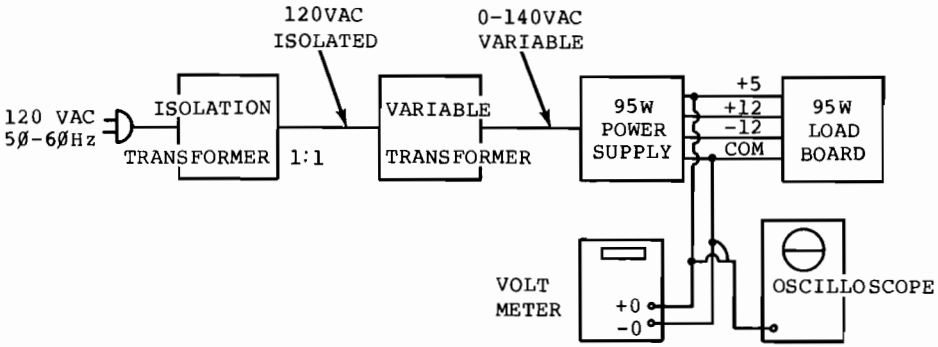


Figure 7-26. Waveform

If it does not, or if no waveform is present, there is a problem with U3 or Q12-15. Do not proceed further until this is repaired. See the No Output section.

Setup Procedure

Set up the test equipment as shown in Figure 7-27. Monitor the AC input voltage and the regulated +5 volt output. Use 50 mV/div. sensitivity and AC coupling on the oscilloscope. Load the 95W Power Supply with its minimum load as specified in Table 7-6. Bring the AC input voltage up slowly with the variable transformer while monitoring the +5 volt output with the oscilloscope and voltmeter. The supply should start with approximately 90 Vac applied and should regulate at +5 Vdc. If the output has reached +5 volts, do a performance test as shown in Paragraph 7.2.1.3.



BE SURE THE INPUT VOLTAGE JUMPER IS CONNECTED FROM E8 TO E9.

Figure 7-27. Test Equipment Setup

No Output

If the power supply does not produce correct output voltages, one or more components have failed. A No Output condition is most likely caused by a shorted or open component in the primary circuitry but may also be caused by a fault in the secondary circuitry.

A. Check the fuse and replace if necessary.

B. Check for shorts and opens in the primary circuit semiconductors. Check the diode bridge BR1, power transistors Q12-15, and catch diode CR11 for shorted junctions. A shorted junction will measure zero ohms in-circuit. Replace any shorted components.

C. Check for shorts and opens in the secondary circuit. Use an ohmmeter to measure from each output to secondary common with the output loads disconnected. Look for shorted rectifiers and capacitors. If the +12 volt output is shorted, also check crowbar SCR Q6.

D. Check the primary DC with the fuse intact. Connect a 35 Vdc power supply to J3 as shown in Figure 3. Start with the variable transformer set to 0 Vac. Monitor the DC voltage from Pin 1 of T1 to primary common. With an input of 95 Vac, there should be about 260 Vdc. If not, check the fuse, rectifier BR1, and thermistors RT1 and RT2.

E. Check Q15 waveforms Look for base drive on the base of Q15 (see Figure 6). The transistor should be switching. Check the collector waveform with a X100 probe (see Figure 7). If base drive is missing, check pin 8 of U3 (see Figure 8). See if U3 has +16 Vdc on pin 10. Check the chip oscillator on pin 5 (see Figure 9).

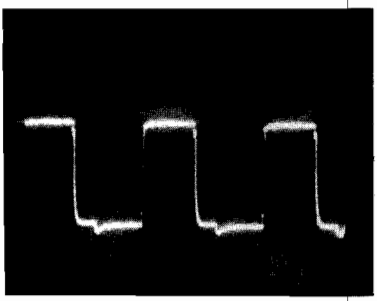


Figure 7-28. Base of Q15

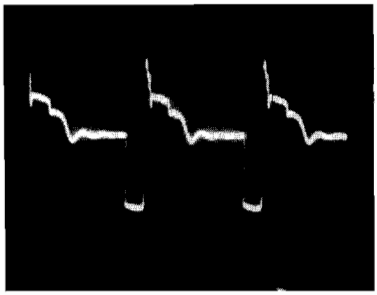


Figure 7-29. Q15 Collector Waveform

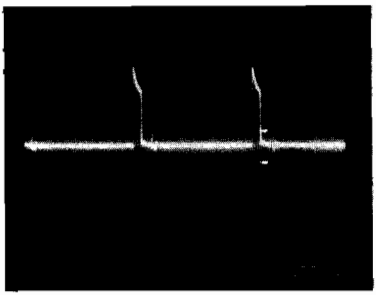


Figure 7-30. Waveform of U3, Pin 8

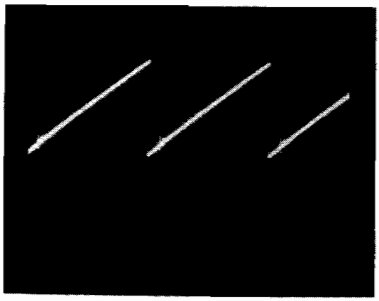


Figure 7-31. Chip Oscillator, Pin 5

Low Outputs

A. All Outputs Are Low. If all outputs are low, check that the voltage selection jumper is in the proper position.

B. +5 Volt Output. The power supply regulates the +5 volt output directly. If the +5V adjustment, R10, is not set correctly, the other outputs will be too high or too low.

7.2.1.3 Performance Test

The following specifications should be met when the power supply is operated under minimum and maximum loads and input voltages.

Output	Min	Max	Ripple(max)
+5.1V	4.95	5.25	50 mV p-p
+12 V	11.4	12.6	150 mV p-p
-12 V	11	15	150 mV p-p

Apply 115 Vac to the line input. Measure the +5.1 V output under full loading. Adjust R10 for a reading between 5.05 and 5.15 volts. Measure the +12.0 volt output under full loading. Adjust R8 for a reading between 11.95 and 12.15 volts.

7.2.1.4 System Description

Basic Principle

A switching power supply circuit employs a high-speed semiconductor switch to control the storage and release of electrical energy in an inductor and provide regulated DC output voltages with a minimum loss of energy in heat-dissipating elements. There are several schemes for achieving this result which differ primarily in the arrangement of the basic circuit elements. These elements include a switch, an inductor, a rectifier, a capacitor and a DC voltage source.

An arrangement well-suited for economical power supplies with rated power outputs under 100 watts is the FLYBACK CONVERTER shown in Figure 7-32. The waveforms in Figure 7-33 are used to describe the operation of the Flyback Converter circuit. For the purpose of this discussion, we will assume that the duration of the "ON" time equals the duration of the "OFF" time.

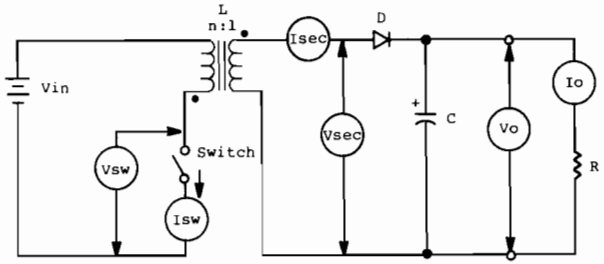


Figure 7-32. Basic Flyback Converter

When the switch is closed (ON) at time ta, Vin is impressed across the primary winding of inductor L and the current Isw increases linearly from zero until the switch opens (OFF) at time tb. Note that Isec is zero while the switch is closed. This is because Vsec is negative with respect to Vo, thus reverse-biasing diode D. Note that Vsw is also zero while the switch is closed.

When the switch opens at time tb, the magnetic field of L instantly collapses and reverses polarity. At this moment, Vsw is equal to Vin plus the voltage across L just before the switch opened (also equal to Vin). Therefore, at the instant the magnetic field reverses polarity, Vsw = 2Vin.

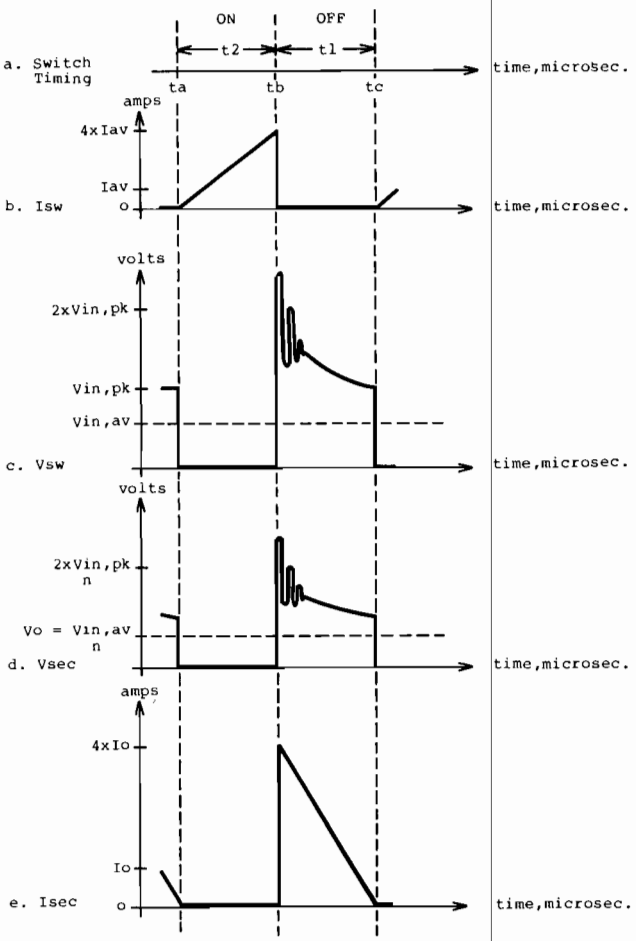


Figure 7-33. Waveforms for Figure 7-32

During the interval when the switch is open (tb to tc), the secondary voltage, Vsec, is a replica of the primary voltage Vsw. Diode D is now forward biased due to the polarity of the inductor windings and because the turns ratio, n, is such that:

$$Vsec \times n > Vo$$

This biasing replenishes the charge in capacitor C that was delivered to the load R during the ta-tb interval. This is the "flyback" interval and is so named because the inductor releases the energy stored in its magnetic field while the switch is OFF.

Several other facts are illustrated by the waveforms of Figure 7-33. First, the voltage Vsw across the switch decays exponentially from 2Vin to Vin during the "OFF" interval. This is because the inductor and the switch timing are adjusted to transfer all of the energy that was stored in the inductor while the switch was ON into the secondary while the switch is OFF. (Observe that Isec DECREASES linearly with time to zero at the end of the "OFF" time period.) This is known as resetting the core. Thus, at time tc when the switch is ready to turn on again, the DC input voltage Vin is again available to charge the inductor. Also at this time, all currents in the inductor are zero.

Second, since we have assumed that Isw increases linearly with time and that the ON and OFF time periods are equal (50% duty cycle), the average current in the primary, Isw (av), is 1/4 the peak current Isw. Also, the average current in the secondary, which is equal to the load current Io, is 1/4 the peak current in the secondary.

Third, the turns ratio is set by the ratio of the average primary voltage (Vsw) over a full cycle at its lowest value to the maximum permissible output voltage, Vo. The lowest Vsw value occurs at low AC line and maximum output load. In practice, the actual turns ratio, the ratio of peak-to-average voltages and currents, and the duty cycle may be adjusted to compensate for circuit losses.

Fourth, notice the ringing or oscillation that appears on the peak portion of Vsw and Vsec. This oscillation occurs at the resonant frequency of the leakage inductance of the inductor L and the parasitic capacitance of the circuit. The parasitic capacitance includes the interwinding capacitance of the inductor and stray capacitance of the switch. If this oscillation is not damped by a suitable means, the peak

voltages may easily exceed the breakdown rating of the switch or the insulation of the inductor.

Block Diagram

The basic circuit illustrated in Figure 7-34 can be divided into three functional blocks: Input DC supply, primary, and secondary. To make use of this model, we need to expand it to provide control for the switch timing and to include sufficient circuitry to satisfy performance and reliability.

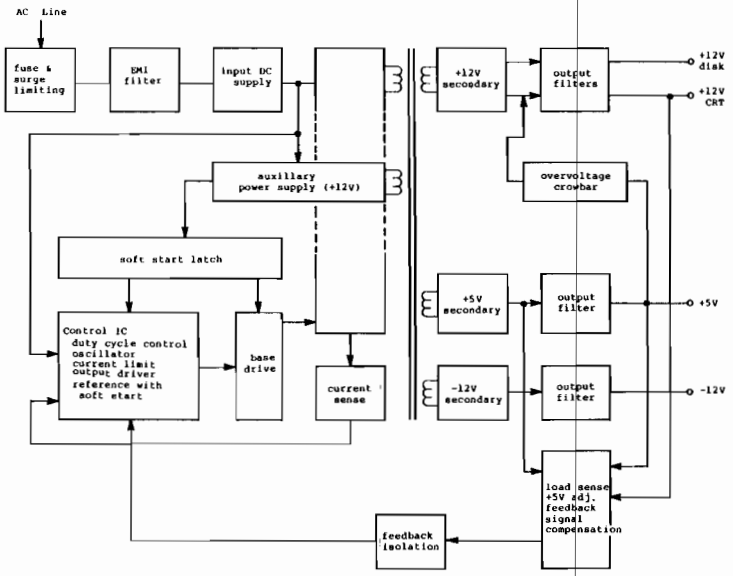


Figure 7-34. Block Diagram.

The other blocks provide additional output voltages, add safety or protective features, reduce circuit noise, and develop signals for use by the control section. The control section continuously operates the bipolar transistor switch and varies the proportion of ON time to OFF time in response

to changes in the AC input line voltage or output load current. This is accomplished by feeding back a signal from the output terminals that instructs the control section to increase or decrease the ON time to compensate for a change in the output voltage.

The DC voltage supply to the control section is controlled by the latch circuit when AC power is first applied to the power supply. A built-in timing circuit allows the input DC supply filter capacitor to become fully charged before power is applied to the control section. After the control section circuit starts and secondary voltages reach their regulated output levels, the auxiliary power supply provides the required DC voltage to operate the control seciton. The latch is reset when the current limit or under-voltage sensors operate, thus removing DC voltage to the Control IC.

There are three secondary or output voltages in addition to the auxiliary supply: +5.1 volt, +12 volt, and -12 volt. The +5.1 and +12 voltages are regulated by the control circuit response to the frequency compensated feedback control signal which comes from the load sense section. Since the load sensing occurs on the secondary side, an optical coupler circuit is necessary to provide safety isolation between the primary side common ground and the secondary side common ground.

All the secondary voltages, including the auxiliary +12 volts, share the same magnetic flux linkage in the transformer core and are controlled by the flyback inductor. Any change in secondary load currents causes a change in the shared magnetic flux. This change in the flux of the inductor sets up an EMF (electromotive force) which causes a flux in opposition to the one which resulted from the change in load current. Thus, the original change tends to be counteracted and the current delivered to the load remains constant.

The output filters reduce the remaining ripple voltage components of the AC line and switching frequencies to levels low enough to prevent interference with the circuits operated by the supply. Switching frequency components conducted through the AC input terminals are suppressed by the EMI filter to avoid interference with other equipment connected to the power line.

The overvoltage crowbar senses an abnormal rise in the +5.1 volt output and short-circuits the voltage line to the common secondary ground, thus tripping the current limiting circuit which finally shuts down the supply.

The surge limiter at the AC line input prevents the input filter capacitor in-rush current surge from exceeding component ratings or unnecessarily tripping external fuses.

7.2.1.5 Theory of Operation
Power Supply Assembly 8790056 (95W Tandy)

PRIMARY CIRCUITS

The input AC is fed through an EMI filter (C33-C36, C41, and T2) before being fed to the rectifier. A bridge rectifier and filter capacitors are connected directly across the AC line to provide the DC input voltage to the power supply. For 115V operation, a jumper from E8 to E9 converts the rectifier to voltage-doubler operation. The power supply fuse, a 3 ampere (120V) or 2 ampere (240V), protects the power supply against abnormally high currents.

Auxiliary Power Supply

The auxiliary power supply (winding 9-10 on T1, half-wave rectifier CR9, and filter C37) supplies power to U3 and the base drive circuitry of Q15. The voltage output is approximately +15 volts but surges to +31 volts during start-up.

Kick-Start Latch

Start-up of the circuit is initiated by the kick-start latch. When power is first applied, C37 starts charging through R42. When the voltage on C37 reaches 31 volts, zener diode CR10 conducts, turning on Q10 which then turns on Q11. With Q11 on, Q10 is held on and the power in C37 is delivered to U3 and the base drive circuitry for Q15. Q15 starts switching and the auxiliary power supply comes on to deliver +15 volts to C37.

Control Section

U2, U3, and Q12-14 make up the control section. U3 has three major functions: (1) an internal voltage reference, (2) a pulse generator, and (3) an error amplifier. The internal reference on pin 12 is +5.0 Vdc. This provides the reference for the comparators and the power for the photo transistor in U2.

The pulse generator frequency is controlled by R37 and C27. The generator output is on pins 8 and 9 and is a square wave that controls Q15.

The comparator inputs on pins 1 and 2 sense the propervoltage regulation by comparing +5 volts on pin 2 to the voltage on pin 1 coming from U2. The other comparator inputs on pins 13 and 14 detect faulty operating conditions. Pin 13 is compared to the +5 volts on pin 14 and the pulse generator will stop if pin 13 falls below +5 volts.

Base Drive

The output transistor U3 forms a Darlington pair with Q14 to provide the necessary drive current through C29 to turn on Q15. Q12 and Q13 are biased on during turn-off to cause Q15 to turn off faster.

Current Limit

Transistors Q8 and Q9 form the current limiting latch. R44 is the current sense resistor. Excess current through Q15 and R44 will cause the voltage across R44 to exceed 0.6 volts, turning on Q9. This then turns on Q8, holding on Q9 and pulling pin 13 of U3 below the +5 Vdc reference on pin 14, causing the oscillator in U3 to stop.

Under-Voltage Lockout

Resistors R24 and R26 form a voltage divider from the input DC to ground. The voltage from the divider goes to pin 13 of U3. If the AC input voltage drops below 90 Vac (180 Vac for 230 V operation), the voltage at pin 13 will drop below the +5 volt reference on pin 14, causing the oscillator to stop.

Snubber

CR11, R45, C38, and C39 provide snubbing to prevent excessive voltage spikes from developing across Q15 during the flyback of T1 when Q15 is biased off.

SECONDARY CIRCUITS

Secondary Outputs

There are three separate secondary output voltages: +5 volts, +12 volts, and -12 volts.

The +5 volts comes from two paralleled windings, each feeding two paralleled rectifiers (CR13-CR14) for improved current handling and heat sinking. A pi-section filter, formed by C6, C10, C11, C12, L2, and C9 filters the +5 volts. R9, C7, R16, and C13 are snubbers to protect the low voltage diodes CR13 and CR14 against transients.

The +12 volts is rectified by CR2 and filtered by a pi-section filter formed by C8, L1, and C42. Transistors Q1 and Q2 and the saturable reactor L3 provide improved 12 volt regulation with varying output loading conditions.

The -12 volts is rectified by CR4 and filtered by a pi-section filter formed by C21, L4, and C20. U5 provides the -12 volt regulation and CR3 and CR12 protect U5 aga|?$@ reverse voltages.

Load Sense And Feedback Development

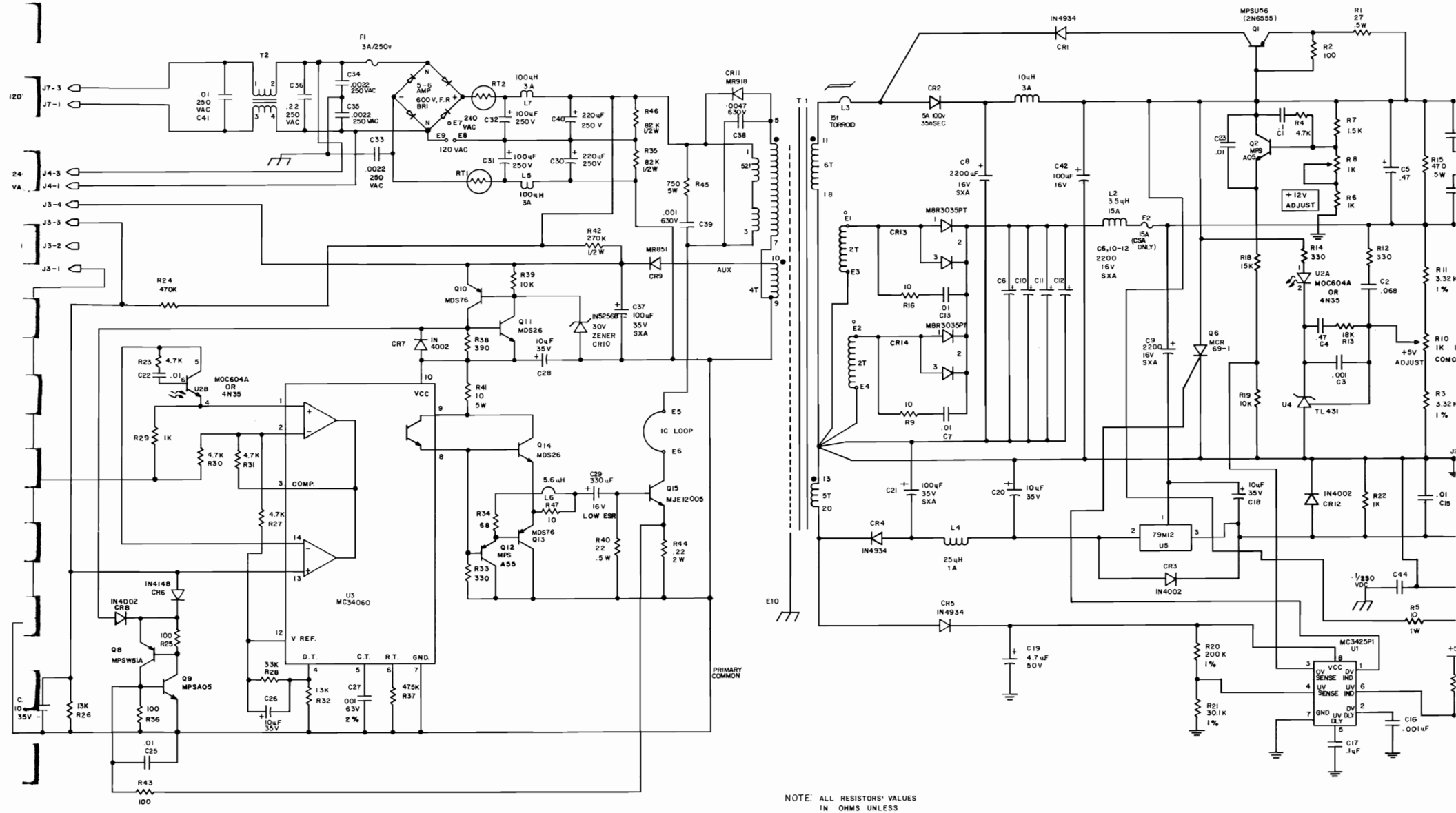
U2 is an opto coupler, containing one light-emitting diode and one phototransistor. The phototransistor controls a comparator in U3 as discussed previously in the Control Section. The LED is controlled by Q3 which senses the +5 volts through a resistive divider that includes R10. this is the regulating feedback path from the secondary circuitry to the primary circuitry.

Overvoltage Crowbar

To prevent the +5 volts from exceeding a safe level, SCR Q6 "crowbars" or short circuits the +5 volt output. This energizes the current limiting circuit in the primary circuitry and the oscillator stops. Q6 is controlled by U11.

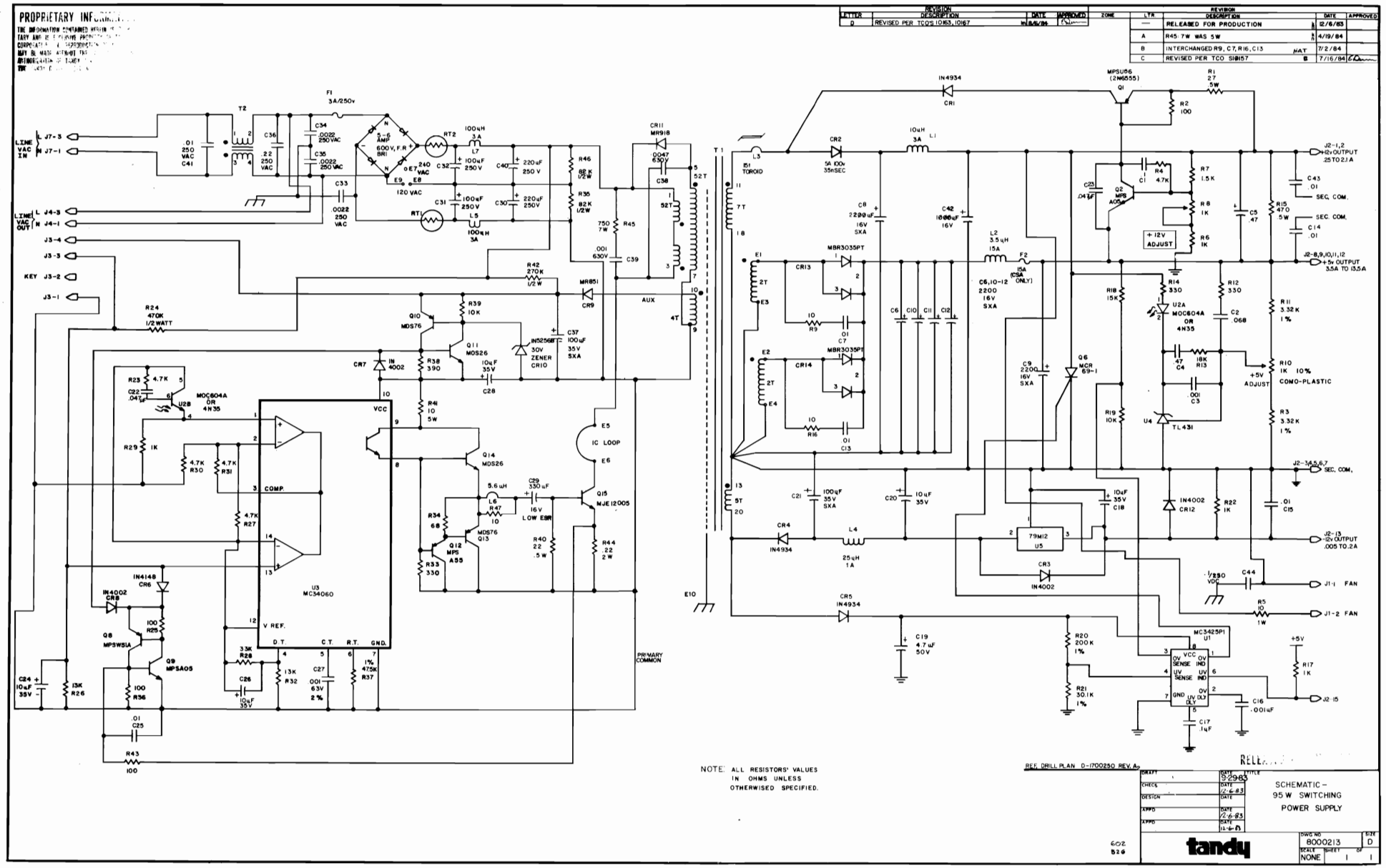
UV And OV Sense

U1 provides UV (under voltage) and OV (over voltage) sense. CR5 conducts during the forward conduction of T1, providing power for U1 and a UV sense signal from R20 and R21. This UV sense provides a TTL UV AC LOW* on pin 6, fully isolated from the primary circuitry. R18 and R19 generate the OV sense signal for U1 pin3 and this controls Q6 via pin 1 of U1.



NOTE: ALL RESISTORS' VALUES IN OHMS UNLESS OTHERWISED SPECIFIED.

Schematic 8000213, 95W Power Supply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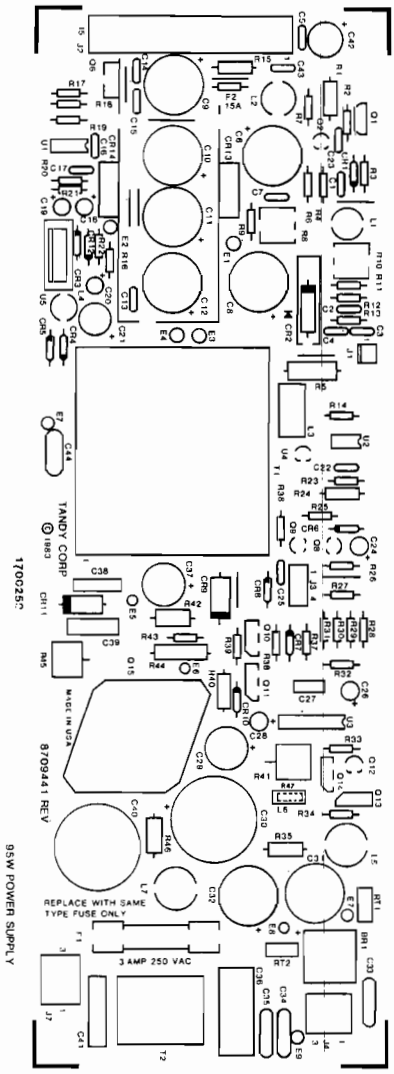
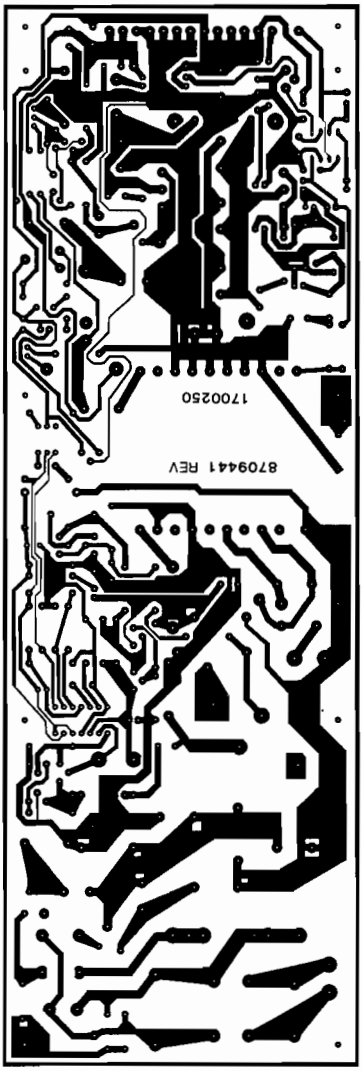
THE
REVISION
LETTER DESCRIPTION DATE APPROVED
D REVISED PER TCO'S 10163, 10167
ZONE
LTR DESCRIPTION DATE APPROVED
— RELEASED FOR PRODUCTION 12/6/83
A R45 7W WAS 5W 4/19/84
B INTERCHANGED R9, C7, R16, C13 7/2/84
C REVISED PER TCO S10157 7/16/84
LINE VAC IN J7-3 J7-1
LINE VAC OUT J4-3 J4-1
J3-4
J3-3
KEY J3-2
J3-1
F1 3A/250v
T2
C41 .01 250 VAC
C34 .0022 250VAC
C36 .22 250 VAC
C35 .0022 250VAC
C33 .0022 250 VAC
BR1 5-6 AMP 600V, F,R
RT2
RT1
L7 100uH 3A
L5 100uH 3A
C32 100uF 250V
C31 100uF 250V
C40 220uF 250 V
C30 220uF 250V
R46 68K 1/2W
R35 82K 1/2W
R45 750 7W
C39 .001 630V
CR11 MR918
C38 .0047 630V
T1
52T
4T
AUX
R42 270K 1/2W
MR851
CR9
R24 47OK 1/2WATT
Q10 MDS76
R39 10K
Q11 MDS26
IN5256B 30V ZENER CR10
C37 100uF 35V SXA
CR7 IN 4002
R38 390
10uF 35V C28
R41 10 5W
U2B MOC604A OR 4N35
R23 4.7K
C22 .047uF
R29 1K
R30 4.7K
R31 4.7K
U3 MC34060
COMP.
R27 4.7K
V REF.
VCC
D.T.
C.T.
R.T.
GND
R28 33K
C26 10uF 35V
R32 13K
C27 .001 63V 2%
R37 1% 475K
C24 10uF 35V
R26 13K
R36 100
C25 .01
R43 100
IN4148 CR6
IN4002 CR8
R25 100
Q8 MPSW51A
Q9 MPSA05
E5 IC LOOP
E6
Q14 MDS26
5.6uH L6
R47 10
C29 330uF 16V LOW ESR
Q15 MJE12005
Q13 MDS76
Q12 MPS A55
R34 68
R33 330
R40 22 .5W
R44 .22 2W
E10
PRIMARY COMMON
NOTE: ALL RESISTORS' VALUES IN OHMS UNLESS OTHERWISED SPECIFIED.
IN4934 CR1
MPSU06 (2N6555) Q1
R1 27 5W
R2 100
L1 10uH 3A
CR2 5A 100v 35nSEC
L3 151 TOROID
11
7T
18
C1 .1
R4 4.7K
C23 .047uF
Q2 MPS A06
R7 1.5K
R8 1K
R6 1K
+12V ADJUST
C5 .47
R15 470 .5W
C43 .01
SEC. COM.
C14 .01
J2-1,2 +12v OUTPUT .25 TO 2.1 A
J2-8,9,10,11,12 +5v OUTPUT 3.5A TO 15.5A
C8 2200uF 16V SXA
C42 1000uF 16V
L2 3.5uH 15A
F2 15A (CSA ONLY)
C6,10-12 2200 16V SXA
MBR3035PT
CR13
CR14
R9 10
R16 10
C7 .01
C13 .01
E1
E2
E3
E4
2T
C9 2200 16V SXA
Q6 MCR 69-1
R18 15K
R19 10K
R14 330
U2A MOC604A OR 4N35
R13 18K
C4 .47
C3 .001
U4 TL431
R12 330
C2 .068
R10 1K 10% COMO-PLASTIC
+5V ADJUST
R11 3.32K 1%
R3 3.32K 1%
J2-3,4,5,6,7 SEC. COM.
C15 .01
C21 100uF 35V SXA
C20 10uF 35V
C18 10uF 35V
IN4002 CR12
R22 1K
79M12 U5
CR3 IN4002
CR4 IN4934
L4 25uH 1A
J2-13 +12v OUTPUT .005 TO 2A
C44
J1-1 FAN
J1-2 FAN
R5 10 1W
CR5 IN4934
C19 4.7uF 50V
MC3425P1 U1
OV SENSE
UV SENSE
GND
VCC
OV IND
UV IND
OV DLY
UV DLY
R20 200K 1%
R21 30.1K 1%
C16 .001uF
C17 1uF
+5V
R17 1K
J2-15
REF. DRILL PLAN 0-1700250 REV. A
DRAFT DATE 9-29-83
CHECK DATE 12-6-83
DESIGN DATE
APPD DATE 12-6-83
APPD DATE 12-6-83
SCHEMATIC - 95 W SWITCHING POWER SUPPLY
tandy
DWG NO 8000213 SIZE D
SCALE NONE SHEET 1 OF 1



Power Supply Component Layout 1700250, PCB Assembly 8790056



Circuit Trace 1700250, 95W Power Supply 8790056

Parts List

Power Supply Assembly 8790056 (95W Tandy)

Item	Sym	Description	Part Number
1	1	Printed Circuit Board	8709441
2	1	Bracket, Heatsink (CR13,14)	8729229
3	1	Heatsink, Diode (CR2)	8549027
4	1	Heatsink, Transistor (Q1)	
6	1	Heatsink, Transistor (Q15)	8549021
7	1	Mount, Transistor (Q15)(with studs)	8549022
8	1	Insulator, TO-3, Cond. Rubber (Q15)	8539043
9	1	Label, DANGER High Voltage	8789889
10	1	Label, CAUTION-Heat Sink	8789888
11	1	Label, Serial Number	8789999
12	2	Screw, #4-40 x 3/8" (Q4,5)	8569002
13	2	Washer, #4 Split Lock (Q4,5)	8589021
14	1	Nut, #4-40 KEPS (Q6)	8579003
15	2	Nut, #6-32 KEPS(Q13, 14)	8579004
16	1	Current Loop, E5 to E6	8433201
17	2	Tab, .110" Faston (E7,8)	8529044
18	1	Jumper, With .110" Faston Connector	8432020
19	1	Socket, IC (U1)	8509011
20	1	Socket, IC (U2)	8509015
21	1	Socket, IC (U3)	8509008
22	2	Clip, Fuse (F1)	8559058
23	2	Nut, #6-32 Zinc Plated (Q15)	8579034
24	1	Screw, #4-40 x 1/4" PPH (Q6)	8569031
25	2	Screw, #6-40 x 1/4" (CR13,14)	8569098
26	1	Washer, Shoulder (Q6)	8589026
	C1	Capacitor, .100 mfd, 63V 10% Metal	8394104
	C2	Capacitor, .068 mfd, 63V 10% Metal	8393684
	C3	Capacitor, .001 mfd, 50V 20% Mtl	8392014
	C4	Capacitor, .47 mfd, 35V 10% Tant	8334474
	C5	Capacitor, .47 mfd, 35V 10% Tant	8334474
	C6	Capacitor, 2200 mfd, 16V 20% Radial	8328221
	C7	Capacitor, .01 mfd, 63V 20% Metal	8393104
	C8	Capacitor, 2200 mfd, 16V 20% Radial	8328221
	C9	Capacitor, 2200 mfd, 16V 20% Radial	8328221
	C10	Capacitor, 2200 mfd, 16V 20% Radial	8328221
	C11	Capacitor, 2200 mfd, 16V 20% Radial	8328221
	C12	Capacitor, 2200 mfd, 16V 20% Radial	8328221
	C13	Capacitor, .01 mfd, 63V 20% Metal	8393104

Parts List

Power Supply Assembly 8790056 (95W Tandy)

Item	Sym	Description	Part Number
	C14	Capacitor, .01 mfd, 63V 20% Metal	8393104
	C15	Capacitor, .01 mfd, 63V 20% Metal	8393104
	C16	Capacitor, .001 mfd, 50V 20% Mtl	8392014
	C17	Capacitor, .100 mfd, 63V 10% Metal	8394104
	C18	Capacitor, 10 mfd, 35V 20% Radial	8326103
	C19	Capacitor, 4.7 mfd, 50V 20% Radial	8325474
	C20	Capacitor, 10 mfd, 35V 20% Radial	8326103
	C21	Capacitor, 100 mfd, 35V 20% Radial	8327103
	C22	Capacitor, .047 mfd, 63V 20% Metal	8393474
	C23	Capacitor, .047 mfd, 63V 20% Metal	8393474
	C24	Capacitor, 10 mfd, 35V 20% Radial	8326103
	C25	Capacitor, .01 mfd, 63V 20% Metal	8393104
	C26	Capacitor, 10 mfd, 35V 20% Radial	8326103
	C27	Capacitor, .001 mfd, 63V 2% Poly	8392104
	C28	Capacitor, 10 mfd, 35V 20% Radial	8326103
	C29	Capacitor, 330 mfd, 16V 20% Radial	8327331
	C30	Capacitor, 220 mfd, 250V 20% Radial	8327227
	C31	Capacitor, 100 mfd, 250V 20% Radial	8327106
	C32	Capacitor, 100 mfd, 250V 20% Radial	8327106
	C33	Capacitor, 2200 pfd, 250V Cer Disk	8302226
	C34	Capacitor, 2200 pfd, 250V Cer Disk	8302226
	C35	Capacitor, 2200 pfd, 250V Cer Disk	8302226
	C36	Capacitor, .22 mfd, 250V 20% Met	8394226
	C37	Capacitor, 100 mfd, 35V 20% Radial	8327103
	C38	Capacitor, .0047 mfd, 630V 10% Poly	8392477
	C39	Capacitor, .001 mfd, 630V 10% Poly	8392017
	C40	Capacitor, 220 mfd, 250V 20% Radial	8327227
	C41	Capacitor, .01 mfd, 250V 20% Met	8393106
	C42	Capacitor, 1000 mfd, 16V 20% Radial	8328102
	C43	Capacitor, .01 mfd, 63V 20% Metal	8393104
	C44	Capacitor, .1 mfd, 250V 20% Metal	8394106
	CR1	Diode, 1N4934	8150934
	CR2	Diode, 5 Amp, 35 nsec	8160050
	CR3	Diode, 1N4001	8150001
	CR4	Diode, 1N4934	8150934
	CR5	Diode, 1N4934	8150934
	CR6	Diode, 1N4148 (Switching)	8150148
	CR7	Diode, 1N4001	8150001
	CR8	Diode, 1N4001	8150001
	CR9	Diode, MR851	8160851
	CR10	Diode, 1N5256B, Zener	8150256

Parts List

Power Supply Assembly 8790056 (95W Tandy)

Item	Sym	Description	Part Number
	J1	Connector, 2 Pin Vertical	8519214
	J2	Connector, 15 PIn	8519194
	J3	Connector, 4 Pin	8519163
	J4	Connector, 3 Pin	8519153
	J5	NA	
	J6	NA	
	J7	Connector, 3 Pin	8519153
	L1	Inductor, 10 uH, 3A 10%	8419007
	L2	Inductor, 3.5 uH, 15A 10%	8419032
	L3	Inductor, Toroid	8419036
	L4	Inductor, 25 uH, 1A 10%	8419034
	L5	Inductor, 100 uH, 3A 10%	8419009
	L6	Coil, 5.6 uH, 10%	8419037
	L7	Inductor, 100 uH, 3A 10%	8419009
	Q1	Transistor, 2N6555, PNP, 1A 80V	8100555
		Transistor, MPS-U56, PNP, .6A 40V	8100056
	Q2	Transistor, MPSA05, NPN, 40V	8110005
	Q3	NA	
	Q4	NA	
	Q5	NA	
	Q6	SCR, MCR69-1, 25A 50PIV	8140691
	Q7	IC, 79M12, Voltage Regulator	8050912
	Q8	Transistor, MPSW51A, PNP, 1A 40V	8101051
	Q9	Transistor, MPSA05, NPN, 40V	8110005
	Q10	Transistor, MDS76, PNP, 3A 40V	8100076
	Q11	Transistor, MDS26, NPN, 3A 40V	8100026
	Q12	Transistor, MPSA55, PNP, .6A 40V	8100055
	Q13	Transistor, MDS76, PNP, 3A 40V	8100076
	Q14	Transistor, MDS26, NPN, 3A 40V	8100026
	Q15	Transistor, MJE12005, NPN, 8A 1500V	8111005
	R1	Resistor, 27 ohm, 1/2W 5%, CF	8217027
	R2	Resistor, 100 ohm, 1/4W 5%, CF	8207110
	R3	Resistor, 3.32 kohm, 1/4W 1%, MF	8200232
	R4	Resistor, 4.7 kohm, 1/4W 5%, CF	8207247
	R5	Resistor, 10 ohm, 1W 5%, CF	8247616
	R6	Resistor, 1 kohm, 1/4W 5%, CF	8207210
	R7	Resistor, 1.5 kohm, 1/4W 5%, CF	8207215
	R8	Potentiometer, 1 kohm, 20%	8279211
	R9	Resistor, 10 ohm, 1/4W 5%, CF	8207010

Parts List

Power Supply Assembly 8790056 (95W Tandy)

Item	Sym	Description	Part Number
	R10	Potentiometer, 1 kohm, 20%	8279211
	R11	Resistor, 3.32 kohm, 1/4W 1%, MF	8200232
	R12	Resistor, 330 ohm, 1/4W 5%, CF	8207133
	R13	Resistor, 18 kohm, 1/4W 5%, CF	8207318
	R14	Resistor, 330 ohm, 1/4W 5%, CF	8207133
	R15	Resistor, 470 ohm, 1/2W 5%, CF	8217147
	R16	Resistor, 10 ohm, 1/4W 5%, CF	8207010
	R17	Resistor, 1 kohm, 1/4W 5%, CF	8207210
	R18	Resistor, 15 kohm, 1/4W 5%, CF	8207315
	R19	Resistor, 10 kohm, 1/4W 5%, CF	8207310
	R20	Resistor, 200 kohm, 1/4W 1%, MF	8200420
	R21	Resistor, 30.1 kohm, 1/4W 1%, MF	8200330
	R22	Resistor, 1 kohm, 1/4W 5%, CF	8207210
	R23	Resistor, 4.7 kohm, 1/4W 5%, CF	8207247
	R24	Resistor, 470 kohm, 1/2W 5%, CF	8217447
	R25	Resistor, 100 ohm, 1/4W 5% CF	8207110
	R26	Resistor, 13 kohm, 1/4W 5%, CF	8207313
	R27	Resistor, 4.7 kohm, 1/4W 5%, CF	8207247
	R28	Resistor, 33 kohm, 1/4W 5%, CF	8207333
	R29	Resistor, 1 kohm, 1/4W 5%, CF	8207210
	R30	Resistor, 4.7 kohm, 1/4W 5%, CF	8207247
	R31	Resistor, 4.7 kohm, 1/4W 5%, CF	8207247
	R32	Resistor, 13 kohm, 1/4W 5%, CF	8207313
	R33	Resistor, 330 ohm, 1/4W 5%, CF	8207133
	R34	Resistor, 68 ohm, 1/4W 5%, CF	8207068
	R35	Resistor, 82 kohm, 1/2W 5%, CF	8217382
	R36	Resistor, 100 ohm, 1/4W 5% CF	8207110
	R37	Resistor, 47.5 kohm, 1/4W 1%, MF	8200347
	R38	Resistor, 390 ohm, 1/4W 5% CF	8207139
	R39	Resistor, 10 kohm, 1/4W 5%, CF	8207310
	R40	Resistor, 22 ohm, 1/2W 5%, CF	8217022
	R41	Resistor, 10 ohm, 5W 5%, WW	8248010
	R42	Resistor, 270 kohm, 1/2W 5%, CF	8217427
	R43	Resistor, 100 ohm, 1/4W 5%, CF	8207110
	R44	Resistor, .22 ohm, 2W 5%, MOF	8248022
	R45	Resistor, 750 ohm, 7W 5%, WW	8248175
	R46	Resistor, 82 kohm, 1/2W 5%, CF	8217382
	R47	Resistor, 10 ohm, 1/4W 5%, CF	8207010
	RT1	Thermistor, 10 ohm @ 25C, Coated	8298010
	RT2	Thermistor, 10 ohm @ 25C, Coated	8298010

Parts List

Power Supply Assembly 8790056 (95W Tandy)

Item	Sym	Description	Part Number
	T1	Transformer, Power, 95W Flyback	8790057
	T2	Choke, Common Mode, 1.24 mH/Side	8790058
	U1	IC, MC3425P, Voltage Protector	8050425
	U2	IC, 4N35, Optoisolator	8170035
	U3	IC, MC34060, Switching Regulator	8060060
	U4	IC, TL431, Positive Shunt Regulator	8060428

7.2.2 Auxiliary Power Supply #8790025 (38W, Hard Disk Drive Only, Astec AA11330)

When the microcomputer is equipped with a built-in hard disk drive, an additional 38W power supply is required to supply voltage to the hard disk drive only. This supply delivers approximately +15 volts in normal operation, but surges to +31 volts durin@ start-up. It is contained in the same housing as the @5W power supply in the Main Unit of the computer.

7.2.2.1 Troubleshooting the Power Supply

Equipment for Test Set Up

1. Isolation Transformer (Minimum of 500 VA rating)

CAUTION

Dangerously high voltages are present in this power supply. For the safety of the individual doing the testing, please use an isolation transformer. The 500 VA rating is needed to keep the AC waveform from being clipped off at the peaks. These power supplies have peak charging capacitors and draw full power at the peak of the AC waveform.

2. 0-280 Variable Transformer (Variac)
   Used to vary input voltage. Recommend 10 Amp, 1.4 KVA rating minimum.

3. Voltmeter
   Needed to measure DC voltages to 50 VDC and AC voltages to 400 Vac. Recommend two digital multimeters.

4. Oscilloscope
   Need X10 probe.

5. Load Board with Connectors
   See Table 7-7 for values of loads required. The entries on the table for Safe Load Power is the minimum power ratings for the load resistors used.

6. Ohmmeter

7. Wattmeter

Setup Procedure

Set up as shown in Figure 7-35. You will want to monitor the input voltage and the output voltage of the regulated bus, which is the +5 Volt output with DVMs. Also monitor the +5 Volt output with the oscilloscope using 50 mv/division sensitivity. The DVM monitoring the +5 Volt output can also be used to check the other outputs. See text under NO OUTPUT for test points within power supply.

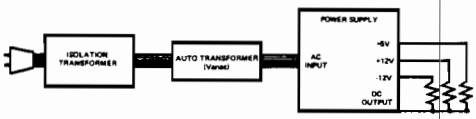


Figure 7-35. Test Setup

Visual Inspection

Check power supply for any broken, burned, or obviously damaged components. Visually check fuse. If there is any question, check with an ohmmeter.

OUTPUT	MIN LOAD	LOAD R	SAFE LOAD POWER	MAX LOAD	LOAD R	SAFE LOAD POWER
+5	0.45A	11.11 ohm	5W	2.5A	2 ohm	25W
+12	0.3A	0.40 ohm	8W	2.02A	24.24 ohm	50W
-12	0	0	0	0	120 ohm	2W

Table 7-7. Load Board Values

Start-Up

First note the position of the input voltage select wire. This wire can be found at the end of the PCB opposite the input/output connectors. Make sure that the jumper wire is in the proper voltage location.

Load the power supply with minimum load as specified in Table 7-7. Bring power up slowly with the variable transformer while monitoring the +5 Volt output with the scope and DVM and the input with a DVM and wattmeter. If the wattmeter shows significant power with low AC power being applied, shut down and refer to section following on NO OUTPUT. The supply should start with approximately 80-120 Vac applied and should regulate when 95 Vac is applied. If the output has reached +5 volts, do a performance test as shown in PERFORMANCE TEST which follows.

NO OUTPUT

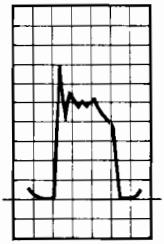
1. Check Fuse. If the fuse is blown, replace it but do not apply power until the cause of failure is found.

2. Preliminary Check On Major Primary Components. Check thermistor (R1), diode bridge (DB1), power transistor (Q2), and catch diode (D3), turn-off transistor (Q1), emitter resistor (R10), and diode (D1) for shorted junctions. If any component is found shorted, replace it.

3. Preliminary Check On Major Secondary Components. Using an ohmmeter from output common to each output (with output loads disconnected), check for shorted rectifiers or capacitors. If +12 volt output is shorted, also check crowbar SCR (SCR1) and zener (Z1).

4. Check For B+. Set up power supply and attach X10 scope probe ground to end of R11 closest to input capacitors. Slowly turn up power and check for B+ on the (+) terminal of the diode bridge (DB1). With the input at 95 Vac, this point should be 120-140 Vdc. If this is not measured, check the fuse, thermister (R1), DB1, R2, D3, and input capacitors C6 and C7.

5. Check Q2 Waveforms. Using X10 probe on the case of T03 package of Q2, check the collector waveform. The transistor should be switching, with the correct waveform shown in Figure 7-36. If this is not present, check for a shorted junction on Q2.



50 V/DIV
5 µsec/DIV

Input – 120VAC
Loads – +5 @ 2A
+12 @ 1A
-12 @ 0.1A

Figure 7-36. Q2 Collector Waveform

If OK, check the base waveform as shown in Figure 7-37. The base of Q2 is the uppermost of the two center leads on the back of Q2 heat sink. If this waveform is not present, check L3, Q1, and D1, secondary components Q3, D11, D12, D5, and L4. If any of the semiconductors is found shorted or if an inductor is open, replace it.

1.0 V/DIV
5 µsec/DIV

Input and Loads
same as above.

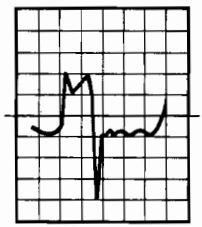


Figure 7-37. Q2 Base Waveform

Performance Test

Each of the test conditions noted below should be set up and results noted to be within the limits specified.

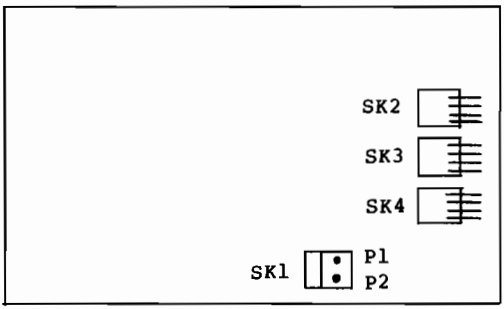
Test	Input	+5 Load	+12 Load	-12 Load
1	95VAC	Max	Max	Max
2	128VAC	Max	Max	Max
3	120VAC	Max	Min	Min
4	128VAC	Min	Min	Min
5	95VAC	Min	Min	Min

VOLTAGE AND RIPPLE SPECIFICATION

OUTPUT	MIN	MAX	NO LOAD	RIPPLE
+5	4.75V	5.25V		50mV P-P
+12	11.40V	12.60V		150mV P-P
-12	11.00V	15.00V		150mV P-P

* Applies to resistive load only. Not under system operating conditions.

Table 7-8. Performance Tables

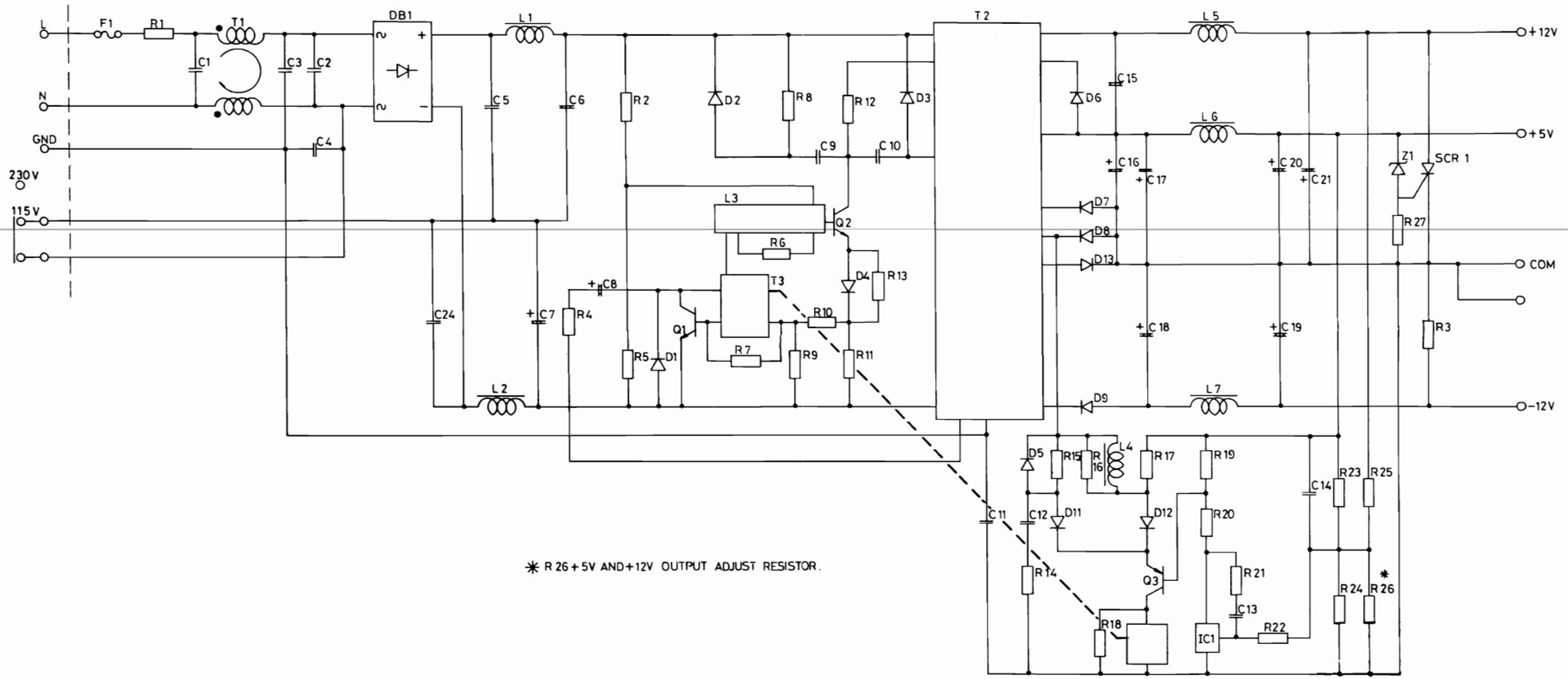


For SK1
P1 - Neutral
P2 - Line

For SK 2,3,4
P1 - -12V 0.1A Max.
P2 - +12V 2.02A Max.
P3 - Common
P4 - +5V 2.5A Max.

Figure 7-38. Power Pin Assignments

R	R1 R4 R2 R5 R6—R13 R14—R18 R19—R27 R3
C	C1 C2,3,4 C24 C5 C6,7,8 C9 C10 C11 C12 C13—C21
L/T	T1 L2 L1 T3 L3 T2 L4—L7
Q/D	D1 Q1 D2 Q2 D4 D3 D5—D9 D11—D13 Q3
MISC	F1 DB1 IC1 Z1 SCR 1



✱ R 26 + 5V AND +12V OUTPUT ADJUST RESISTOR.

Schematic, Power Supply 8790025 (Astec AA11330)

Parts List

Power Supply 8790025 38W (Astec AA11330)

Item	Sym	Description	Part Number
C1		Capacitor, .01 mfd, 250V 20%	068-10300010
C2		Capacitor, .1 mfd, 250V 20%	068-10400010
C3		Capacitor, 4700 pfd, 400V 20% Cer	055-47220001
C4		Capacitor, 4700 pfd, 400V 20% Cer	055-47220001
C5		Capacitor, .22 mfd, 250V 20% Poly	058-22400130
C6		Capacitor, 100 mfd, 250V 20% Elec	057-10120170
C7		Capacitor, 100 mfd, 250V 20% Elec	057-10120170
C8		Capacitor, 220 mfd,10V +50/-10 Elec	057-22120080
C9		Capacitor, 470 pfd, 2KV 10%, Cer	055-47154426
C10		Capacitor, .01 mfd, 1KV 20%, Cer	055-10368925
C11		Capacitor, .01 mfd, 1KV 20%, Cer	055-10368925
C12		Capacitor, .22 mfd, 100V 20% Poly	058-22400160
C13		Capacitor, .022 mfd, 50V 20% Poly	058-22300090
C14		Capacitor, .22 mfd, 100V 20% Poly	058-22400160
C15		Capacitor, 1000 mfd, 25V Elec	057-10220040
C16		Capacitor, 1000 mfd, 25V Elec	057-10220040
C17		Capacitor, 1000 mfd, 25V Elec	057-10220040
C18		Capacitor, 330 mfd, 16V Elec	057-33120120
C19		Capacitor, 330 mfd, 16V Elec	057-33120120
C20		Capacitor, 470 mfd, 25V Elec	057-47120110
C21		Capacitor, 2200 mfd, 16V Elec	057-22220020
C22		Not Used	
C23		Not Used	
C24		Capacitor, .22 mfd, 250V 20%	058-22400130
D1		Rectifier, RGP10A	226-10400050
D2		Rectifier, RGP10J	226-10400060
D3		Rectifier, RGP10M	226-10400100
D4		Rectifier, 1N4001GP	226-10400080
D5		Silicon Diode, 1N4606	212-10700210
D6		Rectifier Assembly	853-00200190
D7		Rectifier Assembly	853-00200190
D8		Rectifier Assembly	853-00200190
D9		Rectifier, RGP10B	226-10400070
D10		Not Used	
D11		Silicon Diode, 1N4606	212-10700210
D12		Silicon Diode, 1N4606	212-10700210
D13		Rectifier, 1N4001GP	226-10400080
DB1		Bridge Rectifier, KBP10	226-30500010

Parts List

Power Supply 8790025 38W (Astec AA11330)

Item	Sym	Description	Part Number
IC1		IC, TL431CLP Regulator	211-10800100
L1		Filter Choke Coil Assembly	852-20100140
L2		Filter Choke Coil Assembly	852-20100140
L3		Base Choke	328-00100030
L4		Choke, 1.5 mH	328-00100010
L5		Filter Choke Coil Assembly	852-20100180
L6		Filter Choke Coil Assembly	852-20100180
L7		Choke Coil	328-00100060
Q1		Transistor, SD467, NPN	209-11700460
Q2		Transistor, Power	853-00400050
Q3		Transistor, SD561, PNP	210-11700350
R1		Thermistor, 4 ohm, 10%	258-40970015
R2		Resistor, 330 kohm, 1/2W 5%	240-33406033
R3		Resistor, 220 ohm, 1W 5%, Metal Ox	248-22106052
R4		Resistor, 33 ohm, 2W 5% Metal Ox	248-33006063
R5		Resistor, 1 kohm, 1/4W 5%	240-10206022
R6		Resistor, 27 ohm, 1/4W 5%	240-27006022
R7		Resistor, 68 ohm, 1/4W 5%	240-68006022
R8		Resistor, 120 ohm, 1W 5% Metal Ox	248-12106052
R9		Resistor, 10 ohm, 1/4W 5%	240-10006022
R10		Resistor, 10 ohm, 1/4W 5%	240-10006022
R11		Resistor, .75 ohm, 1W 5% Metal Flm	247-07586054
R12		Resistor, 1 ohm, 1W 5% Metal Film	247-10086054
R13		Resistor, 5.6 ohm, 1/4W 5%	240-56906022
R14		Resistor, 68 ohm, 1/4W 5%	240-68006022
R15		Resistor, 270 ohm, 1/2W 5%	240-27106033
R16		Resistor, 270 ohm, 1/2W 5%	240-27106033
R17		Resistor, 8.2 ohm, 1/4W 5%	240-82906022
R18		Resistor, 560 ohm, 1/4W 5%	240-56106022
R19		Resistor, 56 ohm, 1/4W 5%	240-56006022
R20		Resistor, 56 ohm, 1/4W 5%	240-56006022
R21		Resistor, 12 kohm, 1/4W 5%	240-12306022
R22		Resistor, 470 ohm, 1/4W 5%	240-47106022
R23		Resistor, 4.7 kohm, 1/4W 2%	247-47015022
R24		Resistor, 68 kohm, 1/4W 5%	240-68306022
R25		Resistor, 22 kohm, 1/4W 2%	247-22025022
R26		Resistor, 2.7 kohm, 1/4W 2%	247-27015022
R27		Resistor, 12 ohm, 1/4W 5%	240-12006022

Parts List

Power Supply 8790025 38W (Astec AA11330)

Item	Sym	Description	Part Number
	SCR1	Silicon Controlled Rectifier, C122F	227-13000010
	T1	Transformer, Common Mode	852-20200950
	T2	Transformer, Power	851-10200940
	T3	Transformer, Control	852-10200680
	Z1	Zener Diode, 5.6V, 1W 5%	222-56086002

7.3 Disk Drives

The Model 2000 Computer may be equipped with either two 5-1/4" Floppy Diskette Drives (Model 26-5103) or one 5-1/4" Floppy Diskette and one Hard Disk Drive (Model 26-5104). All drives are mounted in the Main Unit. The associated 38W power supply required for the Hard Disk Drive version is also integrally mounted to the main power supply inside the Main Unit also. The Hard Disk Controller PCB is mounted in the Card Cage assembly at the rear of the Main Unit in the upper-most slot of the card cage. Its power is supplied from the motherboard of the Main Unit.

7.3.1 Floppy Diskette Drives (Mitsubishi M4853)

The Model 26-5103 contains two floppy disk drives. They are accessible from the front of the Main Unit. Removal for replacement or repair is accomplished according to instructions given in Paragraph 3.1.2. The service manual for this type drive is included at the rear of the Model 2000 Service Manual.

7.3.2 Hard Disk Drive (Tandon TM502)

The Model 26-5104 contains one floppy disk drive and one hard disk drive. The floppy disk drive is mounted in the lower position accessible from the front of the Main Unit and the hard disk drive is mounted internally to the Main Unit. It is accessible for service or repair as noted in Paragraph 3.1.2 also. Service information is contained in the service manual located at the rear of the Model 2000 Service Manual. The Hard Disk Drive is a 10 megabyte (formatted) Tandon TM502. It has two 5-1/4" platters, each of which have two read/write surfaces. Each surface has its own dedicated read/write head attached to a common stepper arm mechanism and 306 cylinders which gives a total of 1224 tracks for the drive.

7.3.3 Hard Disk Controller PCB 8898807

The Hard Disk Controller (HDC) PCB assembly is located in the card cage assembly of the Main Unit and accessible from the rear of the Main Unit. It resides in the upper-most slot of the four positions available in the card cage. It is interconnected to the Hard Disk Drive assembly by a cable assembly connected to the rear of the card. It is a 5" x 10" 2-sided board which is mounted to a custom chassis pan

which makes installation and removal of the board simple. The HDC is designed to provide all data and control signals for one internal and one external 5-1/4" Winchester technology drive.

The HDC is connected to the Model 2000 motherboard via a 96 position Euro-type connector (J5). Eight data lines are passed through an AMD 8304 (U34) non-inverting transceiver. The lower eight address lines (A0 - A7) are driven onto the HDC by a 74LS244 (U33). Other host control input and output signals are buffered by another 74LS244 (U32).

7.3.3.1 Port Decoding

The Model 2000 HDC is I/O mapped to use nine 8-bit ports from 0270H to 027EH and also 026CH, with only even port locations used. The ports are in the larger range of addresses assigned to the signal PCS4*. When PCS4* is active, it indicates an I/O to a port in the range from 0200H to 027FH. PCS4* is qualified with address line A0 to produce the signal P4SEL*, which indicated an even port address in this range. This is further qualified with A4, A5, and A6 to produce DCRCS*, which indicates one of eight HDC registers between 0270H and 027EH is being accessed. A 74S138 (U21) is used to decode an access of port 026CH to trigger a software reset one-shot. The following table shows the HDC ports and their addresses.

Port Address	Register Assigned
026CH	Software Reset
0270H	Data Register
0272H	Error/Write Precomp
0274H	Sector Count
0276H	Sector Number
0278H	Cylinder LSB
027AH	Cylinder MSB (Bits D0 and D1)
027CH	SDH
027EH	Status/Command

7.3.3.2 Drive Control Logic

The heart of the HDC consists of the WD1010 (U18) and the WD1100-11 (U12). The WD1010 is an MOS/LSI device which performs the functions of a Winchester Disk Controller/Formatter. The WD1010 has an 8-bit bidirectional data bus through which it communicates with the bus

transceiver. Selection of the eight internal registers is accomplished through the use of three address lines (A1, A2, and A3), the signal DCRCS*, and either RE* or WE*. RE* and WE* are the signals RD*IB and WR*IB after passing through an LS367 which is enabled by the signal CSI*. When CSI* is inactive, the outputs of the LS367 are tri-stated, allowing the WD1010 to output the signals RE* and WE* to the WD1100-11 and the sector buffer. When the WD1010 wishes to do this, it activates the output BCS* (U18-1) which disables CSI* and produces the signal DISHDB. DISHDB is the inverted BCS* and it is used to disable the bus data transceiver U34. A read of the HDC status register at this time will give a busy indication and no access to the HDC should be attempted until the busy condition no longer exists.

The WD1100-11 is essentially a gate array device which performs several important drive control functions. First, it provides the drive and head select control output signals to the drive interface. Also, it contains two internal one-shots, one of which is used to shape the incoming drive data to a specified pulse width and the other to control the pulse width of the signal DRUN which tells the WD1010 to begin searching for a sector ID field. Finally, the WD1100-11 is used as a sector buffer manager controlling the data flow between the WD1010 and the host system.

The sector buffer (U6) is a 2K x 8-bit static RAM with an access time of 150 nsec or faster. Data from the drive is loaded into it by the WD1010 and WD1100-11 for the host to read and data is loaded into it by the host for the WD1010 to use in formatting or writing to the drive.

The WD1010 and WD1100-11 provide a drive interface compatible with Seagate ST506-type drives. The data and control signals for the internal primary drive are passed to connector J4. The data for the external secondary drive is found on J2 and the control cable for the external drive is connected to J1. Having separate control signal drivers for both drives allows both drives to be terminated at the drive instead of terminating only the last logical drive in a daisy-chain type connection.

7.3.3.3 Data Recovery

System Clock

The fundamental clock is provided by Y1, a 20 MHz crystal oscillator. This is divided to a 10 MHz clock called 2XDR

by one-half of U31. 2XDR is again divided by 2 in U16 to produce the signal WCLK, a 5 MHz square wave which provides the internal timing for the WD1010.

Phase Comparator

The phase comparator circuitry is comprised of a PAL16RA (U16), a 60-nsec delay line (U9), and three D-type flip-flops (U26 and one-half of U25).

When data is being inspected from the drive, its phase relationship with respect to the VCO clock must be determined. The function of this circuitry is to provide windows during which the leading edge of the incoming data bit is compared to the leading edge of the VCO output. The windows are approximately 50 nsec in width. A window is initiated by the leading edge of any data bit as it enters U26-3 (INDATA). The window is terminated by the same data bit, edge-delayed 60 nsec by U9, at U26-11 (DLYDATA) or by the VCO output (OSC*) at U25-3. When both DLYDATA and OSC* arrive at the detector, it is reset (by U15-12) until the next data bit arrives. When DLYDATA arrives first, it sets its detector latch to produce a pump-up condition to speed up the VCO. When OSC* arrives at its detector latch first, it produces a pump-down condition to slow down the VCO.

Error Amplifier and VCO

The error amplifier consists of a quad transistor pack (U22), and a low-pass filter. U22 is wired as a balanced current mirror device which sources or sinks current to the filter stage. Whenever the phase comparator determines the VCD is running slower that the incoming data stream, the error amp receives pump-up pulses. The filter integrates the resulting output of U22-8 and provides an average increase in the voltage reference to the VCO (TP7), causing the VCO to speed up. Similarly, whenever the phase detector determines the VCO is running faster than the incoming data stream, the error amp receives pump-down pulses. These are also integrated by the filter and produce an average decrease in the VCO voltage reference (TP7), causing the VCO to slow down.

The VCO is a 74LS124 (U30) which is initially set by adjusting C8 to produce a free-running frequency of 10 MHz at TP5.

Write Precompensation

Write precompensation is accomplished by two means: (1) by activating the signal RWC on the drive control bus, and (2) by writing data 12 nsec early or late on cylinders in the specified precompensation area. WD1010 will activate RWC when the drive heads step inward past a pre-programmed cylinder. The drive will use this signal to initiate reduction of write current in the heads at this time. WD1010 continually produces the signals EARLY* and LATE* which are fed into the PAL (U16) along with the signal RWC. When RWC is active, U16 outputs a delayed and latched (by 2XDR) version of EARLY* and LATE* called EELD and LELD. When RWC is not active, the signal NE is produced by U16. EELD, LELD, and NE are then used as enables for U10 to determine which version of write data is passed on to the data driver (U4). The three versions of write data are produced by U9 which has output taps of 12, 24, 36, 48, and 60 nsec. The input to U9 is produced by the PAL output (U16-12) INDATA. INDATA is either write data (WDATA) when write gate (WGATE) is active, or read data (RDATA) when WGATE is inactive.

7.3.3.4 Controller Alignment

1. Move jumper plug from E2-E3 to E1-E2. This feeds a 4 MHz square wave into the WD1100-11 data input.

2. Adjust R4 until a high-going pulse of between 75-80 nsec is seen at TP8. This is the signal DLYDATA.

3. Adjust R3 until the signal DRUN at TP3 just begins to toggle. This is a preliminary adjustment and will be refined later.

4. Replace the jumper plug to position E2-E3.

5. Adjust trim capacitor C8 until a 100 nsec square wave is seen at TP5 and the DC level of the VCO voltage reference (TP7) is between 2 and 3 volts.

6. Using a diagnostic program such as "JHDSYS", format the diagnostic track.

7. Execute a continuous read of that track.

8. Set the scope for a 2 msec sweep rate. Trigger Channel 1 with index (rising edge). You should see two index pulses spaced about 17 msec apart.

9. Place channel 2 scope probe on TP3 (DRUN). Adjust R3 until you can most clearly define 17 distinct pulses on channel 2 between the two index pulses on channel 1. Watch the pass counter of the read program to ensure that no errors are occurring.

10. Recheck the 100 nsec square wave at TP5 and the DC reference voltage at TP7. Look for a stable setting, making adjustments as needed according to Step 5.

7.3.3.5 HDC Register Specifications

The following is a list of the HDC registers and their specific functions. For more information on programming, refer to the WD1010 data sheets.

1. 026CH — Software Reset

   Any read or write to this port will trigger a 10 µsec reset pulse to the HDC.

2. 0270H — Data Register

   This is the port through which data is transferred via the sector buffer between the host and the drive.

3. 0272H — Write - Precomp. Register
   The value written to this port is equal to 1/4 the cylinder number where the WD1010 will begin precompensation.

   Read - HDC Error Register
   If the error bit in the status register is set, then this port is read to determine the error.
   Bit 0 - Not Used
   Bit 1 - Track 0 Error
   Bit 2 - Aborted Command
   Bit 3 - Not Used
   Bit 4 - ID Not Found
   Bit 5 - Not Used
   Bit 6 - CRC Error In Data Fld
   Bit 7 - Bad Block Detected

4. 0274H — Sector Count Register

   Indicates the number of sectors to be transferred.

5. 0276H — Sector Number Register

   Loaded with the number of the sector to be accessed (except during format when this is loaded with the number of bytes to be put in gaps 1 and 3 on the disk).

6. 0278H — Cylinder LSB

   Loaded with the lower eight bits of the cylinder to be accessed.

7. 027AH — Cylinder MSB

   Loaded with the upper two bits of the cylinder to be accessed (only bits 0 and 1 are usable. This gives a ten-bit binary limit to total number of cylinders.)

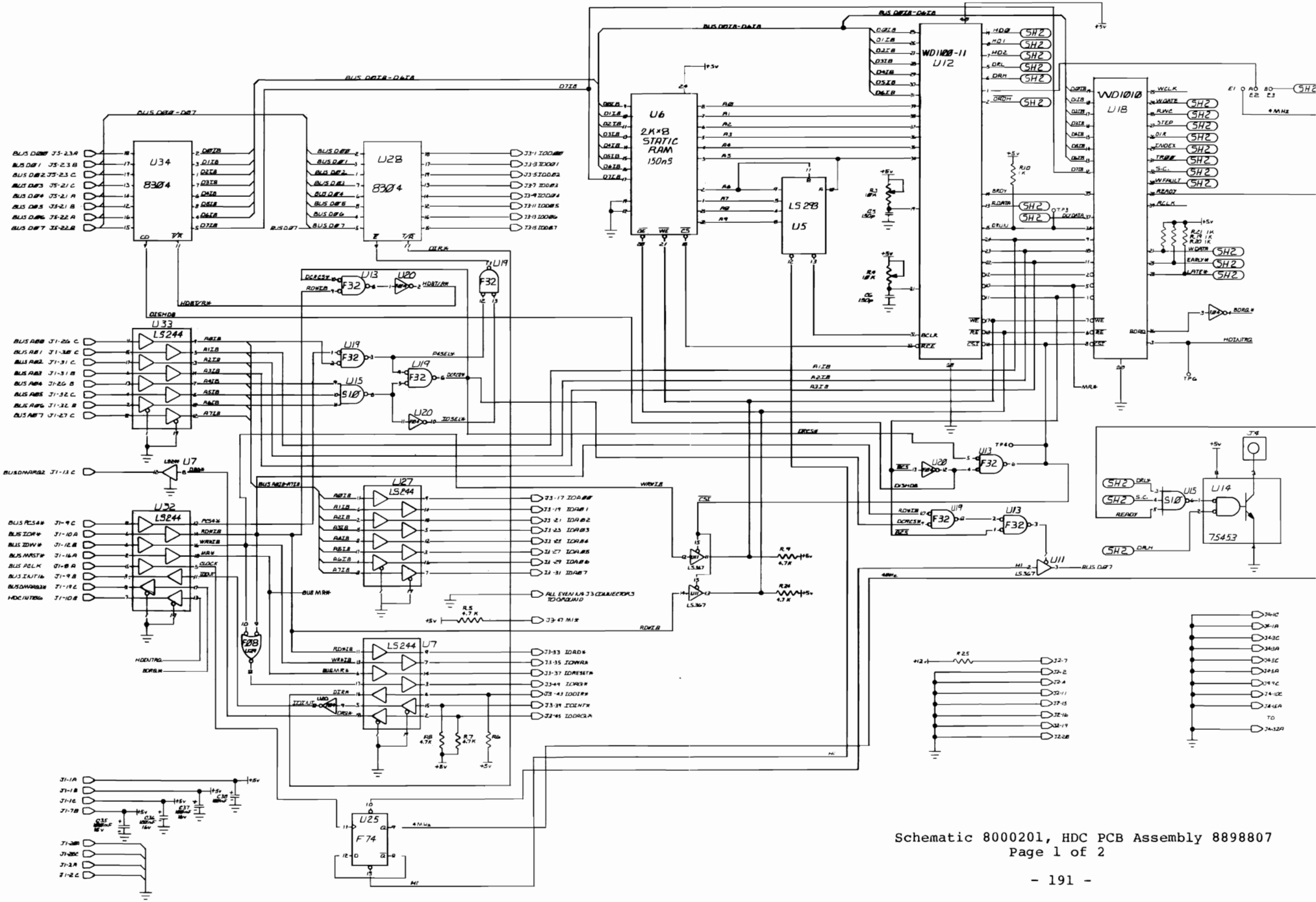
8. 027CH — SDH Register

   This is loaded with the desired sector size, drive select, and head select information using the following format (bit 7 = 0)

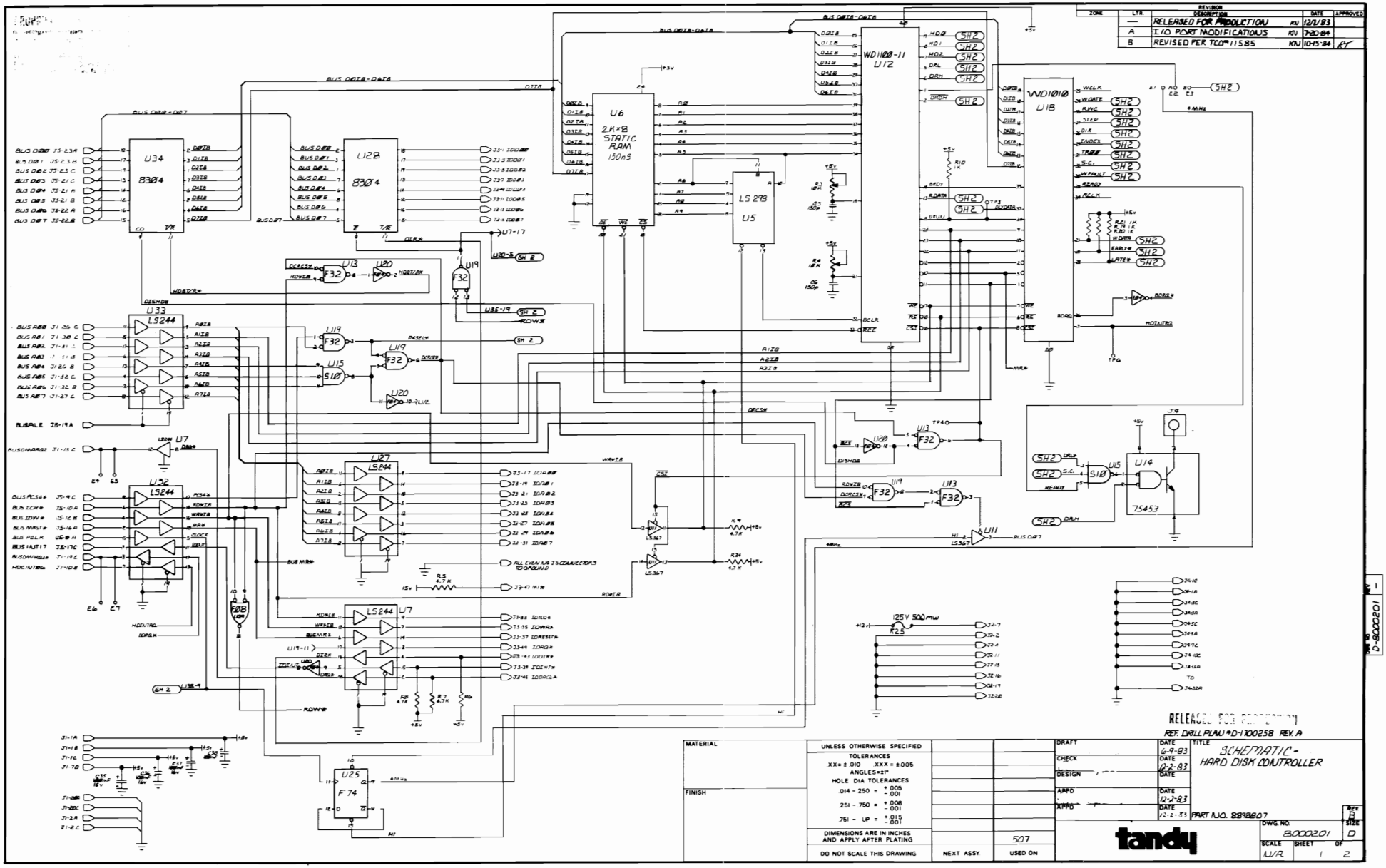
Bits 6	Bits 5	Sector Size
0	0	256
0	1	512
1	0	1024
1	1	128

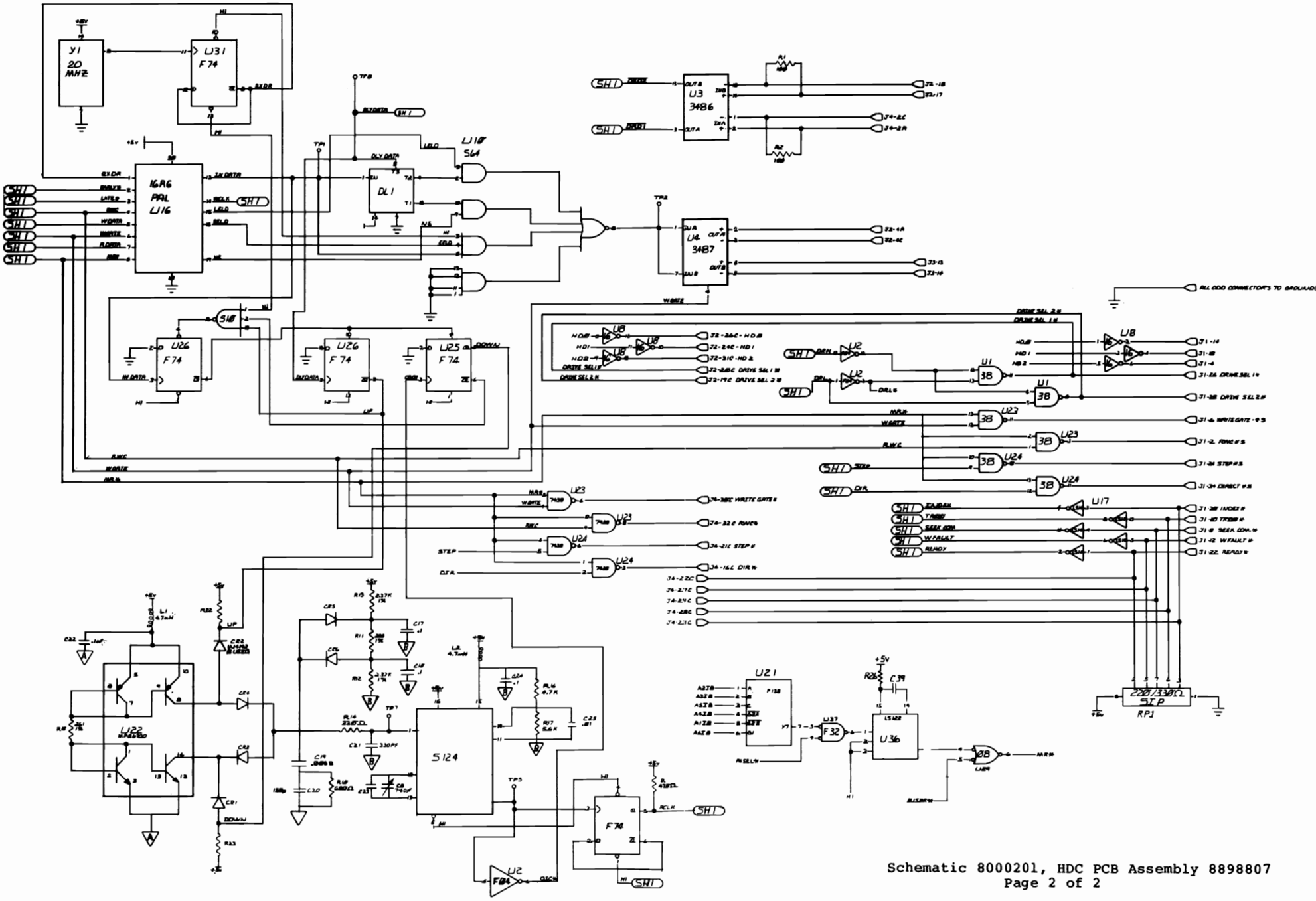
Bits 2	Bits 1	Bits 0	Head Selected
0	0	0	HD 0
0	0	1	HD 1
0	1	0	HD 2
0	1	1	HD 3
1	0	0	HD 4
1	0	1	HD 5
1	1	0	HD 6
1	1	1	HD 7

Bits 4	Bits 3	Drive Selected
0	0	Drive 0
0	1	Drive 1

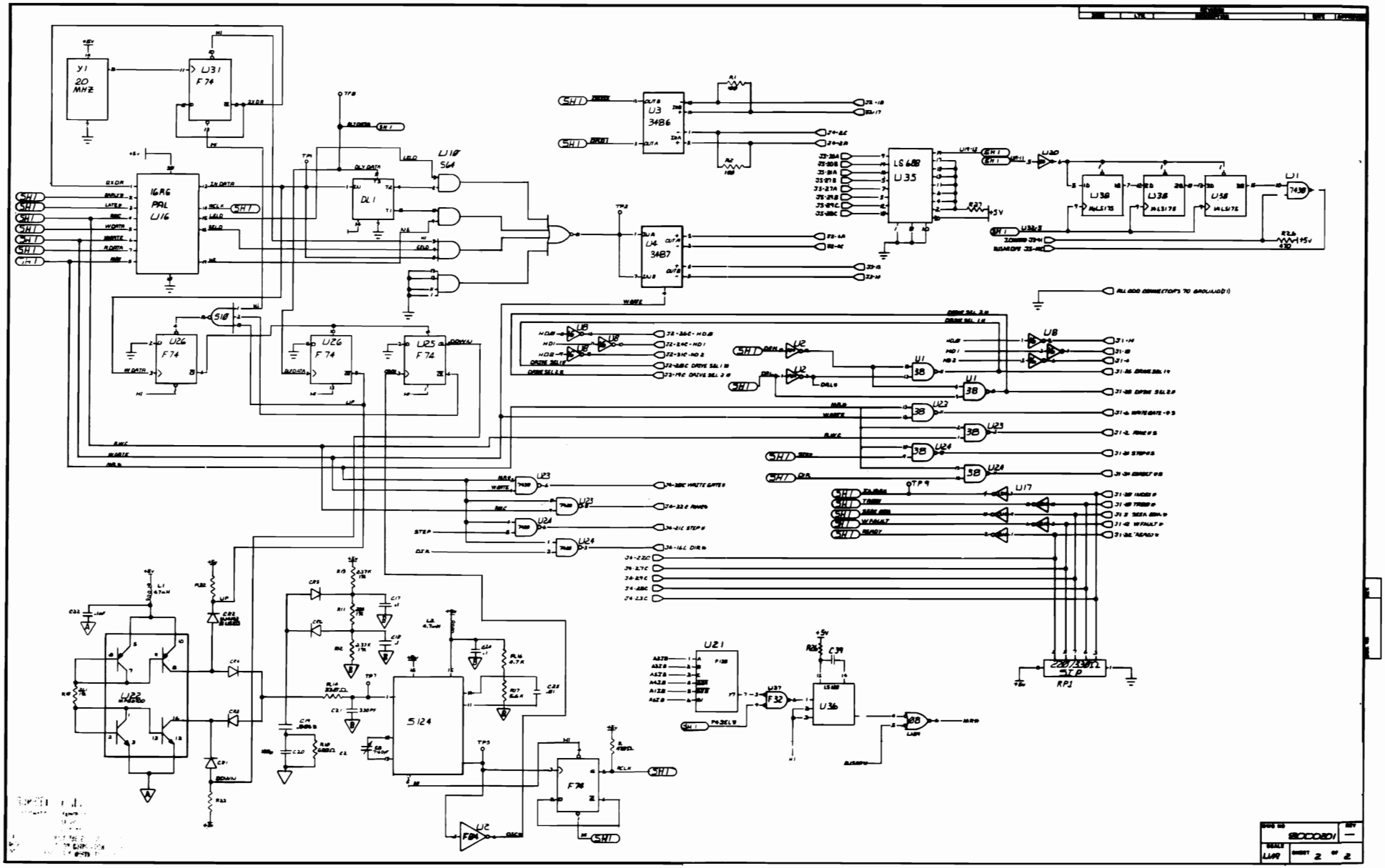


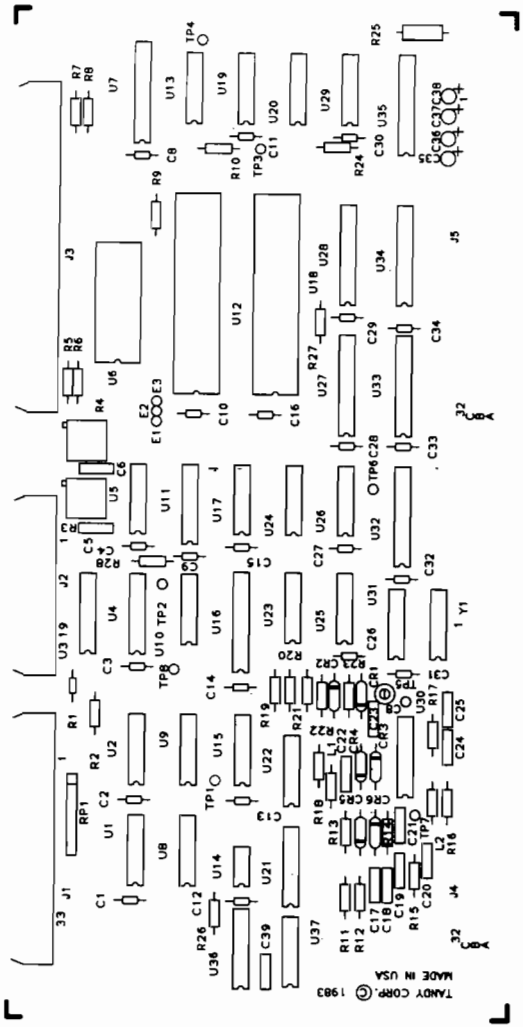
Schematic 8000201, HDC PCB Assembly 8898807
Page 1 of 2


REVISION
LTR | DESCRIPTION | DATE | APPROVED
— | RELEASED FOR PRODUCTION | KN | 12/1/83
A | I/O PORT MODIFICATIONS | KN | 7-20-84
B | REVISED PER TCO# 11585 | KN | 10-15-84 RT
U6 2K×8 STATIC RAM 150nS
WD1100-11 U12
WD1010 U18
LS 298 U5
LS244 U33
LS244 U32
LS244 U27
LS244 U7
F74 U25
75453 U14
RELEASED FOR PRODUCTION
REF. DRILL PLAN #D-1000258 REV. A
MATERIAL
FINISH
UNLESS OTHERWISE SPECIFIED
TOLERANCES
.XX = ± .010 .XXX = ± .005
ANGLES = ±1°
HOLE DIA TOLERANCES
.014 - .250 = +.005 -.001
.251 - .750 = +.008 -.001
.751 - UP = +.015 -.001
DIMENSIONS ARE IN INCHES AND APPLY AFTER PLATING
DO NOT SCALE THIS DRAWING
NEXT ASSY.
507
USED ON
DRAFT
CHECK
DESIGN
APPD
XPPD
DATE 6-9-83
DATE 12-2-83
DATE 12-2-83
DATE 12-2-83
TITLE SCHEMATIC - HARD DISK CONTROLLER
PART NO. 8898807
tandy
DWG NO. 8000201
REV B
SIZE D
SCALE N/A
SHEET 1 OF 2
DWG NO. D-8000201 REV -1

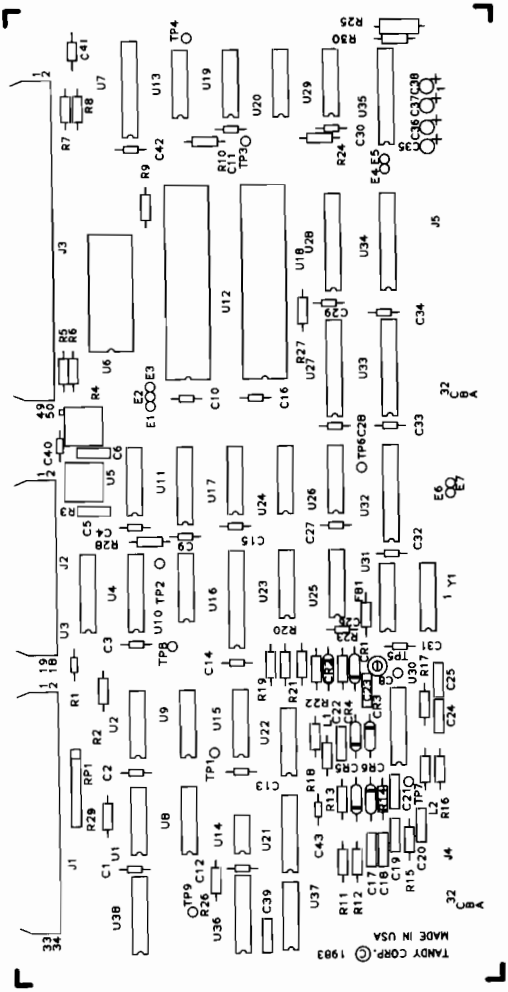


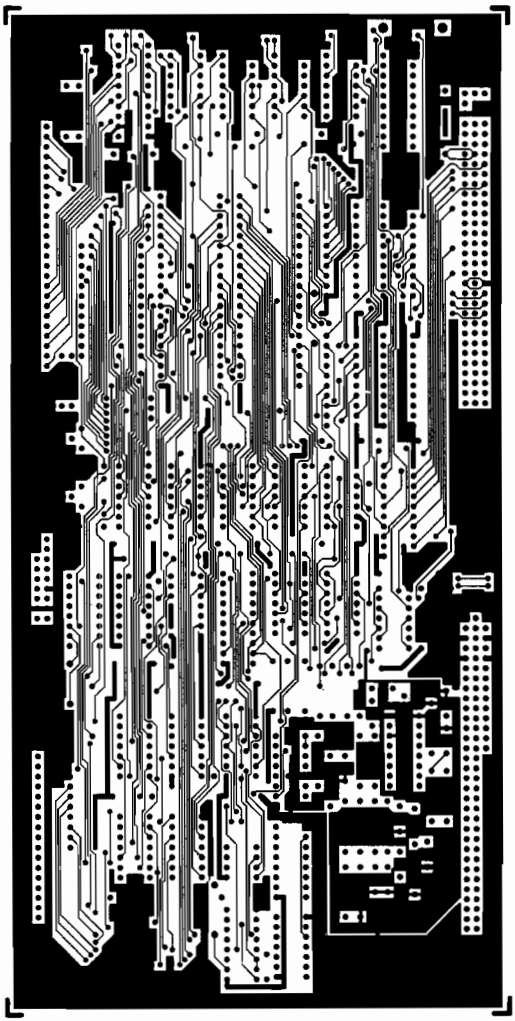
Schematic 8000201, HDC PCB Assembly 8898807
Page 2 of 2



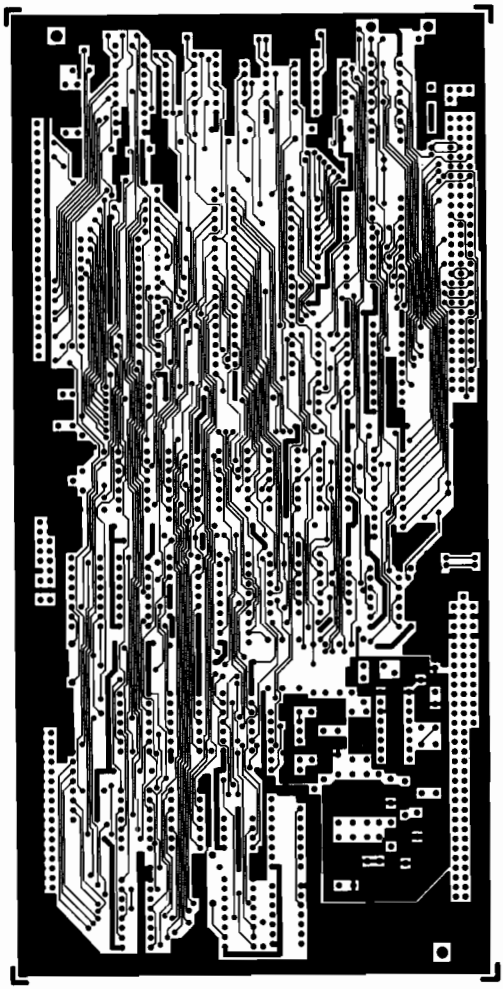


Component Layout, HDC PCB Assembly 8898807

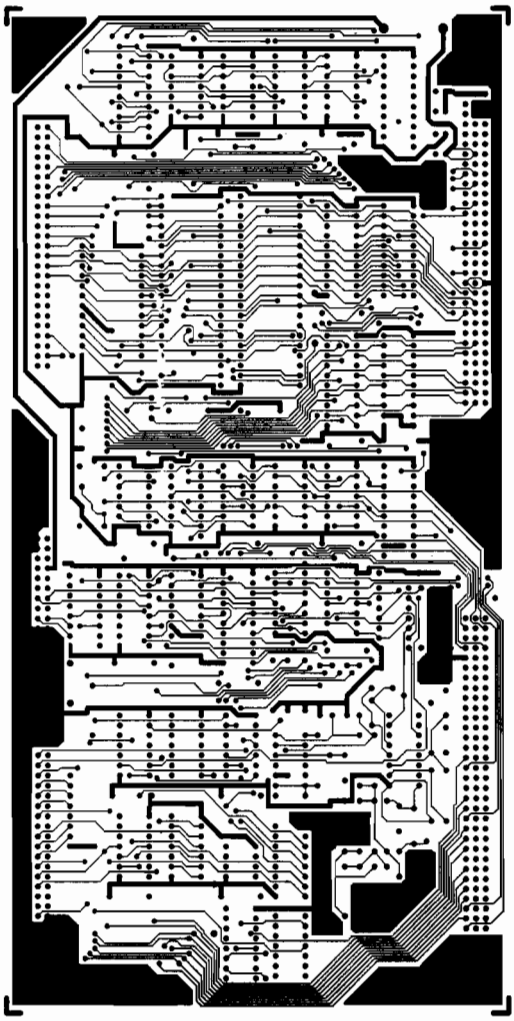

TANDY CORP.
MODEL J HARD DISK CONTROLLER BD.
REF. DWG. NO. 26-3106
SILKSCREEN ARTWORK REV A
TANDY CORP. © 1983
MADE IN USA



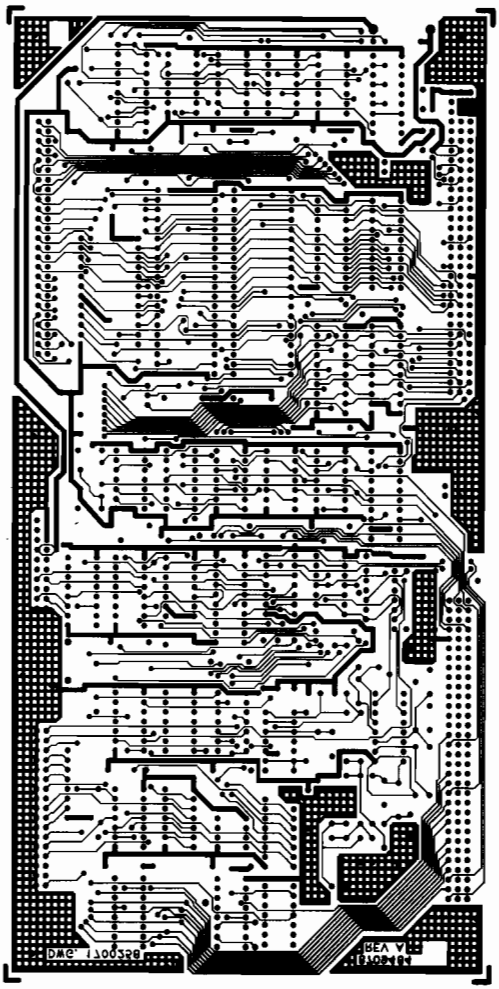
Circuit Trace, HDC PCB Assembly 8898807
Component Side



TANDY CORP.
MODEL 2 HARD DISK CONTROLLER BD.
RS-DOS, MS-DOS, TRSDOS
COMPONENT SIDE ARTWORK REV A



Circuit Trace, HDC PCB Assembly 8898807
Solder Side


TANDY CORP.
MODEL J HARD DISK CONTROLLER BD.
REF. DWG. NO. 1700259
SOLDER SIDE ARTWORK REV A

Parts List

Hard Disk Controller Assembly 889B022

Item	Sym	Description	Part Number
1	1	Chassis, Controller/Interface PCB	8729277
2	2	Nylatch Plunger	8590149
3	2	Nylatch Grommet	8590148
4	1	Insulator, PCB	8539051
5*	1	HDC PCB Assembly	8898807
6	1	Cable Assembly, HDC	8709485
7	2	Screw, #2-56 x 5/16" (Conn. Mtg)	8569212
8	6	Screw, #4-40 x 3/16" (PCB Mtg)	8569220

*See separate parts list

Parts List

Hard Disk Controller Board Assembly 8898807 (8-17-83)

Item	Sym	Description	Part Number
1	1	Hard Disk Controller PCB	8709484
2	10	Staking Pin	8529014
3	1	Connector, 64-Pin DIN (J4)	
4	1	Connector, 96-Pin DIN (J5)	
5	1	Connector, 50-Pin (J3)	
6	1	Connector, 20-Pin (J2)	
7	1	Connector, 34-Pin (J1)	
8	1	Socket, 20-Pin (U16)	8509009
9	1	Socket, 24-Pin (U6)	8509001
10	2	Socket, 40-Pin (U12,18)	8509002
C1		Capacitor, .1 mfd, 50V Mono	8374104
C2		Capacitor, .1 mfd, 50V Mono	8374104
C3		Capacitor, .1 mfd, 50V Mono	8374104
C4		Capacitor, .1 mfd, 50V Mono	8374104
C5		Capacitor, 150 pfd, 50V CerDisk NPO	8301153
C6		Capacitor, 150 pfd, 50V CerDisk NPO	8301153
C8		Capacitor, Trim	
C9		Capacitor, .1 mfd, 50V Mono	8374104
C10		Capacitor, .1 mfd, 50V Mono	8374104
C11		Capacitor, .1 mfd, 50V Mono	8374104
C12		Capacitor, .1 mfd, 50V Mono	8374104
C13		Capacitor, .1 mfd, 50V Mono	8374104
C14		Capacitor, .1 mfd, 50V Mono	8374104
C15		Capacitor, .1 mfd, 50V Mono	8374104
C16		Capacitor, .1 mfd, 50V Mono	8374104
C17		Capacitor, .1 mfd, 50V Mono	8374104
C18		Capacitor, .1 mfd, 50V Mono	8374104
C19		Capacitor, .0068 mfd, 50V Cer Disk	8302684
C20		Capacitor, 150 pfd, 50V CerDisk NPO	8301153
C21		Capacitor, 330 pfd, 50V CerDisk NPO	8301332
C22		Capacitor, .1 mfd, 50V Mono	8374104
C23			
C24		Capacitor, .1 mfd, 50V Mono	8374104
C25		Capacitor, .01 mfd, 50V Cer Disk	8303104
C26		Capacitor, .1 mfd, 50V Mono	8374104
C27		Capacitor, .1 mfd, 50V Mono	8374104
C28		Capacitor, .1 mfd, 50V Mono	8374104
C29		Capacitor, .1 mfd, 50V Mono	8374104
C30		Capacitor, .1 mfd, 50V Mono	8374104
C31		Capacitor, .1 mfd, 50V Mono	8374104
C32		Capacitor, .1 mfd, 50V Mono	8374104

Parts List

Hard Disk Controller Board Assembly 8898807

Item	Sym	Description	Part Number
	C33	Capacitor, .1 mfd, 50V Mono	8374104
	C34	Capacitor, .1 mfd, 50V Mono	8374104
	C35	Capacitor, 100 mfd, 16V Elec Radial	8327101
	C36	Capacitor, 100 mfd, 16V Elec Radial	8327101
	C37	Capacitor, 100 mfd, 16V Elec Radial	8327101
	C38	Capacitor, 100 mfd, 16V Elec Radial	8327101
	CR1	Diode, 1N4148	8150148
	CR2	Diode, 1N4148	8150148
	CR3	Diode, 1N4148	8150148
	CR4	Diode, 1N4148	8150148
	CR5	Diode, 1N4148	8150148
	CR6	Diode, 1N4148	8150148
	L1	Inductor, 4.7 mH	8419017
	L2	Inductor, 4.7 mH	8419017
	R1	Resistor, 100 ohm, 1/4W 5%	8207110
	R2	Resistor, 100 ohm, 1/4W 5%	8207110
	R3	Resistor, 10 kohm, Trimpot	8279312
	R4	Resistor, 10 kohm, Trimpot	8279312
	R5	Resistor, 4.7 kohm, 1/4W 5%	8207247
	R5	Resistor, 4.7 kohm, 1/4W 5%	8207247
	R6	Resistor, 4.7 kohm, 1/4W 5%	8207247
	R7	Resistor, 4.7 kohm, 1/4W 5%	8207247
	R8	Resistor, 4.7 kohm, 1/4W 5%	8207247
	R9	Resistor, 4.7 kohm, 1/4W 5%	8207247
	R10	Resistor, 1 kohm, 1/4W 5%	8207210
	R11	Resistor, 200 ohm, 1/4W 1%	8200120
	R12	Resistor, 2.37 kohm, 1/4W 1%	
	R13	Resistor, 2.37 kohm, 1/4W 1%	
	R14	Resistor, 330 ohm, 1/4W 5%	8207133
	R15	Resistor, 680 ohm, 1/4W 5%	8207168
	R16	Resistor, 4.7 kohm, 1/4W 5%	8207247
	R17	Resistor, 5.6 kohm, 1/4W 5%	8207256
	R18	Resistor, 2.61 kohm, 1/4W 1%	
	R19	Resistor, 1 kohm, 1/4W 5%	8207210
	R20	Resistor, 1 kohm, 1/4W 5%	8207210
	R21	Resistor, 1 kohm, 1/4W 5%	8207210
	R22		
	R23		
	R24	Resistor, 4.7 kohm, 1/4W 5%	8207247
	R25	Resistor, 22 ohm, 1/2W 5%	8217022

Parts List

Hard Disk Controller Board Assembly 8898807

Item	Sym	Description	Part Number
	RP1	Resistor Pak, 220/330 ohm SIP	8290019
	U1	IC, 7438, 2-Input NAND	8000038
	U2	IC, 74F04, Hex Inverter	8015004
	U3	IC, 3486, Quad Receiver	8050486
	U4	IC, 3487, Quad Driver	8050487
	U5	IC., 74LS293, Binary Counter	8020293
	U6	IC, HM6116, 2K x 8 RAM 150 nsec	8046116
	U7	IC, 74LS244, Octal Buffer	8020244
	U9	IC, DDU-4-5060, Delay Line	
	U10	IC, 74S64, AND/OR Inverter	8010064
	U11	IC, 74LS367, Hex Bus Driver	8020367
	U12	IC, WD1100-11	8041111
	U13	IC, 74F32, Quad 2-Input OR	8015832
	U15	IC, 74S10, 3-Input NAND	8010010
	U16	IC, PAL16R6A	8041166
	U17	IC, 74LS14, Hex Inverter	8020014
	U18	IC, WD1010	8041010
	U19	IC, 74F32, Quad 2-Input OR	8015832
	U20	IC, 74F04, Hex Inverter	8015004
	U22	IC, MPQ6700, Transistor Array	
	U23	IC, 7438, 2-Input NAND	8000038
	U24	IC, 7438, 2-Input NAND	8000038
	U25	IC, 74F74, Flip Flop	8015074
	U26	IC, 74F74, Flip Flop	8015074
	U27	IC, 74LS244, Octal Buffer	8020244
	U28	IC, AM8304, Bus Transceiver	8060304
	U29	IC, 74F08, Quad 2-Input AND	8015008
	U30	IC, 74S124, Voltage Con. Osc.	8010124
	U31	IC, 74F74, Flip Flop	8015074
	U32	IC, 74LS244, Octal Buffer	8020244
	U33	IC, 74LS244, Octal Buffer	8020244
	U34	IC, AM8304, Bus Transceiver	8060304
	Y1	Crystal Osc., 20 MHz	8409029

7.4 Motherboard

7.4.1 Introduction

The Model 2000 Mother Board is a part of the Card Cage/Mother Board sub-assembly which provides a simple method of adding optional features to the main unit.

The Mother Board assembly consists of a printed circuit board with four 96-pin male reverse DIN eurocard connectors (DIN 41612) to accommodate the option card(s); a 96-pin female reverse DIN eurocard connector for connection to the Main Logic Board; a 6-pin Molex connector which supplies DC power to the Mother Board and the option card(s) via the DC power harness; and various resistor networks for terminating the signals on the expansion connectors.

7.4.2 Theory of Operation

All of the signals available on the option card connectors are provided for general interface to the Main Logic Board. The only exceptions are seven signals which are specifically used by the graphics option card and are available only on the bottom connector (J18). The following table describes the signal interface and connector pin assignments for option card connector J15-J18.

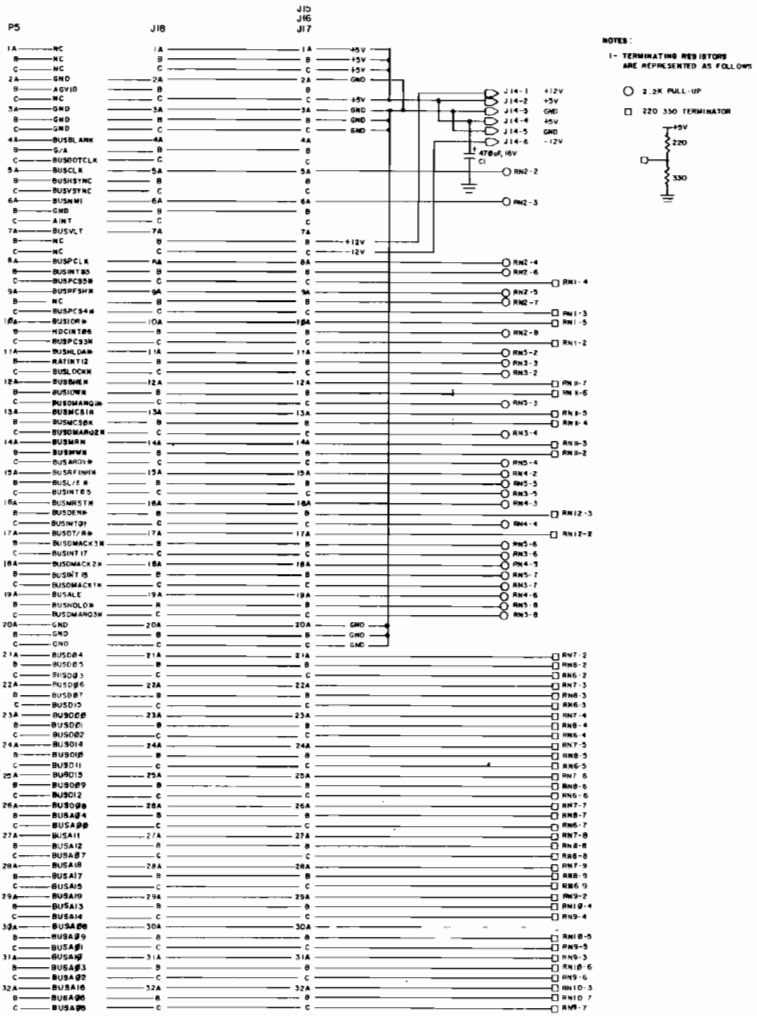
Description	Mnemonic	Pin Number
20-bit Address Bus	BUSA00-BUSA19	26b-32c
16-bit Data Bus	BUSD00-BUSD15	21a-26a
Memory Chip Select	BUSMCS0*, BUSMCS1*	13b, 13a
Peripheral Chip Select	BUSPCS3*, BUSPCS4*, BUSPCS5*	10c, 9c, 8c
Interrupt Control	BUSINT03, BUSINT05, HDCINT06, BUSINT07, RATINT12, MEMINT15, BUSINT17	8b, 15c, 10b, 16c, 11b, 18b, 17c
Non-Maskable Interrupt	NMI*	6a
DMA Request	BUSDMARQ1*, BUSDMARQ2*, BUSDMARQ3*	12c, 13c, 19c
DMA Acknowledge	BUSDMACK1*, BUSDMACK2*, BUSDMACK3*	18c, 18a, 17b
Memory Read and Write	BUSMR*, BUSMW*	14a, 14b
I/O Read and Write	BUSIOR*, BUSIOW*	10a, 12b
Master Reset	BUSMRST*	16a
Address Latch Enable	BUSALE	19a

Data Transmit/Receive	BUSDT/R*	17a
Data Enable	BUSDEN*	16b
System Bus Control	BUSHOLD*, BUSHLDA*, BUSLOCK*, BUSBHE*, BUSL/E*	19b, 11a, 11c, 12a, 15b
Asynchronous Ready	BUSARDY*	14c
Memory Refresh Control	BUSRFSH*, BUSRFINH*	9a, 15a
8 MHz Processor Clock	BUSPCLK	8a
System Clock (not used)	BUSCLK	5a
Video Dot Clock	BUSDOTCLK	4c
Video Vertical Sync	BUSVSYNC	5c
Video Horizontal Sync	BUSHSYNC	5b
Video Blanking	BUSBLANK	4a
Video Intensity	AINT	6c
Video Control	BUSVLT, AGVID, G/A	7a, 2b, 4b

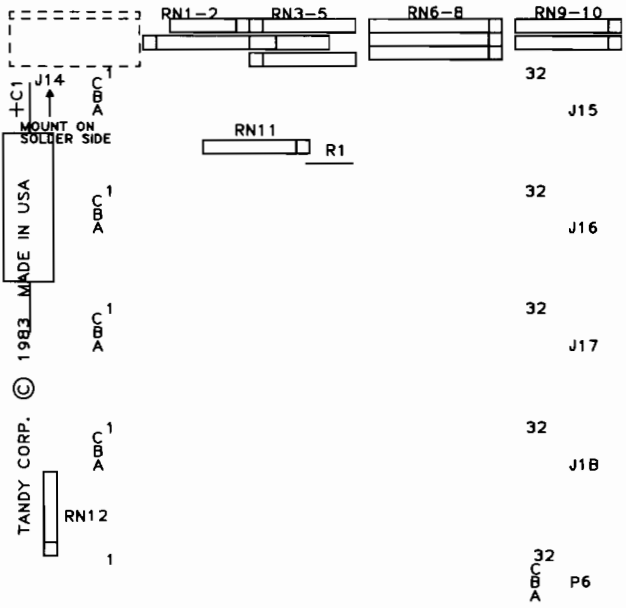
DC power is supplied directly to the Mother Board through a 6-pin Molex connector (J14). Pin assignments for DC power are shown in the table below.

	Connector J14	Connector J15-J18
+12 Volts	1	7b
-12 Volts	6	7c
+5 Volts	2, 4	1a, 1b, 1c, 2c
Ground	3, 5	2a, 3a, 3b, 3c, 6b, 20a, 20b, 20c

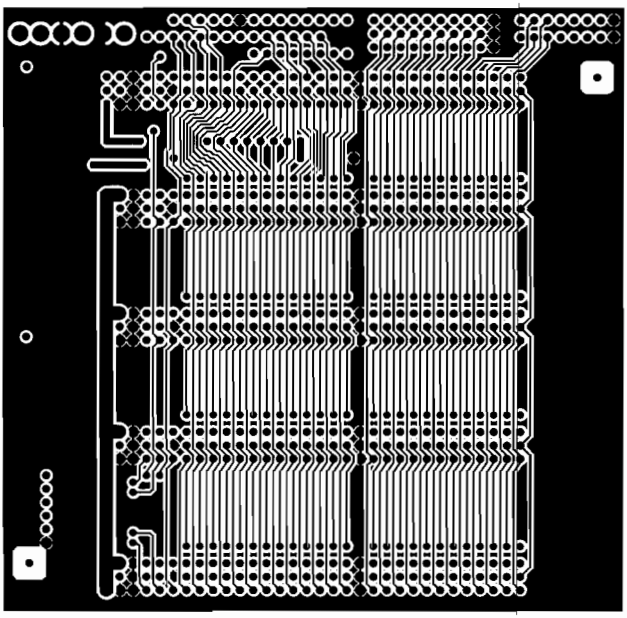
All of the signals, except the video signals, that are used by the option cards have been terminated on the Mother Board. Resistor networks have been used to either pull up the signal with a 2.2 kohm resistor to +5 volts or establish a 3-volt level using a 220 ohm/330 ohm split termination. See the schematic to determine the termination on each signal.



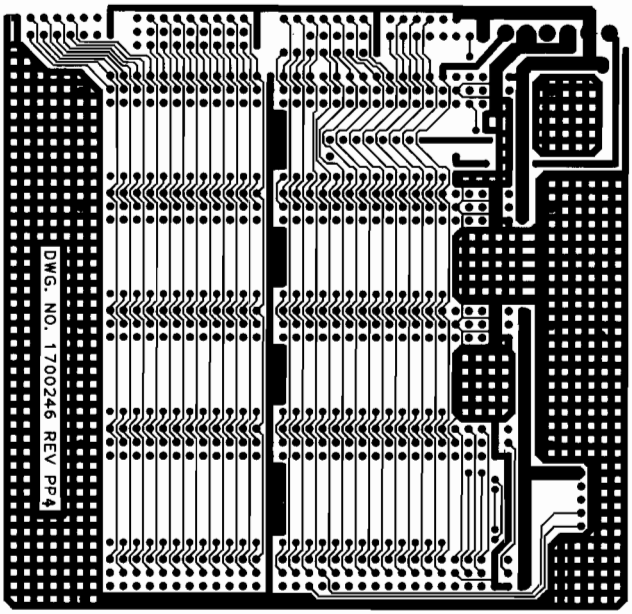
Schematic 8000212, Mother Board



Component Layout, Mother Board PCB Assembly 8898803



Circuit Trace, Mother Board PCB Assembly 8898803
Component Side



Circuit Trace, Mother Board PCB Assembly 8898803
Solder Side

Parts List

Mother Board Assembly 8898803

Item	Sym	Description	Part Number
1	1	Mother Board PCB	8709431
2	1	Connector, 96-pin Rt. Ang. Fem (P6)	8519181
3	1	Connector, 6-pin Straight (J14)	8519186
4	4	Connector, 96-pin Male (J15-18)	8519182
5	1	Serial Number Tag, PCB	87891045
6	2	Screw, #2-56 x 3/8" PPH	8569201
7	2	Nut, #2-56	8579042
R1		Resistor, 0 ohm	8290000
RN1		Res. Pak, 220/330 ohm 6-pin SIP	8
RN2		Res. Pak, 2.2 kohm 8-pin SIP	8290039
RN3		Res. Pak, 2.2 kohm 8-pin SIP	8290039
RN4		Res. Pak, 2.2 kohm 6-pin SIP	8290043
RN5		Res. Pak, 2.2 kohm 8-pin SIP	8290039
RN6		Res. Pak, 220/330 ohm 10-pin SIP	8290020
RN7		Res. Pak, 220/330 ohm 10-pin SIP	8290020
RN8		Res. Pak, 220/330 ohm 10-pin SIP	8290020
RN9		Res. Pak, 220/330 ohm 8-pin SIP	8290019
RN10		Res. Pak, 220/330 ohm 8-pin SIP	8290019
RN11		Res. Pak, 220/330 ohm 8-pin SIP	8290019
RN12		Res. Pak, 220/330 ohm 6-pin SIP	8

7.5 128K RAM PCB

7.5.1 INTRODUCTION

The Model 2000 has the capablility of 256K words of memory, with parity, located on the Main Logic Board. This memory is separated into two sections: a 128K word System Memory board and a 128K word Internal Expansion Memory board. The System Memory is mapped from 00000H to 1FFFFH and the Internal Expansion Memory is mapped from 20000H to 3FFFFH.

7.5.2 THEORY OF OPERATION - 128K SYSTEM RAM

The System RAM board consists of a 6.3 inch by 2.5 inch printed circuit board with eighteen high speed dynamic Random Access Memories (RAM's). Each RAM device is organized as 65,536 one bit words with a maximum access time of 150 nanoseconds. Bulk decoupling of the +5 volt power bus to the RAM's is provided by 100 microfarad, 6.3 volt dipped tantalum electrolytic capacitors. Also, each device is decoupled with a 0.1 microfarad capacitor across its Vcc (pin 8) and ground (pin 16) pins.

Interface to the memory control and timing sections on the Main Logic Board is accommplished through a special pin header which mates with a 40-pin, bottom entry connector (P11) on the System RAM board. Signal pin assignments for P11 are shown in Table 1. The System RAM board also interfaces to the Internal Expansion RAM board through a 40-pin, right angle receptacle (P13). Table 2 specifies pin assignments for P13.

7.5.3 SIGNAL DEFINITION

The following list defines each signal available on the System RAM connectors. For specific memory control and timing specifications see Section 7.1.8 of the Main Logic Board theory of operation.

ADDRESS RANGE	00000H-1FFFFH	20000H-3FFFFH
Write Input	WR0*	WR1*
Row Address Select	RAS0*	RAS1*
WORD SEGMENT	UPPER	LOWER
Column Address Select	CASL*	CASU*
Data Input Parity	DIPL	DIPU
Data Output Parity	DOPL	DOPU
8-bit Memory Address Bus	DMEMA00-DMEMA07	
16-bit Memory Data Bus	IB00-IB15	

7.5.4 Troubleshooting

Memory Read or Write errors can be determined by using the memory diagnostic routines that are available for the Model 2000.

After initializing the test program, a top of memory algorithm is executed to determine how much memory has been installed in the Model 2000 under test. If the response to the memory size inquiry does not agree with the amount of memory the user has installed, it can be assummed that either the memory installation was not performed correctly or the memory boards installed are defective. The user should check all connectors to insure proper and complete mating before attempting to isolate a defective board and/or component.

Once the user is confident of the installation integrity, the memory diagnostic test may be run. There are three tests that are available: a read/write data test; a long modified address test and a short modified address test.

The data test writes a known data pattern to all memory locations. The data is then read back and compared to the known data pattern for errors. Errors generated by this test would indicate a problem either on the data/address bus interface to memory or with the decoders associated with the memory array.

The modified address test has two versions: the long test will test the RAM 65,536 times per pass (0000H-FFFFH) and the short test will test the RAM 256 times per pass (0000-00FF). The number of tests per pass is determined by a 16-bit mask register which is incremented by one for each write/read cycle through the entire memory array (i.e., 00000H-7FFFFH for 512K). The data pattern written is the result of the exclusive-OR of the high address segment register (16-bit) with the result of the exclusive-OR of the lower address segment or offset (16-bit) and the mask register. This data pattern is written through the memory array and then read and compared to check for accuracy. Errors that occur will be listed individually in the error table that specifies the data written, the data read, the exclusive-OR of the data written and the data read, and the address where the error occurred. In most cases, this will indicate which RAM chip in a particular bank has failed.

It is recommended that all three RAM tests should be used to verify correct operation of the RAM installed in the unit. Although these tests do not exercise every combination of bits that can be written throughout the full RAM capacity, they exercise enough write/read operations to achieve a fairly reliable test of memory I/O and data recovery to isolate most common memory failures. A complete test that exercises every bit in an array is impractical because of the extreme number of bit combinations, especially in larger memory arrays. For a 16-bit system, there are $16(2^n)$ combinations, where n equals the memory size (e.g., 128K,256K,512K), that must be written, read and compared to complete the full test. In comparison, the modified address method reduces the amount of time it takes to complete a pass but even the long modified address test on a 512K memory array will take approximately 30 hours to complete.

Table 7-9. Pll Pin Assignments

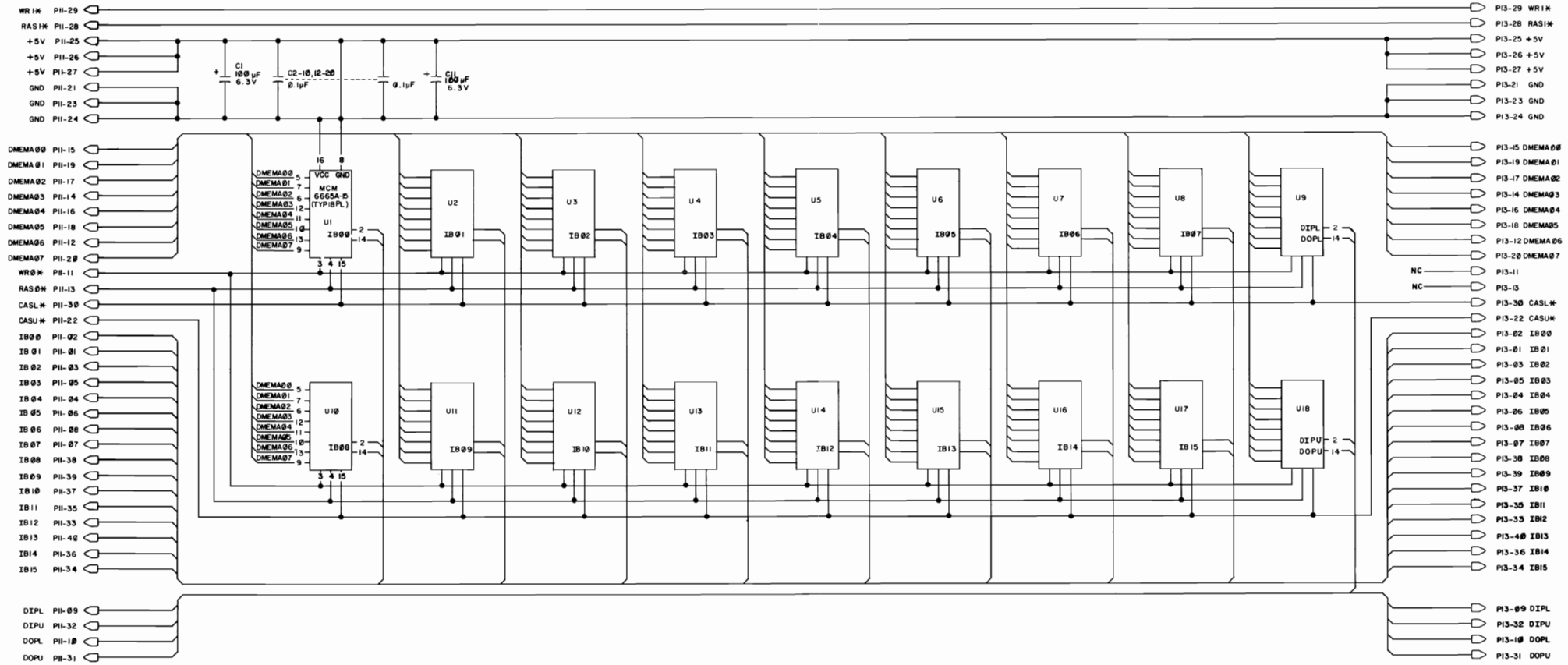
System RAM To Main Logic Board Interface

PIN #	SIGNAL	PIN #	SIGNAL
01	IB01	02	IB00
03	IB02	04	IB04
05	IB03	06	IB05
07	IB07	08	IB06
09	DIPL	10	DOPL
11	WR0*	12	DMEMA06
13	RAS0*	14	DMEMA03
15	DMEMA00	16	DMEMA04
17	DMEMA02	18	DMEMA05
19	DMEMA01	20	DMEMA07
21	GROUND	22	CASU*
23	GROUND	24	GROUND
25	+5 VOLTS	26	+5 VOLTS
27	+5 VOLTS	28	RAS1*
29	WR1*	30	CASL*
31	DOPU	32	DIPU
33	IB12	34	IB15
35	IB11	36	IB14
37	IB10	38	IB08
39	IB09	40	IB13

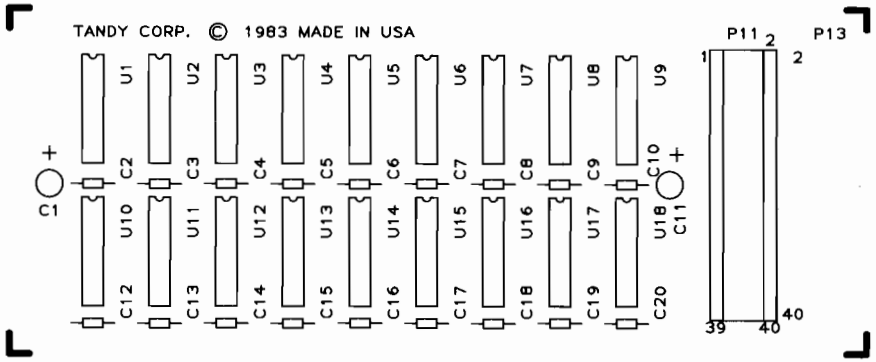
Table 7-10. P13 Pin Assignments

System RAM To Internal Expansion RAM Interface

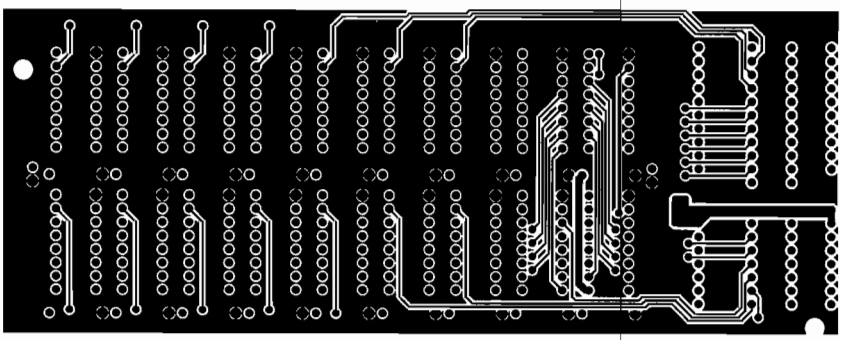
PIN #	SIGNAL	PIN #	SIGNAL
01	IB01	02	IB00
03	IB02	04	IB04
05	IB03	06	IB05
07	IB07	08	IB06
09	DIPL	10	DOPL
11	NO CONNECTION	12	DMEMA06
13	NO CONNECTION	14	DMEMA03
15	DMEMA00	16	DMEMA04
17	DMEMA02	18	DMEMA05
19	DMEMA01	20	DMEMA07
21	GROUND	22	CASU*
23	GROUND	24	GROUND
25	+5 VOLTS	26	+5 VOLTS
27	+5 VOLTS	28	RASl*
29	WRl*	30	CASL*
31	DOPU	32	DIPU
33	IB12	34	IB15
35	IB11	36	IB14
37	IB10	38	IB08
39	IB09	40	IB13



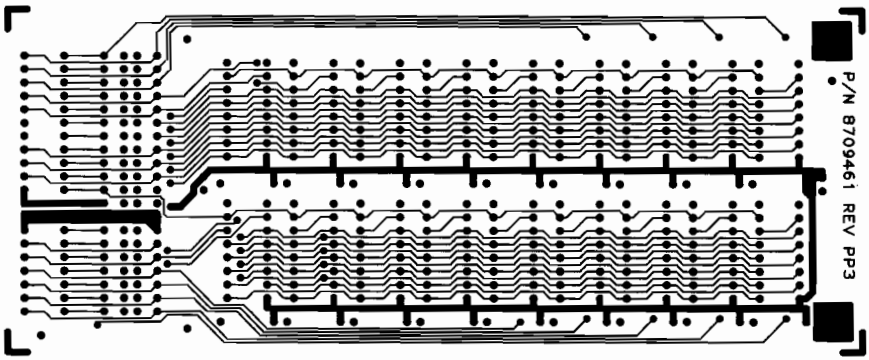
Schematic 8000204, System RAM



Component Layout, System RAM PCB Assembly 8898806



Circuit Trace, System RAM PCB Assembly 8898806
Component Side



Circuit Trace, System RAM PCB Assembly 8898806
Solder Side

Parts List

128K Internal RAM Board Assembly 8898806

Item	Sym	Description	Part Number
1	1	128K RAM PCB	8709461
2	2	Connector, 20-Pin Bottom Entry(P11)	8519199
3	1	Connector, 40-Pin (P13)	8519200
4	1	PCB Serial Number Label	87891043
C1		Capacitor, .1 mfd, 50V Mono Axial	8374104
C2		Capacitor, .1 mfd, 50V Mono Axial	8374104
C3		Capacitor, .1 mfd, 50V Mono Axial	8374104
C4		Capacitor, .1 mfd, 50V Mono Axial	8374104
C5		Capacitor, .1 mfd, 50V Mono Axial	8374104
C6		Capacitor, .1 mfd, 50V Mono Axial	8374104
C7		Capacitor, .1 mfd, 50V Mono Axial	8374104
C8		Capacitor, .1 mfd, 50V Mono Axial	8374104
C9		Capacitor, .1 mfd, 50V Mono Axial	8374104
C10		Capacitor, 100 mfd, 6V Tant. Rad.	8337100
C11		Capacitor, .1 mfd, 50V Mono Axial	8374104
C12		Capacitor, .1 mfd, 50V Mono Axial	8374104
C13		Capacitor, .1 mfd, 50V Mono Axial	8374104
C14		Capacitor, .1 mfd, 50V Mono Axial	8374104
C15		Capacitor, .1 mfd, 50V Mono Axial	8374104
C16		Capacitor, .1 mfd, 50V Mono Axial	8374104
C17		Capacitor, .1 mfd, 50V Mono Axial	8374104
C18		Capacitor, .1 mfd, 50V Mono Axial	8374104
C19		Capacitor, .1 mfd, 50V Mono Axial	8374104
C20		Capacitor, 100 mfd, 6V Tant. Rad.	8337100
U1		IC, MCM6665-15 RAM	8041665
U2		IC, MCM6665-15 RAM	8041665
U3		IC, MCM6665-15 RAM	8041665
U4		IC, MCM6665-15 RAM	8041665
U5		IC, MCM6665-15 RAM	8041665
U6		IC, MCM6665-15 RAM	8041665
U7		IC, MCM6665-15 RAM	8041665
U8		IC, MCM6665-15 RAM	8041665
U9		IC, MCM6665-15 RAM	8041665
U10		IC, MCM6665-15 RAM	8041665
U11		IC, MCM6665-15 RAM	8041665
U12		IC, MCM6665-15 RAM	8041665
U13		IC, MCM6665-15 RAM	8041665
U14		IC, MCM6665-15 RAM	8041665
U15		IC, MCM6665-15 RAM	8041665
U16		IC, MCM6665-15 RAM	8041665
U17		IC, MCM6665-15 RAM	8041665
U18		IC, MCM6665-15 RAM	8041665

7.6 Keyboard Assembly

The keyboard for the Tandy Model 2000 computer is a 90-key keyboard with twelve function keys, numeric keypad, and special purpose keys for paging. It is connected to the Main Unit by a coiled cable and may be operated from a location up to 4 feet from the main unit. The cable assembly may be disconnected from the keyboard assembly during repair if desired (see Paragraph 6.4 for disassembly procedures).

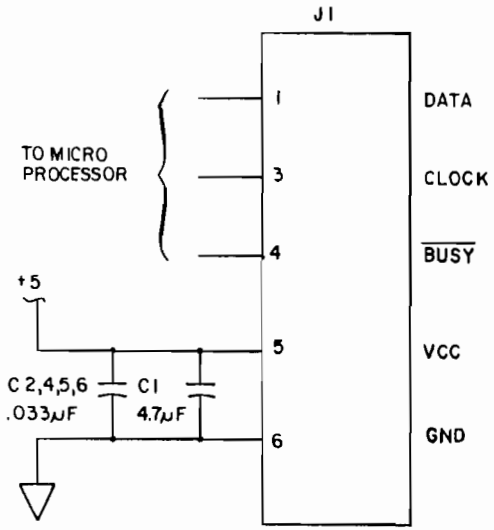


Figure 7-39. Keyboard Assembly Connector

7.6.1 Keyboard Specifications

The keyboard is a fully encoded type with microprocessor control. Power required by the keyboard is +5 Vdc supplied from the Main Unit.

1. Key Type - all keys generate "make" and "break" codes. See Key Code Chart for key codes. Break codes are formed by adding 80H to the make code. Keys 49 and 71 have alternate action which "makes" on one actuation of the key and "breaks" on succeeding actuation. No code is generated for these two keys when the key is released.

2. Number of Keys - 90

3. Repeat Strobe - there is a repeat strobe of 66 to 111 msec when any key is depressed for more that 1 second with the exception of SHIFT, CTRL, CAPS, ENTER and NUMBER LOCK.

7.6.2 Key Code Chart

Key Number	Legend	Scan Code
1	F1	3B
2	F2	3C
3	F3	3D
4	F4	3E
5	F5	3F
6	F6	40
7	F7	41
8	F8	42
9	F9	43
10	F10	44
11	F11	59
12	F12	5A
13	INSERT	55
14	DELETE	53
15	BREAK	54
16	ESC	01
17	1 !	02
18	2 @	03
19	3 #	04
20	4 $	05
21	5 %	06
22	6 ^	07
23	7 &	08
24	8 *	09
25	9 (	0A
26	0)	0B
27	- _	0C
28	= +	0D
29	BACKSPACE	0E
30	ALT	38
31	PRINT	37
32	7 (backslash)	47
33	8 (Tilde)	48
34	9 PG UP	49
35	TAB	0F
36	Q	10
37	W	11
38	E	12
39	R	13
40	T	14
41	Y	15
42	U	16
43	I	17
44	O	18
45	P	19

Key Number	Legend	Scan Code
46	{ [	1A
47	}]	1B
48	HOLD	46
49	NUM LOCK	45
50	4 :	4B
51	5	4C
52	6	4D
53	CTRL	1D
54	A	1E
55	S	1F
56	D	20
57	F	21
58	G	22
59	H	23
60	J	24
61	K	25
62	L	26
63	; :	27
64	' "	28
65	ENTER	1C
66		29
67	HOME	58
68	1 END	4F
69	2 (Grave)	50
70	3 PG DN	51
71	CAPS	3A
72	SHIFT	2A
73	Z	2C
74	X	2D
75	C	2E
76	V	2F
77	B	30
78	N	31
79	M	32
80	, <	33
81	. >	34
82	/ ?	35
83	SHIFT	36
84		2B
85		4A
86		4E
87	0	52
88	.	56
89	ENTER	57
90	(Space Key)	39
91 thru 95	- reserved for International	

7.6.3 Keyboard Timing

Figure 7-40 is the timing chart for the Model 2000 Keyboard Assembly.

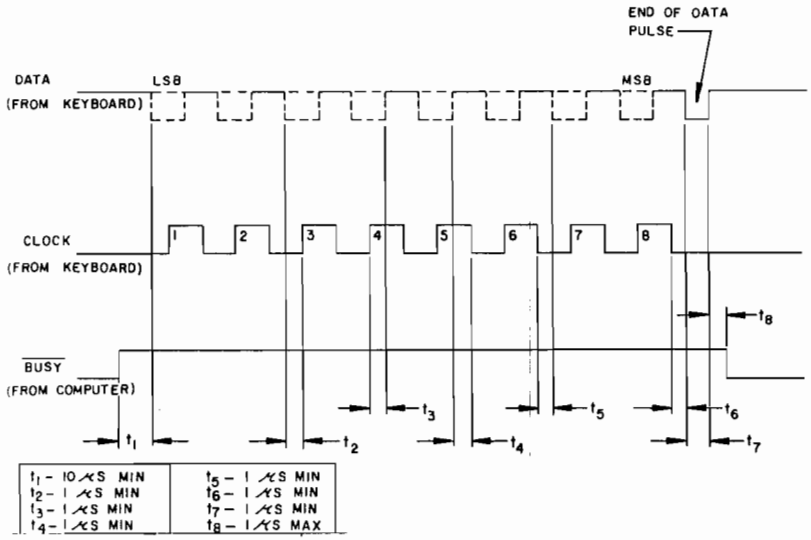


Figure 7-40. Keyboard Assembly Timing Chart

7.6.4 Keyboard Layout

Shown below is the keyboard layout and number designation of the keys on the Model 2000 keyboard. They should be used with Table 7-11 (Key Code Chart) for determining data signal transmitted by the keyboard.

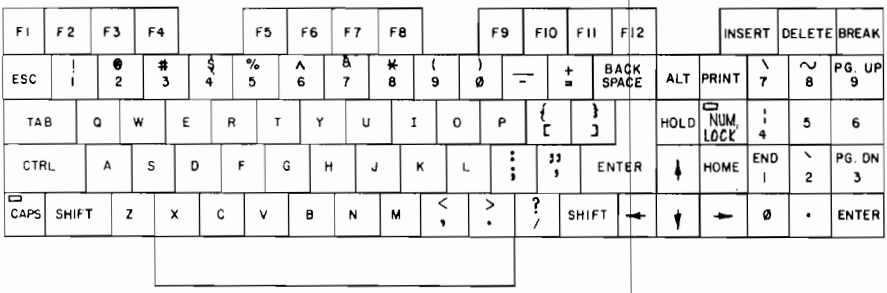
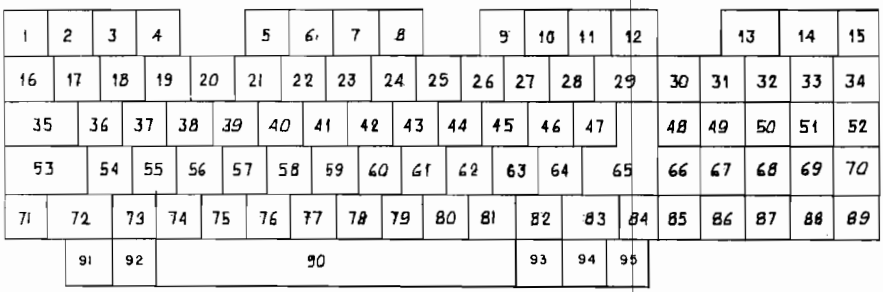
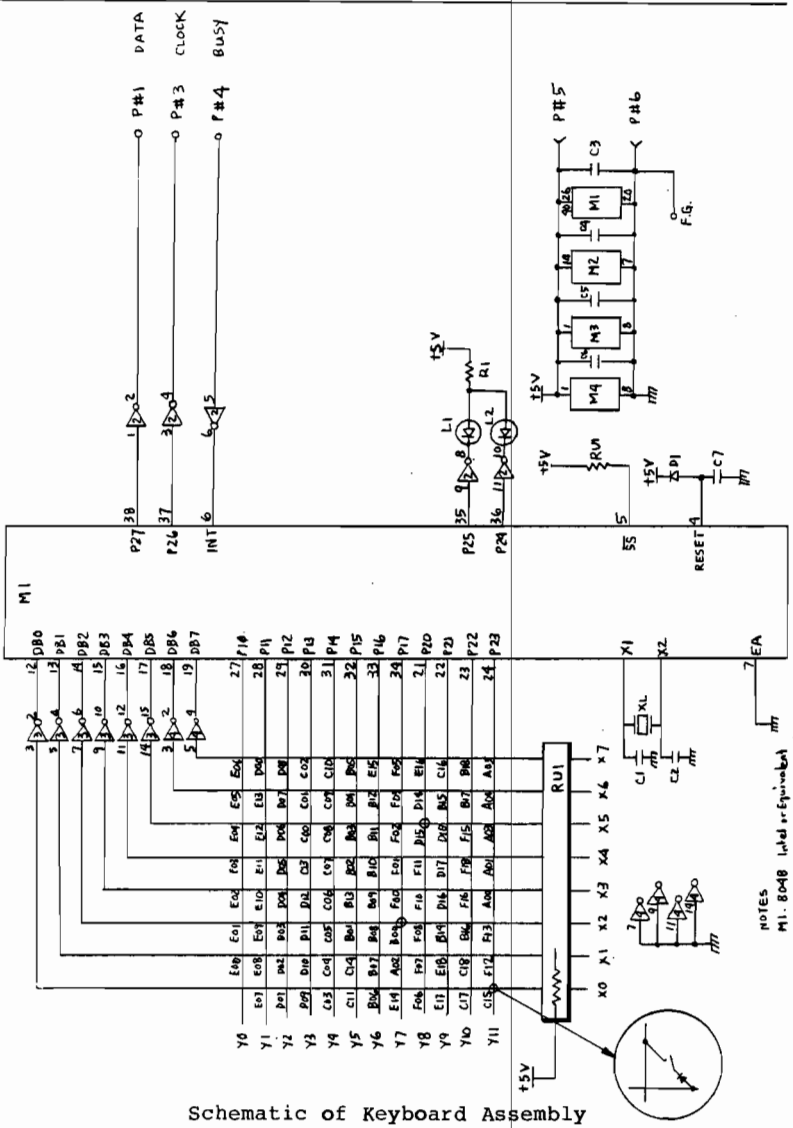


Figure 7-41. Keyboard Identification



NOTE: KEYS 91 THRU 95 NOT USED ON U.S. VERSION, USED ON INTERNATIONAL VERSION ONLY

Figure 7-42. Key Number Identification



Schematic of Keyboard Assembly

8/ Parts Lists/Exploded Views

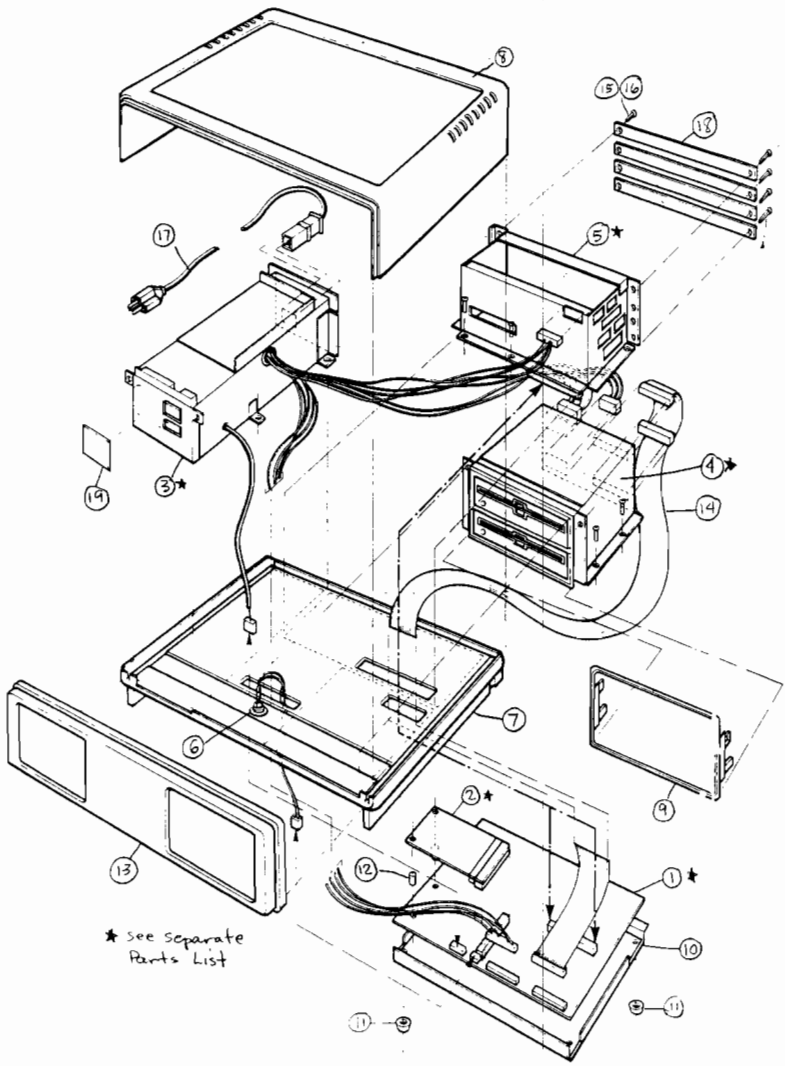
Contained in this section of the manual are parts lists and exploded views and parts lists for the various subassemblies of the Tandy Model 2000 Microcomputer. This section has been divided into major subassembly components to facilitate its use. These sections include the Main Logic Unit (with associated subassembly drawings/parts lists), and the Keyboard Assembly. The Display Unit and Internal Floppy Disk Drive/Hard Disk Drive Assemblies are described in Appendices at the end of this manual. Other optional features are described and listed in supplements which support the particular option.

Pictorial representation contained in the exploded views may vary slightly from the actual unit due to improvements incorporated into the unit after printing of this manual. For information concerning variations, contact Technical Support in Fort Worth, Texas.

Parts List

Main Logic Unit Assembly

Item	Sym	Description	Part Number
1	1	Main Logic PCB Assembly	889B001
2	1	128K RAM Board Assembly	8898806
3	1	Power Supply Assembly	889B003
3A	1	Power Supply Insulator	2930050
4	1	Mini-Floppy Disk Drive Assembly	
5	1	Card Cage Assembly	
6	1	Speaker Assembly	
7	1	Bottom, Case	8719320
8	1	Top, Case	8719319
9	1	Bezel, Disk Drive (Mitsubishi)	8719401
	1	Bezel, Disk Drive (Tandon)	8719355
	2	Handle, Disk Drive (Tandon)	8719353
10	1	Chassis, Main Logic PCB	8729240
11	4	Foot, Case	8719370
12	2	Standoff, RAM Board	8590150
13	1	Bezel, Front	8719318
14	1	Cable Assembly, Floppy Disk Signal	8709447
15	8	Plunger, Nylatch	8590149
16	8	Grommet, Nylatch	8590148
17	1	Power Cord, AC	8709468
18	4	Panel, Card Cage	8729233
19	1	Logo	8719330

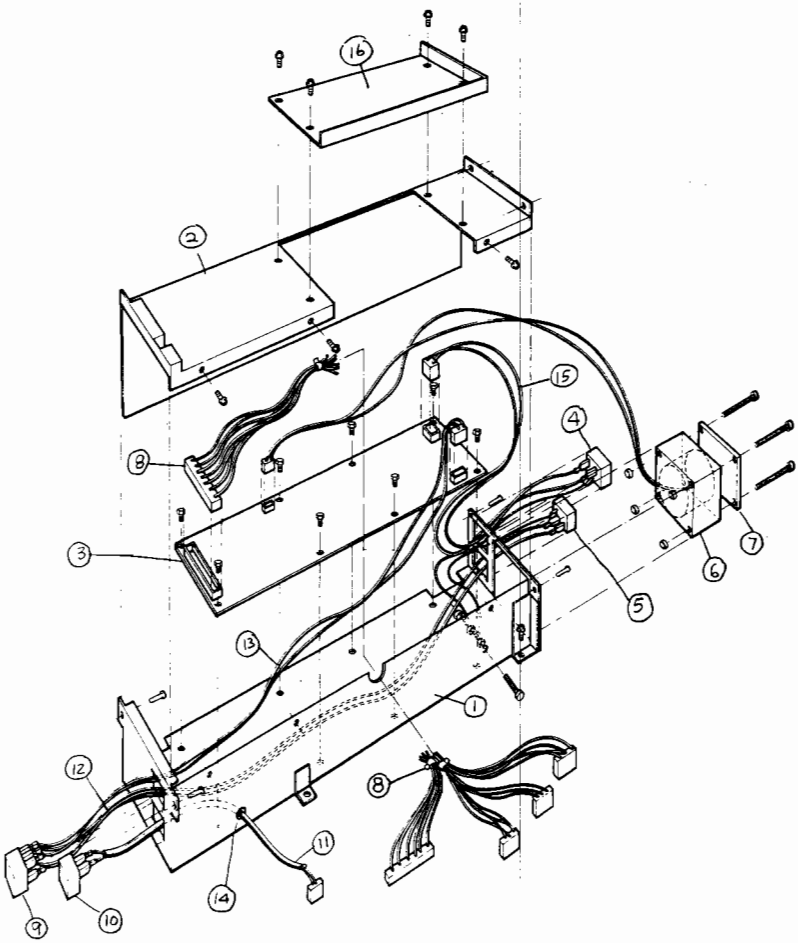


Exploded View, Main Logic Unit

Parts List

Power Supply Assembly 88898003 (95W Tandy)

Item	Sym	Description	Part Number
1	1	Weldment, Lower Enclosure	8729256
2	1	Enclosure, Upper	8729231
3	1	Power Supply PCB Assembly	8790056
4	1	Convenience Outlet	8519195
5	1	AC Inlet	8519207
6	1	Fan, DC	8790407
7	1	Guard, Finger	8719369
8	1	Cable Assembly, DC Main Power	
9	1	Switch, Power	8489073
10	1	Switch, Reset	8489071
11	1	Cable Assembly, Reset	8709464
12	1	Cable Assembly, AC Power In	8709471
13	1	Cable Assembly, Power Switch	8709467
14	1	Bushing, Reset Harness	
15	1	Cable Assembly, Auxiliary Power	8709466
16	1	Cover, Power Supply	8729230
17	1	Fuse, AC (5 x 20 mm)	8479033
18	1	Insulator	2930050

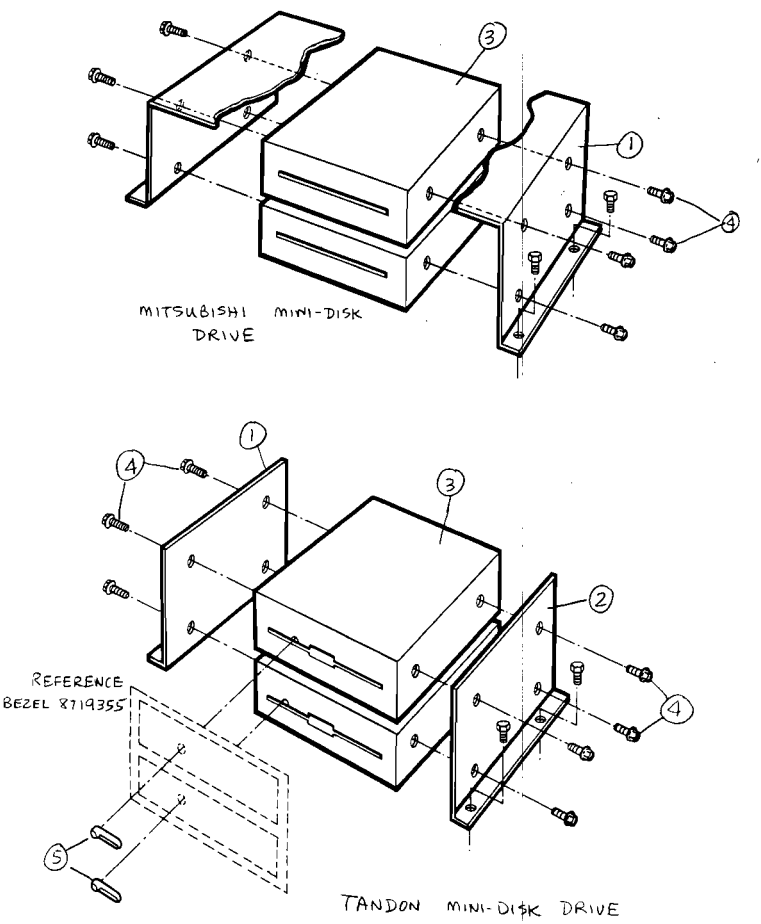


Exploded View, Power Supply Assembly 889B003

8.1.2 Mini-Floppy Disk Drive Assembly

Item	Sym	Description	Part Number
1	1	Bracket, LH Mounting (Tandon Drive)	8729235
	1	Bracket, Mtg (Mitsubishi Drive)	8719401
2	1	Bracket, RH Mounting (Tandon Drive)	8729236
3	2	Drive, Mini-Floppy Disk (Tandon)	8790122
	2	Drive, Mini-Floppy Disk(Mitsubishi)	8790124
4	8	Screw, #6-32 x 1/4" PSL MS	8569218
5	2	Handle, Disk Drive (Tandon)	8719353

Note: For additional breakdown of parts for individual disk drive types, see addendum section at the back of this Model 2000 Service Manual.

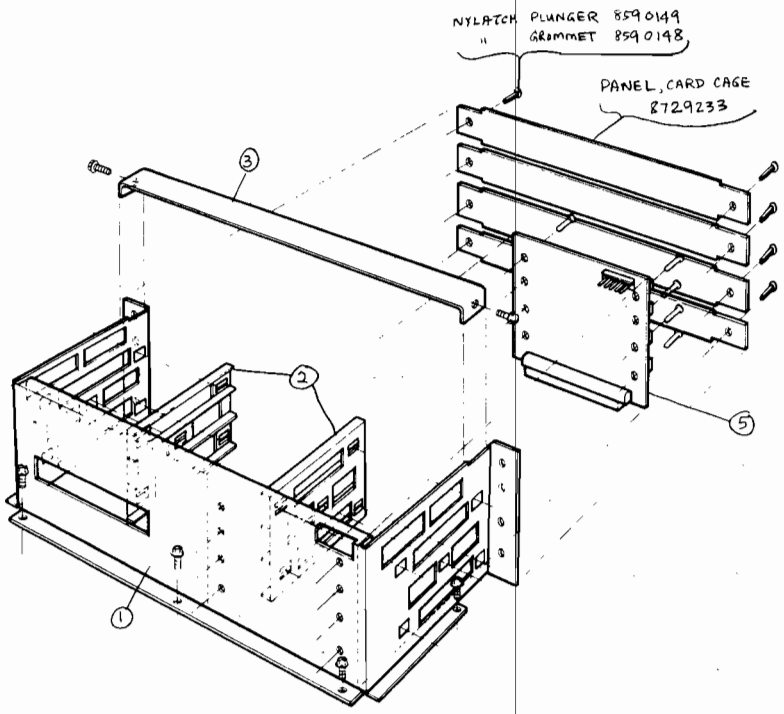


Exploded View, Disk Drive Assemblies

Parts List

Card Cage Assembly, Model 2000 Microcomputer

Item	Sym	Description	Part Number
1	1	Card Cage	8729234
2	2	Guide, Card Cage	8719333
3	1	Brace, Card Cage	8729255
4	1	Motherboard PCB Assembly	8898803
5	8	Screw, #2-56 x 5/16" PPH MS	8569212
6	2	Screw, #6 x 5/16" PSL TCS	8569214

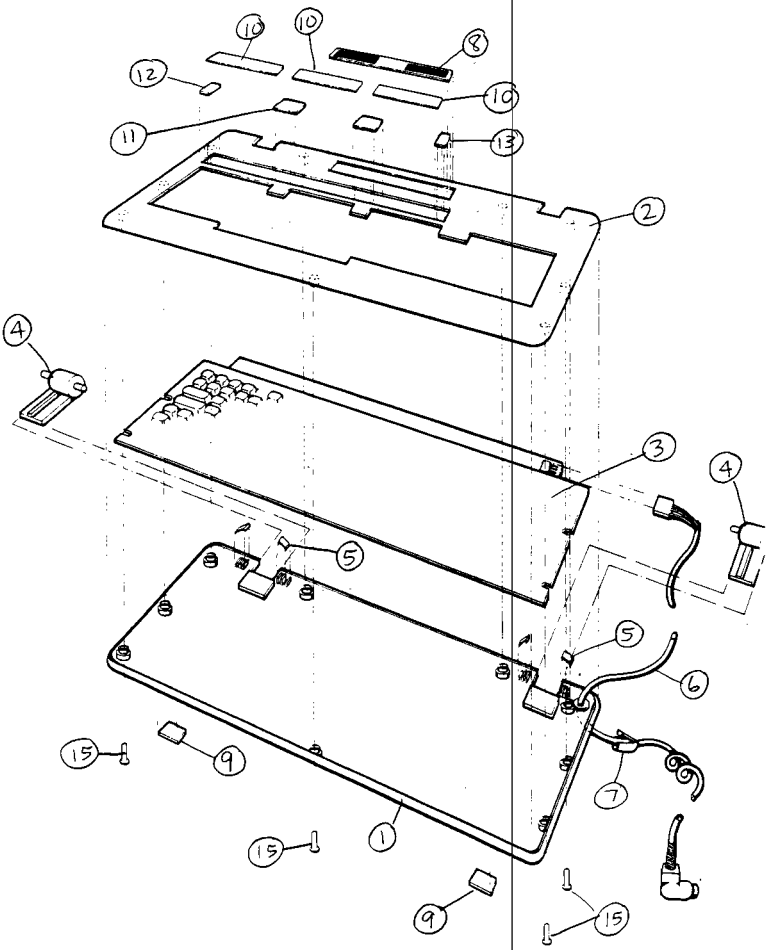


Exploded View, Card Cage Assembly

Parts List

Keyboard Assembly, Model 2000 Microcomputer

Item	Sym	Description	Part Number
1	1	Case, Keyboard Bottom	8719335
2	1	Case, Keyboard Top	8719334
3	1	Keyboard PCB Assembly	8080033
4	2	Support, Keyboard	8719336
5	4	Spring, Keyboard Support	8739014
6	1	Cable Assembly, Keyboard	8709472
7	1	Strain Relief, Cable	8590145
8	1	Logo	8719329
9	2	Pad, Keyboard Friction	8591004
10	3	ID Card, Function Key	87891012
11	1	Center Guide, ID Card	8719371
12	1	Left Guide, ID Card	8719373
13	1	Right Guide, ID Card	8719372
14	4	Screw, #6 x 1/2" PPH PTF Zn	8569079
15	5	Screw, #6 x 7/16" PPH PTF Zn	8569229



Exploded View, Keyboard Assembly

8.3 Display Unit

For the exploded view/parts listing for the display monitor,refer to the addendum sections to the Model 2000 computer. These sections contain detailed exploded views and parts list for both the monochrome and color monitor.

9.1 Internal 128K Expansion RAM

9.1.1 Introduction

The standard 128K word memory capacity of the Model 2000 may be extended to 256K words without using any option card slots by the addition of the 128K word Internal Expansion RAM board. This board is configured, with parity, to reside from address 20000H to 3FFFFH.

9.1.2 Theory Of Operation

There are eighteen high speed dynamic Random Access Memories (RAM's) on the 5.8 inch by 2.5 inch printed circuit board which makes up the Internal Expansion RAM board. Each RAM device is organized as 65,536 one bit words with a maximum access time of 150 nanoseconds. Bulk decoupling of the +5 volt power bus to the RAM's is provided by 100 microfarad, 6.3 volt dipped tantalum electrolytic capacitors. Also, each device is decoupled with a 0.1 microfarad capacitor across its Vcc (pin 8) and ground (pin 16) pins.

Interface to memory control and timing logic is accomplished through 40-pin right angle pin header (J13) on the Internal Expansion RAM board which mates with the right angle receptacle (P13) on the System RAM board. The following table defines the pin assignments on the interface connector (J13).

9.1.3 Signal Definition

The following list defines each signal available on the Internal Expansion RAM connector. For specific memory control and timing specifications see section 7.5.

WORD SEGMENT	UPPER	LOWER
Column Address Select	CASU*	CASL*
Data Input Parity	DIPU	DIPL
Data Output Parity	DOPU	DOPL
Write Input	WR1*	
Row Address Select	RAS1*	
8-bit Memory Address Bus	DMEMA00-DMEMA07	
16-bit Memory Data Bus	IB00-IB15	

9.1.4 Troubleshooting

Memory Read or Write errors can be determined by using the memory diagnostic routines that are available for the Model 2000.

After iniatilizing the test program, a top of memory algorithm is executed to determine how much memory has been installed in the Model 2000 under test. If the response to the memory size inquiry does not agree with the amount of memory the user has installed, it can be assummed that either the memory installation was not performed correctly or the memory boards installed are defective. The user should check all connectors to insure proper and complete mating before attempting to isolate a defective board and/or component.

Once the user is confident of the installation integrity, the memory diagnostic test may be run. There are three tests that are available: a read/write data test; a long modified address test and a short modified address test.

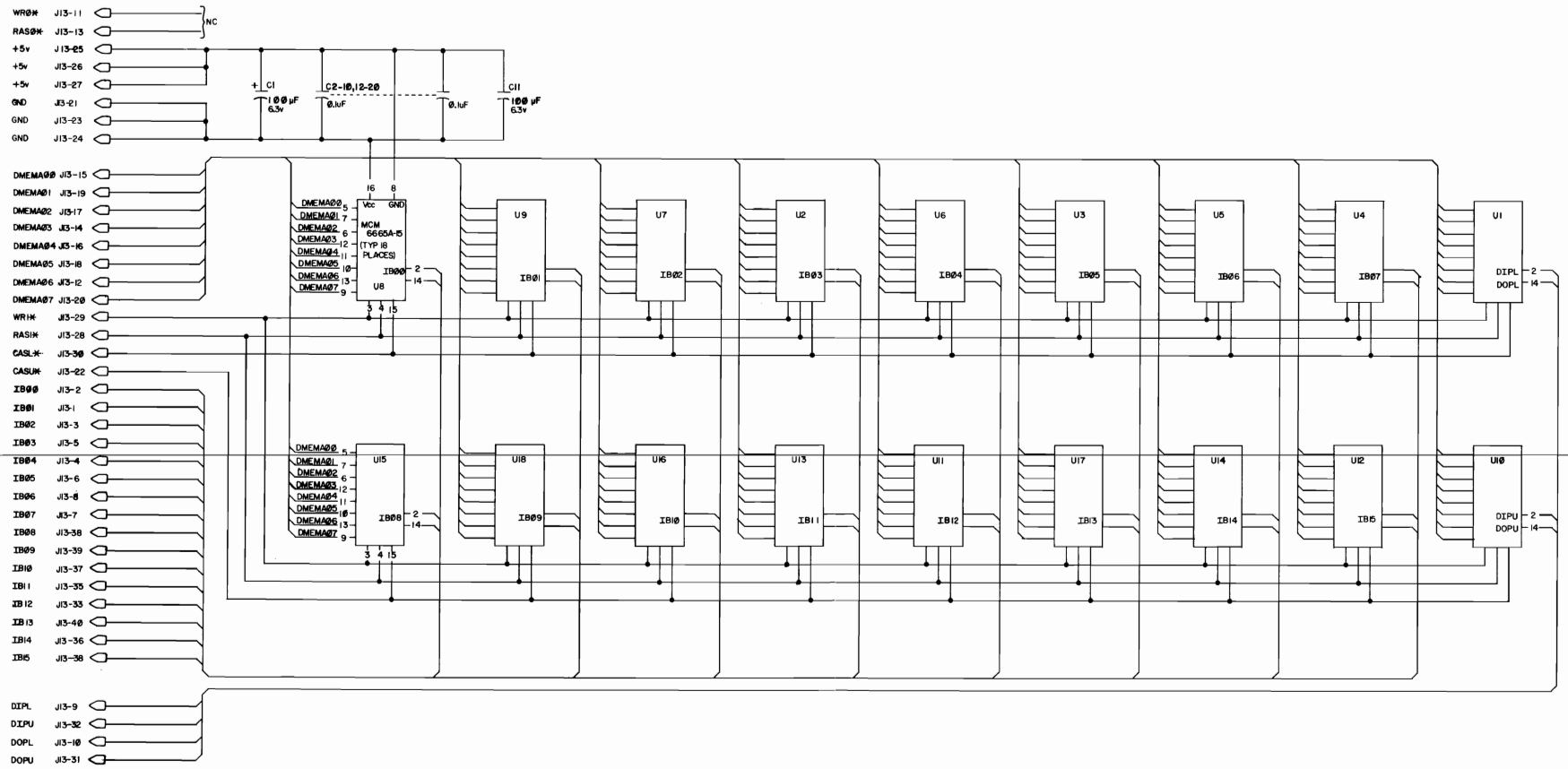
The data test writes a known data pattern to all memory locations. The data is then read back and compared to the known data pattern for errors. Errors generated by this test would indicate a problem either on the data/address bus interface to memory or with the decoders associated with the memory array.

The modified address test has two versions: the long test will test the RAM 65,536 times per pass (0000H-FFFFH) and the short test will test the RAM 256 times per pass (0000-00FF). The number of tests per pass is determined by a 16-bit mask register which is incremented by one for each write/read cycle through the entire memory array (i.e., 00000H-7FFFFH for 512K). The data pattern that is written is the result of the exclusive-OR of the high address segment register (16-bit) with the result of the exclusive-OR of the lower address segment or offset (16-bit) and the mask register. This data pattern is written through the memory array and then read and compared to check for accuracy. Errors that occur will be listed individually in the error table that specifies the data written, the data read, the exclusive-OR of the data written and the data read, and the address where the error occurred. In most cases, this will indicate which RAM chip in a particular bank has failed.

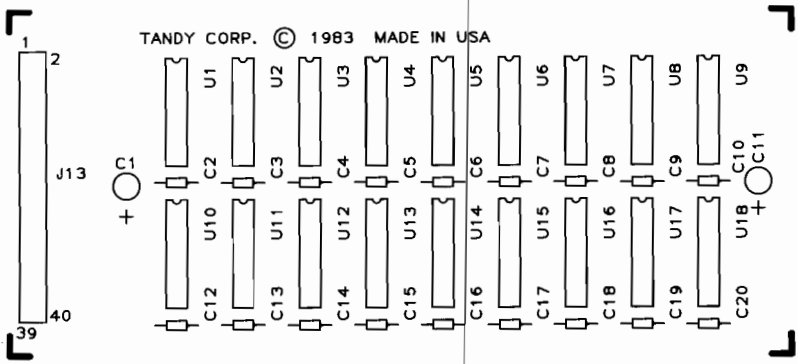
It is recommended that all three RAM tests should be used to verify correct operation of the RAM installed in the unit. Although these tests do not exercise every combination of bits that can be written throughout the full RAM capacity, they exercise enough write/read operations to achieve a fairly reliable test of memory I/O and data recovery to isolate most common memory failures. A complete test that exercises every bit in an array is impractical because of the extreme number of bit combinations, especially in larger memory arrays. For a 16-bit system, there are $16(2^n)$ combinations, where n equals the memory size (e.g., 128K,256K,512K), that must be written, read and compared to complete the full test. In comparison, the modified address method reduces the amount of time it takes to complete a pass but even the long modified address test on a 512K memory array will take approximately 30 hours to complete.

PIN #	SIGNAL	PIN #	SIGNAL
01	IB01	02	IB00
03	IB02	04	IB04
05	IB03	06	IB05
07	IB07	08	IB06
09	DIPL	10	DOPL
11	NO CONNECTION	12	DMEMA06
13	NO CONNECTION	14	DMEMA03
15	DMEMA00	16	DMEMA04
17	DMEMA02	18	DMEMA05
19	DMEMA01	20	DMEMA07
21	GROUND	22	CASU*
23	GROUND	24	GROUND
25	+5 VOLTS	26	+5 VOLTS
27	+5 VOLTS	28	RAS1*
29	WR1*	30	CASL*
31	DOPU	32	DIPU
33	IB12	34	IB15
35	IB11	36	IB14
37	IB10	38	IB08
39	IB09	40	IB13

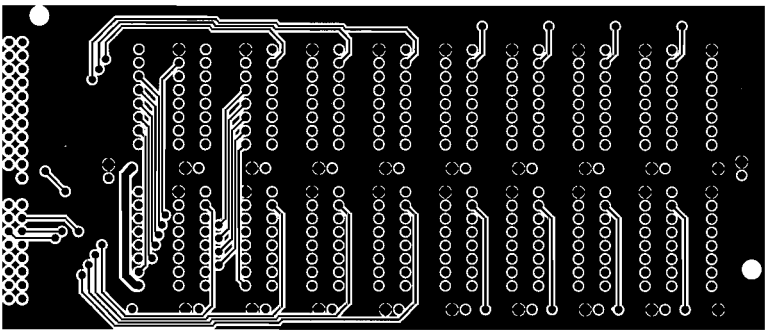
TABLE 1. J13 PIN ASSIGNMENTS
INTERNAL EXPANSION RAM TO SYSTEM RAM INTERFACE



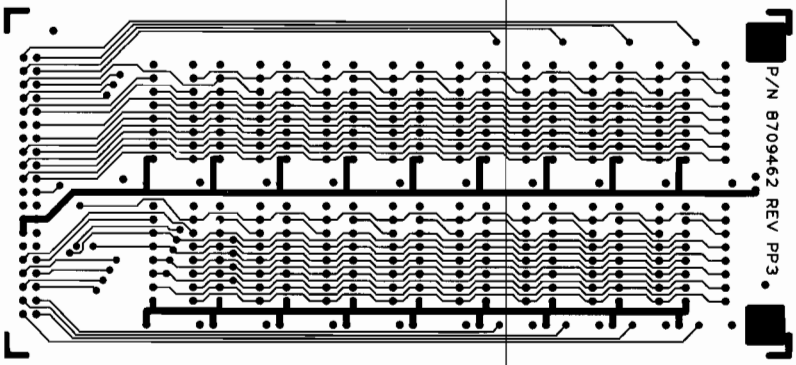
Schematic 8000205, 128K Internal RAM Expansion PCB



Component Layout 1700252, Internal RAM Expansion PCB



Circuit Trace 1700252, 128K Int RAM PCB
Component Side



Circuit Trace 1700252, 128K Int RAM PCB
Circuit Side

9.2 External Memory Board

The Model 2000 Expansion Memory Board (EXP MEM BD) is an optional plug-in board. Each board provides either 128K or 256K bytes of memory. The Model 2000 will accommodate up to three of these boards: two with a maximum of 256K bytes and the third with 128K bytes. This will bring the total Model 2000 RAM capacity to 896K bytes. Some features of the Exp Memory Board are independent on-board refresh control, delay line timing control, and byte-wide single-bit error detection. The block diagram of the EXP MEM BD is shown in Figure 9-1.

9.2.1 Memory Array

The memory array is made up of 64K x 1 Dynamic RAM ICs with 150 nanosecond access time. These RAM ICs are arranged into four groups of 9 ICs each; low word - high and low byte, and high word - low and high byte (see Figure 9-1). In each of the four groups, eight of the RAMs are for the stored data and one is for the error detection or parity bit. The data bus groups together the two high bytes D8 - D15 and the two low bytes D0 - D7. Each byte group has its own Model 2000 / Ext Memory Board interface. This conforms to the Model 2000 Bus / 80186 architectural feature of byte accesses. Physically, the internal data bus is accomplished by connecting the corresponding bits of each byte together. Additionally, the input and output data pins of each individual RAM IC are connected together. (This is allowed because single operation accesses only are allowed). The interface circuity consists of input buffers and output latches. Latching the output data prevents the stretching of the internal READ cycle until the CPU is complete and therefore allows the read and write cycles to be of equal length. And, most importantly, it allows refresh cycles to be added to any CPU access by inserting wait states.

9.2.2 Address Logic

The EXP MEM BD uses all twenty address bits of the Model 2000 bus, A0 thru A19. A19 and A18 are used for board selection, A17 is used for word selection, A16 thru A1 are the RAM address inputs, and A0, in conjuction with BHE (80186 signal), is used for byte selection.

A19,A18

These two address bits are used by the Model 2000 to decode which group of four 256K bytes (128K words) is being accessed. On the EXP MEM BD, they generate the signal SELECT. The circuit consists of U64 (a 74F138 3-to-8 decoder) used as a 2-to-4 decoder. A18 and A19 are the decoded inputs and MC0, MC1 (80186 memory chip selects) are the enables. Three of the four possible decoded outputs are provided as jumper selectable outputs - B1, B2, and B3. One of the jumper options has to be made before the board will operate. For the first board in the system, the jumper must be between B2 and S; for the second board between B3 and S, and for the third board between B1 and S. See Figure 9-2 for more details.

A17

This address bit is combined with the RAM row address strobe RASP to select either the array high word (A17 true) or the array low word (A17 false). This takes place at U15.

A16 thru A1

These address bits are used by the RAM ICs to decode one of 64K internal memory locations. The RAM ICs, due to the number of pins, require the address bits to be divided into two groups and the groups loaded sequentially. These two groups are ROW address (loaded first) and COLUMN address (loaded second). The circuit that accomplishes this is composed of line receivers U68, U70 (74LS244s), and 2-to-1 multiplexers U67 and U69 (74F258s). The line receivers are always enabled. The multiplexers are enabled when ENRCAD* is true (low). The address group applied to the RAMs is determined by the logic level of MUX* - low (normal state) for row address, high (active state) for column address. The outputs of the decoders are routed to the RAM array through damping resistors (RP4). These resistors are shared by refresh address buffer U66.

9.2.3 Refresh Address

The 256 refresh address combinations are generated by an eight-bit counter U72. The clock for this counter is RFCNT* which occurs at the end of each refresh cycle. The counter works in the continuous mode, i.e. the counter counts 0, 1, ..254, 255, 0,..etc. The refresh address buffer U66 applies the current count to the array via the damping resistors RP4 when it is enabled by ENRFAD* being true (low) (ENRCAD will be false).

9.2.4 Memory Control

The Memory Control logic generates all the timing clocks/control strobes to access the memory, refresh the memory, and generate/check parity. A general description of the operational characteristics of the EXT MEM BD will set the stage for the more detailed individual circuit analysis that follows.

First, the EXT MEMORY BOARD has three modes of operation:

9.2.4.1 Memory access without refresh.

This mode has two variants. If it is a video access, refresh is inhibited. If it is a CPU access and CNT = 0, no refresh is required. RDY is set immediately.

9.2.4.2 Memory access with refresh

In this mode, the memory access is performed first and then followed by 1 to 16 refresh cycles. This is accomplished by holding the RDY cleared until the last refresh cycle and extending the CPU access. If it is a READ access, the output data is latched for the CPU at the end of the first cycle. (This is because the CPU will not READ the data until RDY is set).

9.4.2.3 Refresh only

In this mode, a memory access is taking place at an off-board memory location but a refresh cycle(s) is required. Therefore, a single refresh cycle is performed in parallel to the other access. Only a single refresh cycle is allowed because the RDY line cannot be controlled. The timing cycle for a read, write or refresh is the same. Only the decoded timing strobes are different. For instance, the difference between a read and a write is the presence of the write strobe to the array and the direction of the data flow. A refresh cycle inhibits CAS and selects the refresh address instead of the CPU addresses. A RAS only cycle is a refresh cycle to the RAM and no data is affected. A block diagram of the memory controller is shown in Figure 9-3.

GLOSSARY OF TERMS

The following will be helpful in understanding the remaining discusion.

RAS0* = Row Address Strobe for lower word. A17=0.
= RASP * A17/ + RFRAS
RAS1* = Row Address Strobe for upper word. A17=1.
= RASP * A17 + RFRAS
RASP = Row Address Strobe Prime. Basic strobe for RAS,RAS1.
RFRAS* = ReFresh RAS. RAS is row address strobe.
CASH* = Column Address Strobe, High byte.
= CASP * BHE
CASL* = Column Address Strobe,Low byte.
= CASP * A0
CASP = Column Address Strobe Prime. Basic strobe for CASH,CASL.
MUX* = Row column address select.
WRITEH* = WRITE strobe,High byte.
WRITEL* = WRITE strobe,Low byte.
WRITEP* = Write Prime.
LRFSH = Latched Refresh. Indicates the current timing cycle is for refresh.
ENRCAD* = ENable Row Column ADdress. Goes to U67, U69.

ENRFAD* = ENable ReFresh ADdress. Goes to U66.
RASCLR* = RAS CLeaR. Terminates RASP.
RFSRT* = ReFresh StaRT. Restarts a timing cycle.
RFCNT* = ReFresh cycle CouNT. Counts down CNT.
CNT = Refresh cycles due CouNT.
SCNT = Synchronized CNT.
STROBE* = parity interrupt timing strobe.
SELECT = board SELECTed by address. Access starts when MREAD or MWRITE occur.
PARH = PARity High. Parity has occurred on high byte.
PARL = PARity Low. Parity has occurred on low byte.

9.2.5 Timing Sequence Generator

The timing sequence generator consists of delay lines U32, U49, half the J-K flip-flop U48, and the AND-OR gate U47. The timing sequence is started by triggering the flip-flop by the leading edge of the signal MEMCYC. This sets Q low. This low appears 80 nanoseconds later from the delay line at the clear of the flip-flop and sets Q high. Thus, an 80 nanosecond negative pulse is initiated down the delay line, creating a series of timing pulses - once. If the conditions are right, a short pulse RFSRT is created at the 300 nanosecond tap to begin the cycle over.

The signal MEMCYC/ is created under two conditions. The first is a memory access - that is, SELECT, MREAD and MWRITE are true.

The second condition is the need for a refresh cycle. If SCNT is true but SELECT is false, the next MREAD or MWRITE creates a MEMCYC. The signal RFSRT will add cycles to the original cycle if and only if SELECT is true and as long as SCNT is true. These added cycles are refresh cycles and can be added only if the signal BUSARDY (CPU "wait") can be controlled.

9.2.6 Refresh Counter

The refresh method is basically a single cycle every 16 microseconds. The exception is that the refresh cycles are allowed to stack up until a convenient time when a refresh burst occurs that is equal in number to the deficit amount. The refresh counter circuitry consists of the refresh period counter U45, U61, and the deficit counter U27, U11, and 1/6 of U46. The refresh counters U45 and U61 provide a constant time tick (125 nanosecond negative pulse) every 16.0 microseconds to U27. This causes U27 to count up. Every time a refresh cycle is performed, a signal RFCNT is applied which causes U27 to count down. The CNT logic U11 samples the output of U27 and, if the count is greater than zero, CNT is true.

9.2.7 Refresh Count Synchronizer

The output signal from the refresh counter CNT needs to be synchronized with MREAD or MWRITE to prevent CNT from affecting the access status after the cycle has started (RDY already set). This is accomplished by the two flip-flops

U28(1/2), U12(1/2), 3/4 U13, 1/4 U29, and 1/6 U65. Working backward, the output SCNT is the logical AND of the synchronized CNT (U29.11) and the enable RFINH/ (refresh inhibit- refresh not allowed during video accesses). The synchronized CNT signal is the logical OR of two versions of synchronized CNT - one that is latched and one that reflects the real time status of CNT. The latched version of CNT is required so that SCNT becomes true only between memory cycles. Once a refresh cycle is started, denoted by the presence of LRFSH (latched refresh), the latched version of CNT is cleared and replaced by the real-time version which will allow SCNT to go false when CNT = 0. (The latched version will not update until next ALE which will not occur until CNT = 0 which allows the memory access cycle to finish and proceed to the next ALE). There are two latches instead of one because of the special sequence where a non-SELECTed refresh cycle preceeds a normal access. In this case, the delayed strobe D300 is active when the new access is started. This causes the decoder to latch a refresh cycle and hang-up the sequence by failing to set RDY. By making the sync chain two flip-flops, only alternate bus accesses can cause a refresh cycle.

9.2.8 Decoder

The decoder accepts the input timing signals from the timing generator and the status signals and creates the timing strobes for the MEMORY TIMING LOGIC. The decoders U30, U31, U42, and part of U71 are programmable logic arrays and contain proprietary information. Timing diagrams are shown in Figure 9-4.

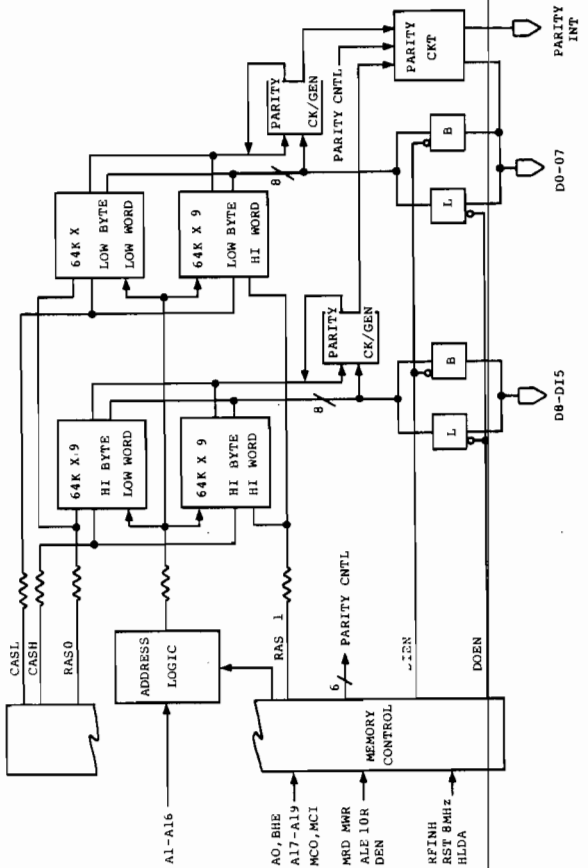


Figure 9-1. Block Diagram, External Memory Board

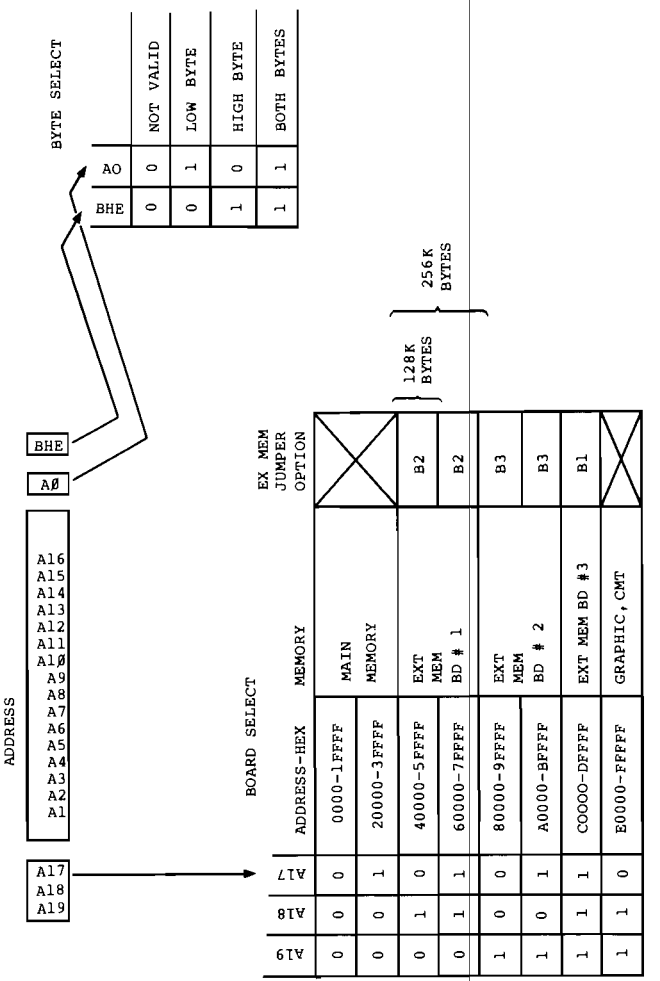


Figure 9-2. Board Select

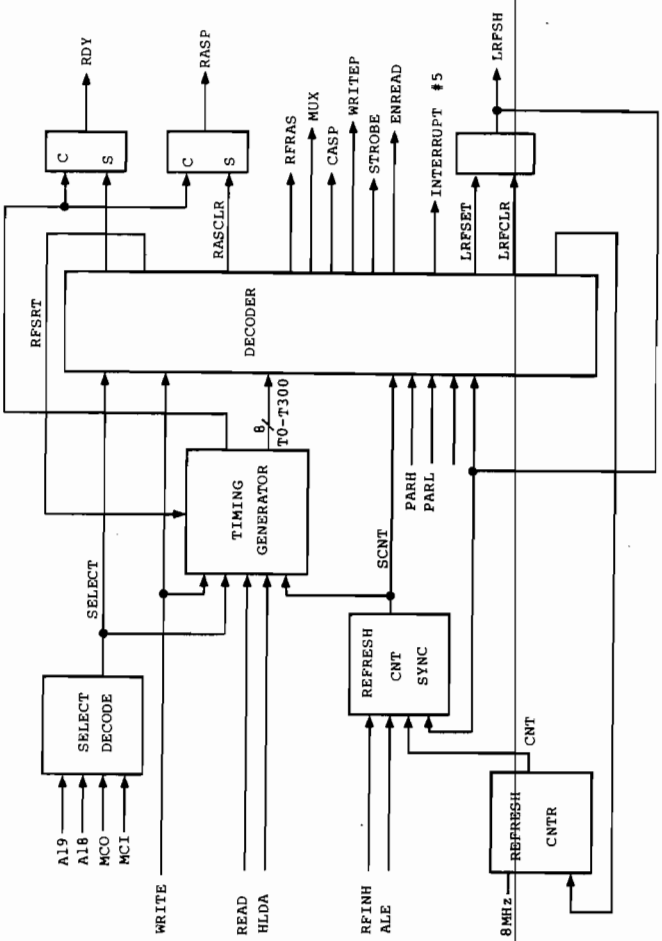


Figure 9-3. Memory Control Block Diagram

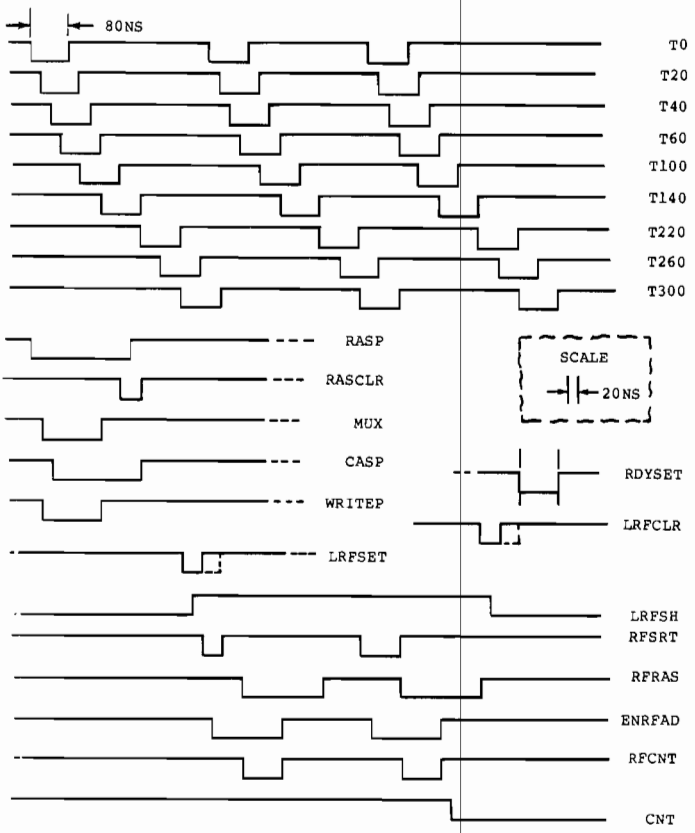


Figure 9-4. Normal Cycle Plus Refresh Cycle

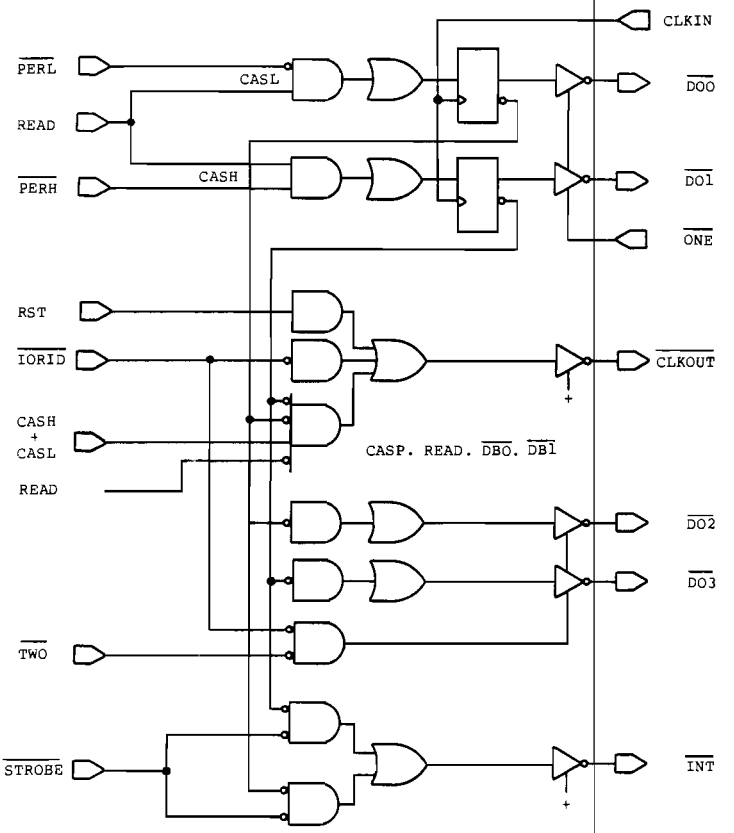
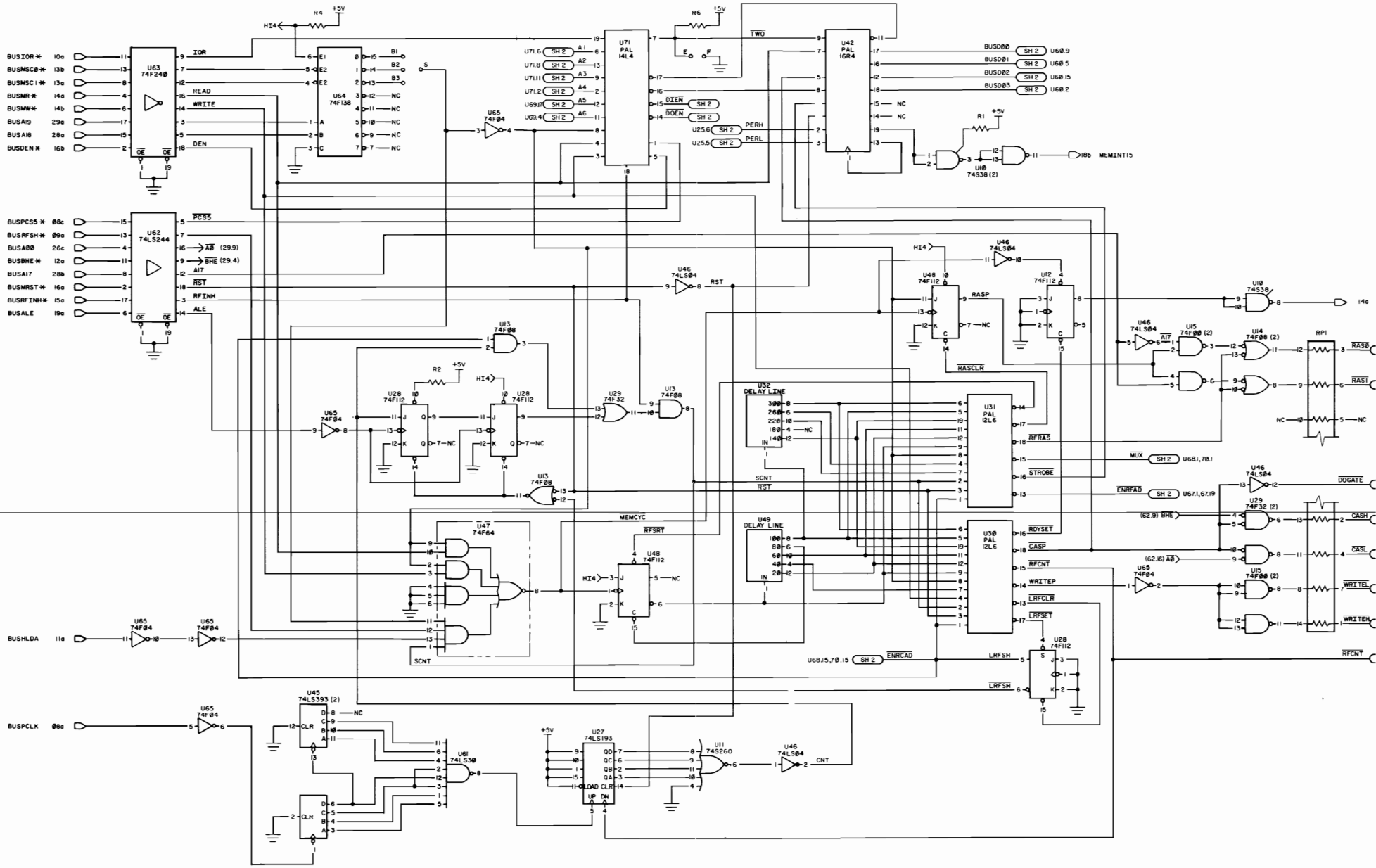
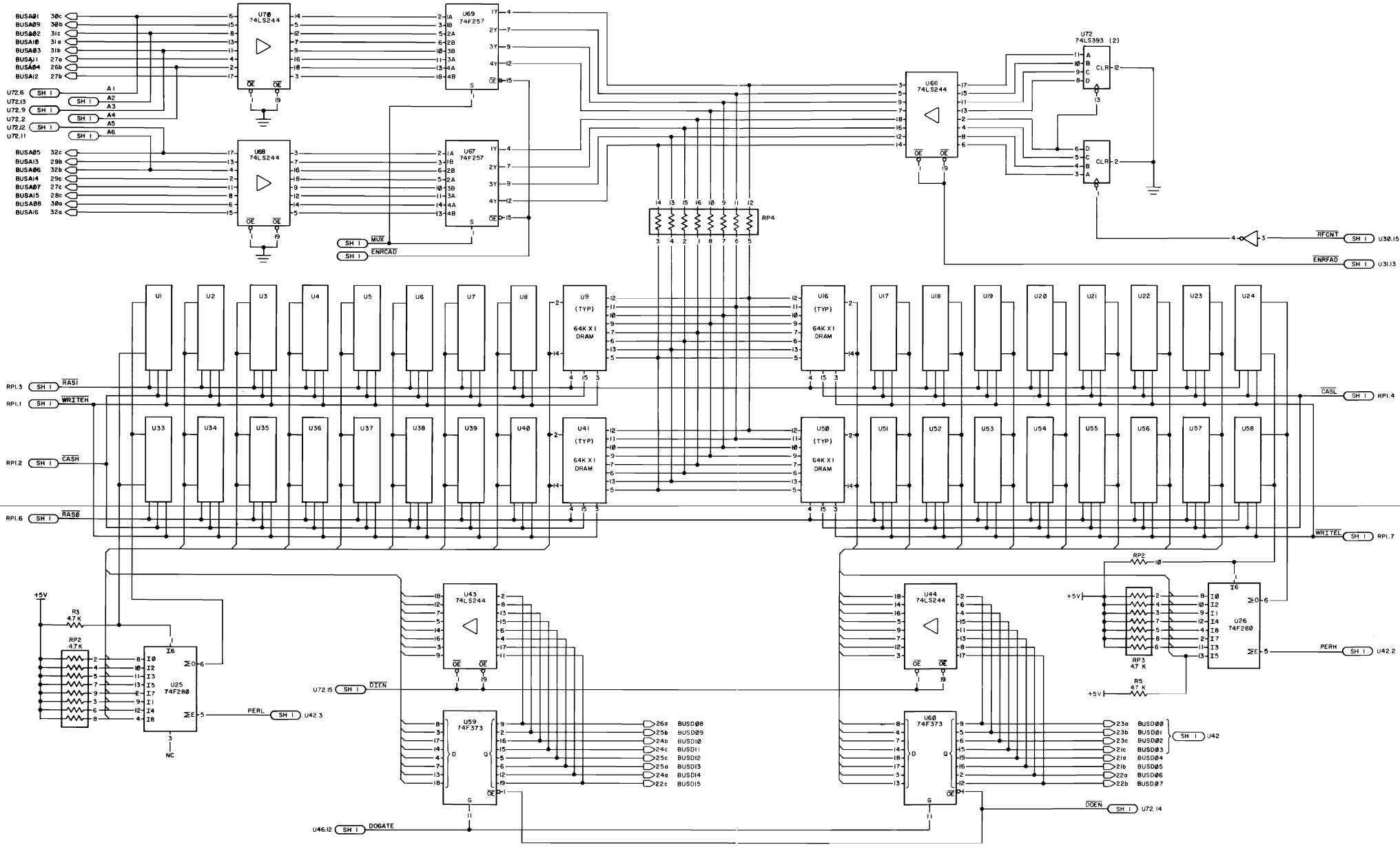


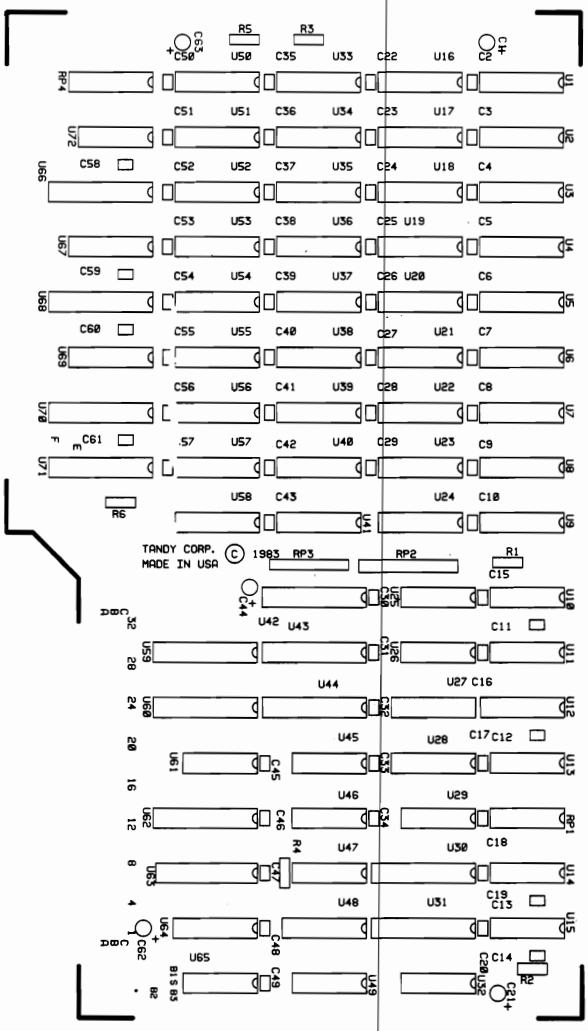
Figure 9-5. U42 Diagram



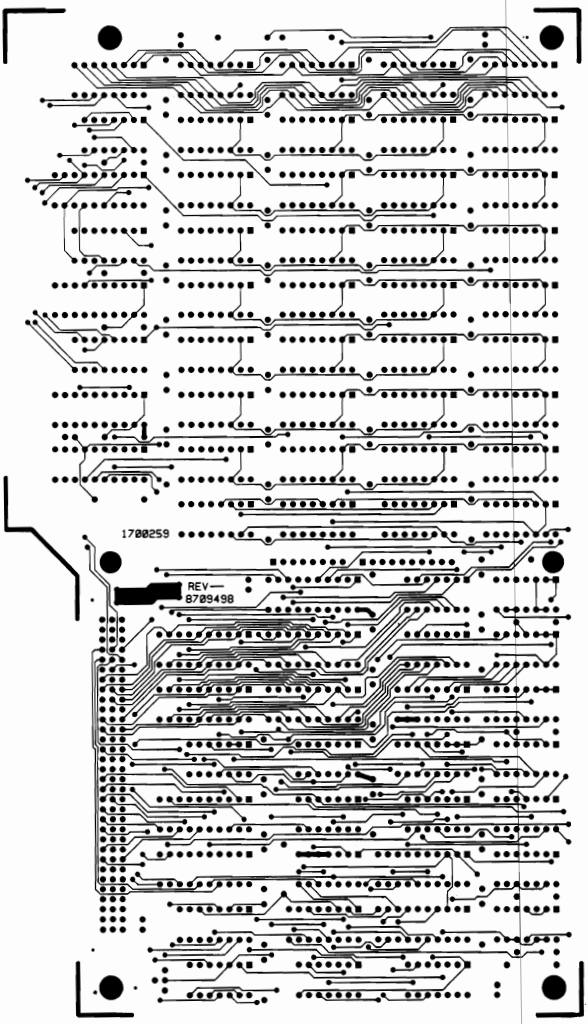
Schematic 8000218, 128/256K External RAM PCB Block Diagram
Page 1 of 2



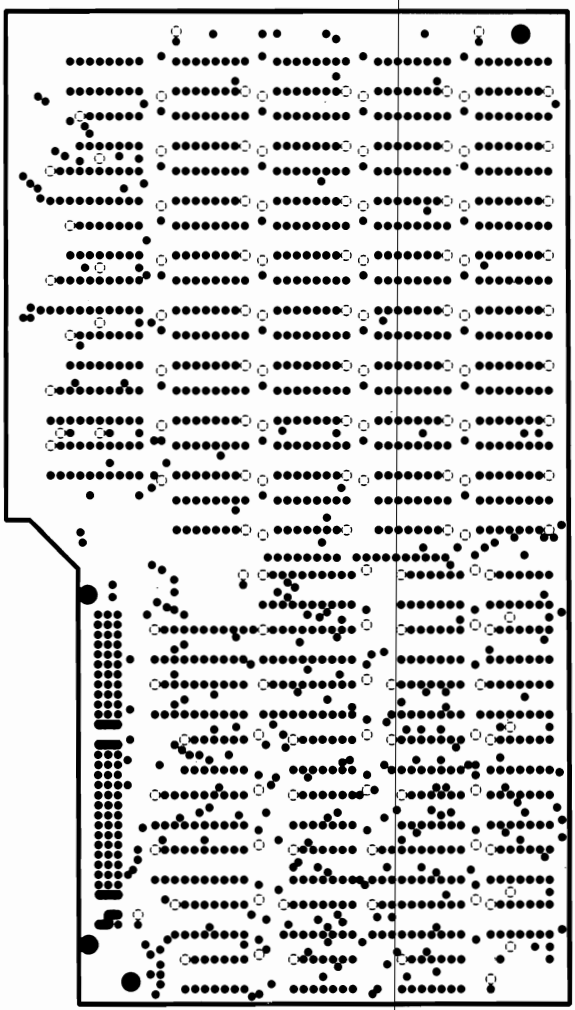
Schematic 8000218, 128/256K External RAM PCB Block Diagram
Page 2 of 2



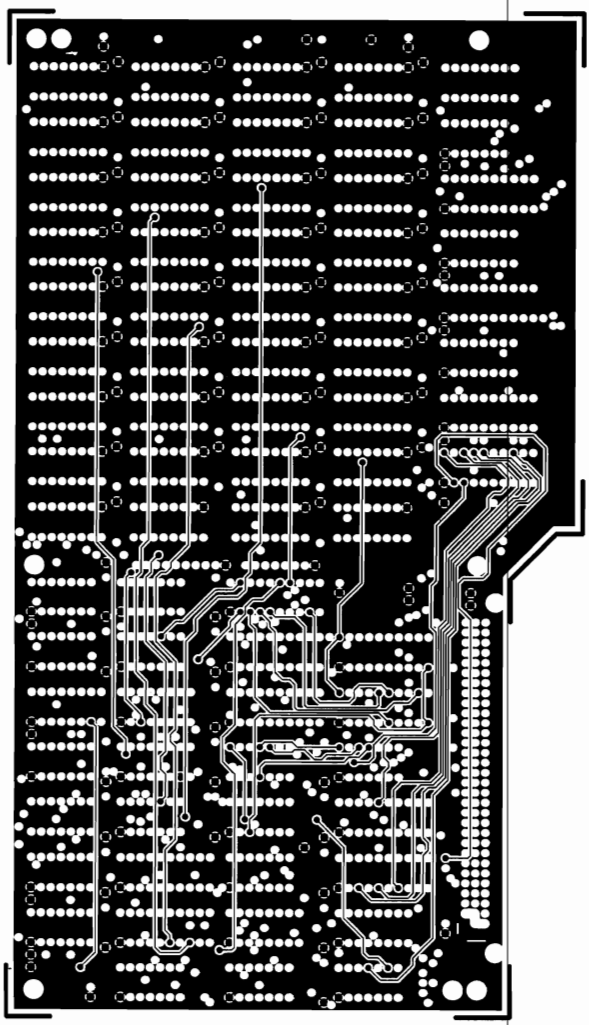
Component Layout, External 256K RAM Memory Expansion 889B011



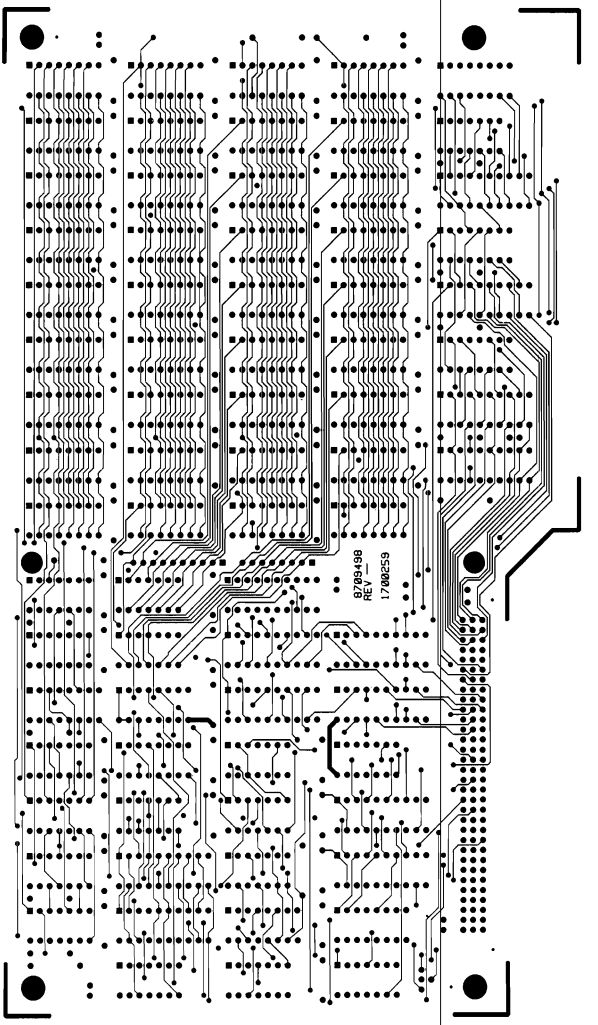
Circuit Trace, External 256K RAM PCB Assembly 889B011
Component Side



Circuit Trace, External 256K RAM PCB 899B011
Ground Plane



Circuit Trace, External 256K RAM PCB Assembly 889B011
Power Plane



Circuit Trace, External 256K RAM PCB Assembly 889B011
Component Side

Parts List - 26-5161 External RAM Board (11-14-83)

PCB 889B011 256K Board Populated with 128K

Item	Sym	Description	Part Number
1	1	External 256K Logic PCB	8709498
2	6	Staking Pins, A thru F	8529014
3	36	Socket, 16-Pin DIP (U1-9,16-24, 33-41,50-58)	8509003
4	4	Socket, 20-Pin DIP (U30,31,42,71)	8509009
5	1	Connector, 96 Pin Euro Female (J1)	8519181
6	2	Screw, #2-56 x 3/8" PPH (J1)	8569201
7	2	Nut, #2-56 (J1)	8579042
8	1	Chassis, 128/256K Memory	8729278
9	2	Nylatch Plunger	8590149
10	2	Nylatch Grommet	8590148
11	6	Screw, #4-40 x 3/16" PPH MS	8569220
12	1	Label, Serial	87891041
	C1	Capacitor, 100 mfd, 6.3V Tant. Rad.	8337100
	C2	Capacitor, .1 mfd, 50V Mono	8374101
	C3	Capacitor, .1 mfd, 50V Mono	8374101
	C4	Capacitor, .1 mfd, 50V Mono	8374101
	C5	Capacitor, .1 mfd, 50V Mono	8374101
	C6	Capacitor, .1 mfd, 50V Mono	8374101
	C7	Capacitor, .1 mfd, 50V Mono	8374101
	C8	Capacitor, .1 mfd, 50V Mono	8374101
	C9	Capacitor, .1 mfd, 50V Mono	8374101
	C10	Capacitor, .1 mfd, 50V Mono	8374101
	C11	Capacitor, .1 mfd, 50V Mono	8374101
	C12	Capacitor, .1 mfd, 50V Mono	8374101
	C13	Capacitor, .1 mfd, 50V Mono	8374101
	C14	Capacitor, .1 mfd, 50V Mono	8374101
	C15	Capacitor, .1 mfd, 50V Mono	8374101
	C16	Capacitor, .1 mfd, 50V Mono	8374101
	C17	Capacitor, .1 mfd, 50V Mono	8374101
	C18	Capacitor, .1 mfd, 50V Mono	8374101
	C19	Capacitor, .1 mfd, 50V Mono	8374101
	C20	Capacitor, .1 mfd, 50V Mono	8374101
	C21	Capacitor, 100 mfd, 6.3V Tant. Rad.	8337100
	C22	Capacitor, .1 mfd, 50V Mono	8374101
	C23	Capacitor, .1 mfd, 50V Mono	8374101
	C24	Capacitor, .1 mfd, 50V Mono	8374101
	C25	Capacitor, .1 mfd, 50V Mono	8374101
	C26	Capacitor, .1 mfd, 50V Mono	8374101
	C27	Capacitor, .1 mfd, 50V Mono	8374101
	C28	Capacitor, .1 mfd, 50V Mono	8374101

Parts List - 26-5161 External RAM Board

PCB 889B011 256K Board Populated with 128K

Item	Sym	Description	Part Number
	C29	Capacitor, .1 mfd, 50V Mono	8374101
	C30	Capacitor, .1 mfd, 50V Mono	8374101
	C31	Capacitor, .1 mfd, 50V Mono	8374101
	C32	Capacitor, .1 mfd, 50V Mono	8374101
	C33	Capacitor, .1 mfd, 50V Mono	8374101
	C34	Capacitor, .1 mfd, 50V Mono	8374101
	C35	Capacitor, .1 mfd, 50V Mono	8374101
	C36	Capacitor, .1 mfd, 50V Mono	8374101
	C37	Capacitor, .1 mfd, 50V Mono	8374101
	C38	Capacitor, .1 mfd, 50V Mono	8374101
	C39	Capacitor, .1 mfd, 50V Mono	8374101
	C40	Capacitor, .1 mfd, 50V Mono	8374101
	C41	Capacitor, .1 mfd, 50V Mono	8374101
	C42	Capacitor, .1 mfd, 50V Mono	8374101
	C43	Capacitor, .1 mfd, 50V Mono	8374101
	C44	Capacitor, 100 mfd, 6.3V Tant. Rad.	8337100
	C45	Capacitor, .1 mfd, 50V Mono	8374101
	C46	Capacitor, .1 mfd, 50V Mono	8374101
	C47	Capacitor, .1 mfd, 50V Mono	8374101
	C48	Capacitor, .1 mfd, 50V Mono	8374101
	C49	Capacitor, .1 mfd, 50V Mono	8374101
	C50	Capacitor, 100 mfd, 6.3V Tant. Rad.	8337100
	C51	Capacitor, .1 mfd, 50V Mono	8374101
	C52	Capacitor, .1 mfd, 50V Mono	8374101
	C53	Capacitor, .1 mfd, 50V Mono	8374101
	C54	Capacitor, .1 mfd, 50V Mono	8374101
	C55	Capacitor, .1 mfd, 50V Mono	8374101
	C56	Capacitor, .1 mfd, 50V Mono	8374101
	C57	Capacitor, .1 mfd, 50V Mono	8374101
	C58	Capacitor, .1 mfd, 50V Mono	8374101
	C59	Capacitor, .1 mfd, 50V Mono	8374101
	C60	Capacitor, .1 mfd, 50V Mono	8374101
	C61	Capacitor, .1 mfd, 50V Mono	8374101
	C62	Capacitor, .1 mfd, 50V Mono	8374101
	C63	Capacitor, 100 mfd, 6.3V Tant. Rad.	8337100
	R1	Resistor, 1 kohm, 1/4W 5%	8207210
	R2	Resistor, 1 kohm, 1/4W 5%	8207210
	R3	Resistor, 4.7 kohm, 1/4W 5%	8207247
	R4	Resistor, 1 kohm, 1/4W 5%	8207210
	R5	Resistor, 4.7 kohm, 1/4W 5%	8207247
	R6	Resistor, 1 kohm, 1/4W 5%	8207210

Parts List - 26-5161 External RAM Board

PCB 889B011 256K Board Populated with 128K

Item	Sym	Description	Part Number
	RP1	Resistor Pak, 56 ohm, 14-Pin DIP	8
	RP2	Resistor Pak, 4.7 kohm, 10-Pin SIP	8294247
	RP3	Resistor Pak, 4.7 kohm, 8-Pin SIP	8292246
	RP3	Resistor Pak, 27 ohm, 16-Pin DIP	8290027
	U10	IC, 74S38, Quad 2-Input NAND	8010038
	U11	IC, 74S260, Dual 5-Input NOR	8010260
	U12	IC, 74F112, Flip-Flop	8015112
	U13	IC, 74F08, Quad 2-Input AND	8015008
	U14	IC, 74F08, Quad 2-Input AND	8015008
	U15	IC, 74F00, Quad 2-Input NAND	8015000
	U25	IC, 74S280, Parity Generator	8010280
	U26	IC, 74S280, Parity Generator	8010280
	U27	IC, 74ALS193, Counter	8025193
	U28	IC, 74F112, Flip-Flop	8015112
	U29	IC, 74F32, Quad 2-Input OR	8015032
	U30	IC, PAL12L6	8040126
	U31	IC, PAL12L6	8040126
	U32	IC, Delay Line, 200 nsec	8429010
	U33	IC, 6665-150, DRAM	8041665
	U34	IC, 6665-150, DRAM	8041665
	U35	IC, 6665-150, DRAM	8041665
	U36	IC, 6665-150, DRAM	8041665
	U37	IC, 6665-150, DRAM	8041665
	U38	IC, 6665-150, DRAM	8041665
	U39	IC, 6665-150, DRAM	8041665
	U40	IC, 6665-150, DRAM	8041665
	U41	IC, 6665-150, DRAM	8041665
	U42	IC, PAL16R4	8040164
	U43	IC, 74ALS244, Octal Buffer	8025244
	U44	IC, 74ALS244, Octal Buffer	8025244
	U45	IC, 74LS393, Counter	8020393
	U46	IC, 74LS04, Hex Inverter	8020004
	U47	IC, 74F64, AND-OR Inverter	8015064
	U48	IC, 74F112, Flip-Flop	8015112
	U49	IC, Delay Line 100 nsec	8429024
	U50	IC, 6665-150, DRAM	8041665
	U51	IC, 6665-150, DRAM	8041665
	U52	IC, 6665-150, DRAM	8041665
	U53	IC, 6665-150, DRAM	8041665
	U54	IC, 6665-150, DRAM	8041665
	U55	IC, 6665-150, DRAM	8041665

Parts List - 26-5161 External RAM Board

PCB 889B011 256K Board Populated with 128K

Item	Sym	Description	Part Number
	U56	IC, 6665-150, DRAM	8041665
	U57	IC, 6665-150, DRAM	8041665
	U58	IC, 6665-150, DRAM	8041665
	U59	IC, 74F373, Octal Latch	8015373
	U60	IC, 74F373, Octal Latch	8015373
	U61	IC, 74LS30, 8-Input NAND	8020030
	U62	IC, 74LS244, Octal Buffer	8025244
	U63	IC, 74F240, Octal Buffer	8015240
	U64	IC, 74F138, Decoder	8015138
	U65	IC, 74F04, Hex Inverter	8015004
	U66	IC, 74LS244, Octal Buffer	8025244
	U67	IC, 74LS257, Multiplexer	8015257
	U68	IC, 74LS244, Octal Buffer	8025244
	U69	IC, 74F257, Multiplexer	8015257
	U70	IC, 74LS244, Octal Buffer	8025244
	U71	IC, PAL14L4	8040104
	U72	IC, 74LS393, Counter	8020393

9.3 Hi-Resolution Graphics Option 640 X 400

The High Resolution (Hi-Res) Graphics option for the Model 2000 provides 640 X 400 pixels on the VM-1 or CM-1 video monitors. The board contains 96K bytes of high speed RAM for storage of graphics data, and a user programmable color palette for color assignment. The board resides in the lower slot of the Model 2000 card cage.

9.3.1 Memory Organization

The graphics memory is organized in a planer fashion. Up to three 16K by 16 memory planes may be installed. If two-color video is required, then PLANE 0 is installed. Installing PLANE 1 and PLANE 2 provides 8-color video.

There is a 6-bit STATUS PORT on the graphics board to inform the programmer how many planes are installed. See STATUS PORT DESCRIPTION for more information.

All three memory planes occupy the same physical address space. To determine which of the three planes the CPU is reading from or writing to, a PLANE SELECT REGISTER must be set up prior to accessing graphics RAM. See the section entitled PLANE SELECT REGISTER (9.3.4).

The memory starts at address E000:0H in the 186 Processor address space. This address corresponds to the UPPER LEFT of the video screen. The next address is to the right. The lower right corner is the last address. The full screen requires 32,000 bytes or 16,000 words to fully describe a single plane. The board responds to both byte and word accesses. Word accesses must be on even addresses only. Either the high byte or the low byte may be transferred during byte accesses.

The graphics memory may be accessed at any time. The Hi-Res circuitry uses WAIT states to synchronize the data transfer between CPU and graphics memory. The average speed at which data may be transferred is 16 bits per microsecond.

9.3.2 Pixel Mapping

Each bit in the graphics memory represents a dot (pixel) on the video screen. The MSB of a byte or word is the LEFTMOST pixel. The LSB is the last pixel to the right.

9.3.3 Color Palette - Changing a Pixel Color

The Hi-Res board contains a high speed static RAM which serves as the color palette. The palette "looks up" a color by forming an address using the data from each installed plane. PLANE 0 is pallette address bit A0, PLANE 1 is palette address bit A1, and PLANE 2 is palette address bit A2. Palette address bit A3 is always tied high, a 1. If a plane is NOT installed, the palette address bit is a 1. Therefore, if PLANE 0 contained a 1, PLANE 1 a 0, and PLANE 2 a 0, the palette would "look-up" the color at address 1001 in the palette memory.

Since there are three memory planes (maximum), there can be up to eight colors displayed at one time on the screen. The CM-1 color monitor can display 15 colors. Therefore, any of the available 15 colors, up to 8 at a time, can be displayed.

The CPU can write the palette to change the color lookup table. The palette is located in the Processor I/O space, and is on word (even address) boundries. The Processor uses PCS3 as the I/O port decode for graphics boards.

The palette appears to the programmer as 16 word addresses, starting at I/O address 0180H. The palette is a WRITE-ONLY device. I/O address 0180H is the first palette address, 0182H the second, etc. Data is stored in the palette on data bits D3-D0. The upper data bits are ignored. Remember that these addresses are not the same as the address formed to "look-up" a color for a particular pixel.

Although a program may access the palette anytime, it is possible to generate an undesirable "tear" or horizontal bar on the screen during a palette write from the CPU. To prevent the video monitor from doing this, the palette must be written to only during vertical blanking time. The SMC9007 Video Controller, used in the Model 2000, has a status register which reflects the status of vertical sync. Also, the 9007 can provide interrupts to the Processor each vertical sync. It is up to the individual programmer as to which is preferred.

The data in the palette is tied to the video guns of the CM-1 color monitor as shown in the table below. As can be seen, D0 controls the blue gun, D1 the green gun, D2 the red gun, and D3 the half intensity. A 1 in D3 is full intensity, a 0 half intensity. The following table shows possible colors versus data bits.

D3	D2	D1	D0	COLOR on CM-1
0	0	0	0	black
0	0	0	1	dark blue
0	0	1	0	dark green
0	0	1	1	dark cyan
0	1	0	0	dark red
0	1	0	1	dark magenta
0	1	1	0	dark yellow
0	1	1	1	gray
1	0	0	0	black
1	0	0	1	blue
1	0	1	0	green
1	0	1	1	cyan
1	1	0	0	red
1	1	0	1	magenta
1	1	1	0	yellow
1	1	1	1	white

I R G B

9.3.4 Plane Select Register

Since the three memory planes the the Hi-Res board occupy the same address space, there must be some way to determine which one the CPU is trying to read from or write to. This is done by writing the proper data into the plane select register.

The plane select register is I/O mapped as address 01A0H. It is WRITE-ONLY. It is 6 bits wide on D0-D5. The register has 3 functions.

First, it selects which plane of memory the CPU has access to. Only one plane at a time may be selected. If more than one plane is selected, the register DESELECTS ALL PLANES.

Second, it determines if the graphics planes are displayed or "turned off". If they are turned off, the address into the palette will be 08H (the plane data forced to 0). This does NOT erase the data in the planes, but simply forces the palette address to see 08H.

Third, it determines if addresses into the palette are from the internal memory planes, or from the 9007 video memory. See DISPLAYING ALPHA-NUMERIC TEXT USING THE HI-RES BOARD for further information.

Below is a chart for the bits contained in the plane select register.

BIT	FUNCTION
0	Select plane 0
1	Select plane 1
2	Select plane 2
3	No connection
4	Graphics on/off
5	Graphics/Alpha switch
6 and 7	No connection

To select a particular plane, a 1 must be in the corresponding bit while the remaining two plane selects are a 0. If plane 1 is to be selected, then D0 and D2 would contain a 0, while D1 would contain a 1.

The graphics on/off bit, D4, contains a 1 to turn on (display) the graphics data in the installed planes. A 0 forces the palette to ignore the memory plane data and display the color contained at palette address 08H (Processor I/O address 0190H).

The graphics/alpha bit, D5, determines which data is used as palette addresses. If this bit is a 1, the Hi-Res memory planes are used. If this bit is a 0, the 9007 video data is used (this displays text on the CM-1 color monitor).

9.3.5 Displaying Alpha-Numeric Text

The Hi-Res board contains circuitry to switch between the internal memory planes or external data for use as palette addresses. In the Model 2000, the external data is hard-wired on the bus as the 9007 video and the video attribute bit INTENSITY. If the external mode is selected (referred to as the ALPHA MODE), the video data is palette address bit A0 and the attribute bit for intensity is palette address bit A1. Palette address bits A2 and A3 are tied high (a 1). This allows 4-color text to be displayed on the CM-1 color monitor.

For this to work properly, the 9007 must be in 640 X 400 display mode, NOT in 800 X 400 mode. Text from the 9007 and graphics data from the Hi-Res board CANNOT be displayed at the same time on the CM-1 monitor.

9.3.6 Displaying Monochrome Graphics on VM-1 B/W Monitor

You have the option of using either a monochrome monitor (the VM-1), a Hi-Res board and a color monitor (the CM-1) or both. This implies four possible combinations for having text (generated by the main unit's 9007) and graphics (generated by the Hi-Res option) displayed at the same time. These are summarized below:

VM-1	CM-1
TEXT	TEXT
TEXT	GRAPHICS
GRAPHICS	TEXT
GRAPHICS	GRAPHICS

Of the four possible modes, ONLY THREE ARE ALLOWED. Graphics on the VM-1 and Text on the CM-1 is NOT allowed. The way that a particular mode is selected is by two I/O ports, one on the Hi-Res board and one in the Model 2000 main unit. The plane select register on the Hi-Res board selects between text and graphics displayed on the CM-1. This bit is sent to the main pc board and used with the VIDEO SELECT BIT located at port 0101H. If D15 of this port is a 1, the 9007 video goes to the VM-1 monitor. If the bit is a 0, then the graphics data from PLANE 0 goes to the VM-1. In this manner, monochrome graphics can be displayed on the VM-1 from the Hi-Res board. If other planes are installed, the VM-1 ignores them and uses PLANE 0 ONLY.

Alpa-Numeric Palette Table

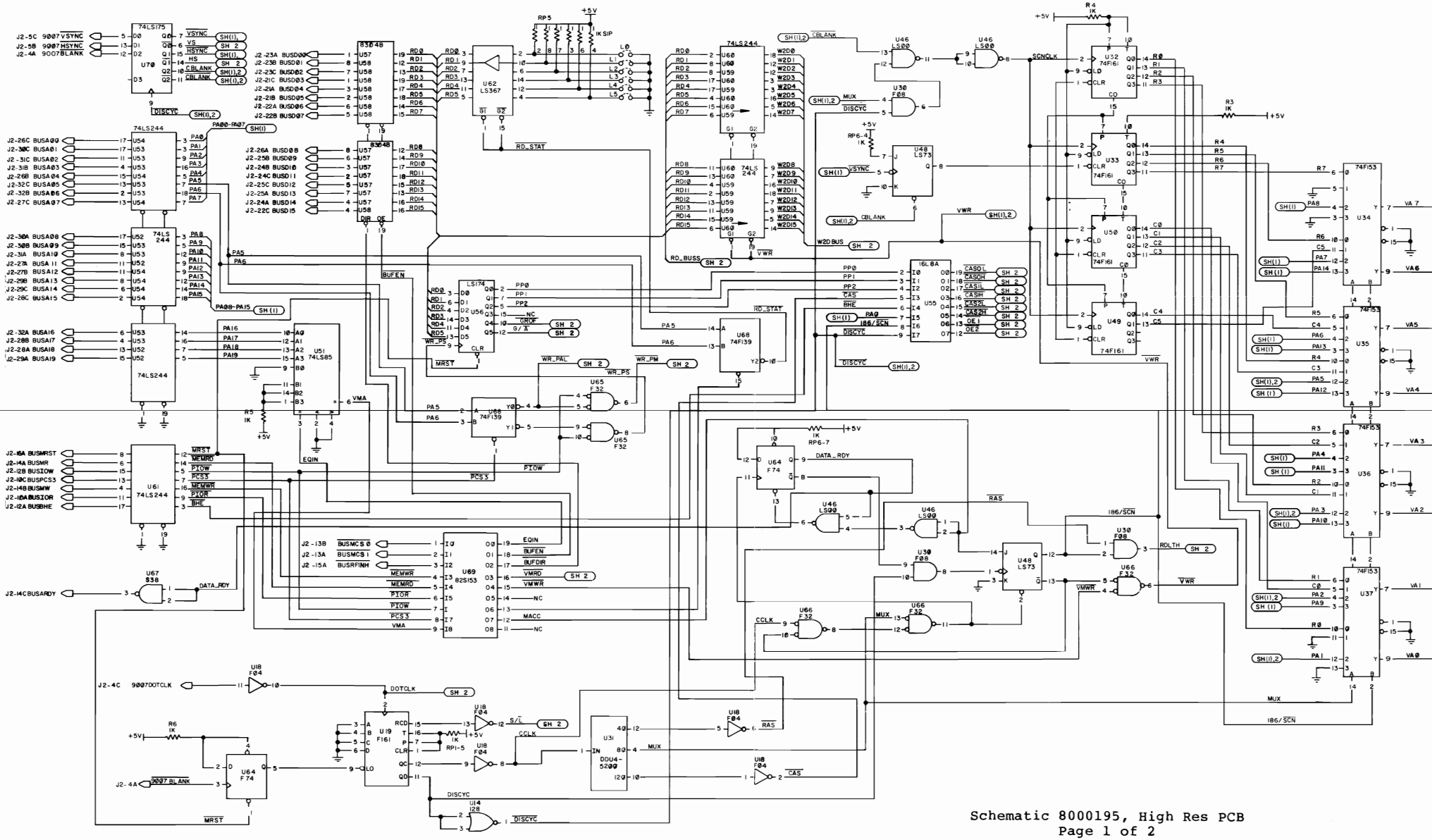
198 - Background - Low intensity color
19A - Character - Low intensity color
19C - Background - High intensity color
19E - Character - High intensity color

9.3.7 Status Port Description

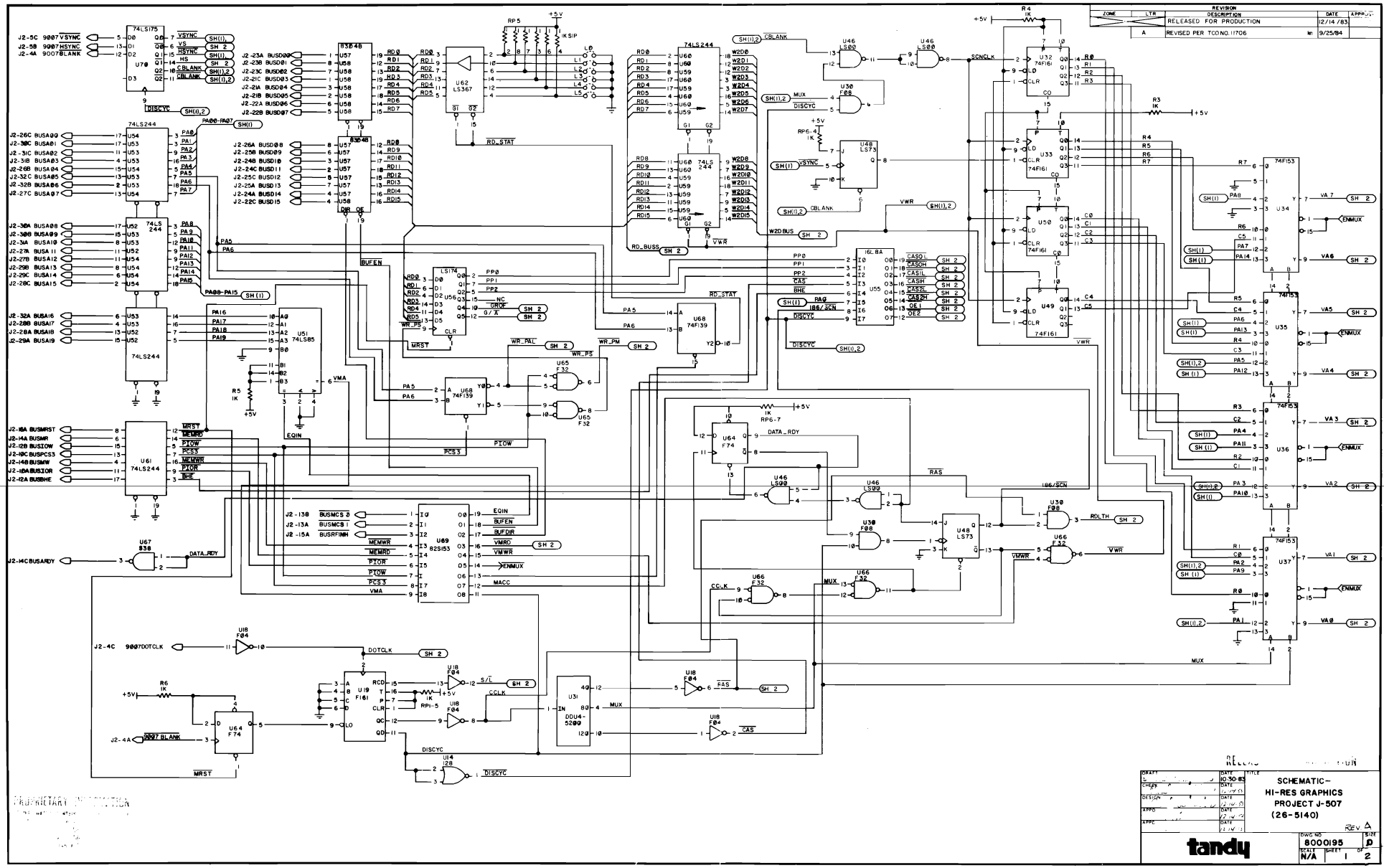
The Hi-Res board contains a 6 bit status port, which is READ-ONLY. This port is used to determine the number of installed planes, pcb revision level, etc. It is located in the I/O map at address 0180H. The following description relates the bits in the port to their meaning.

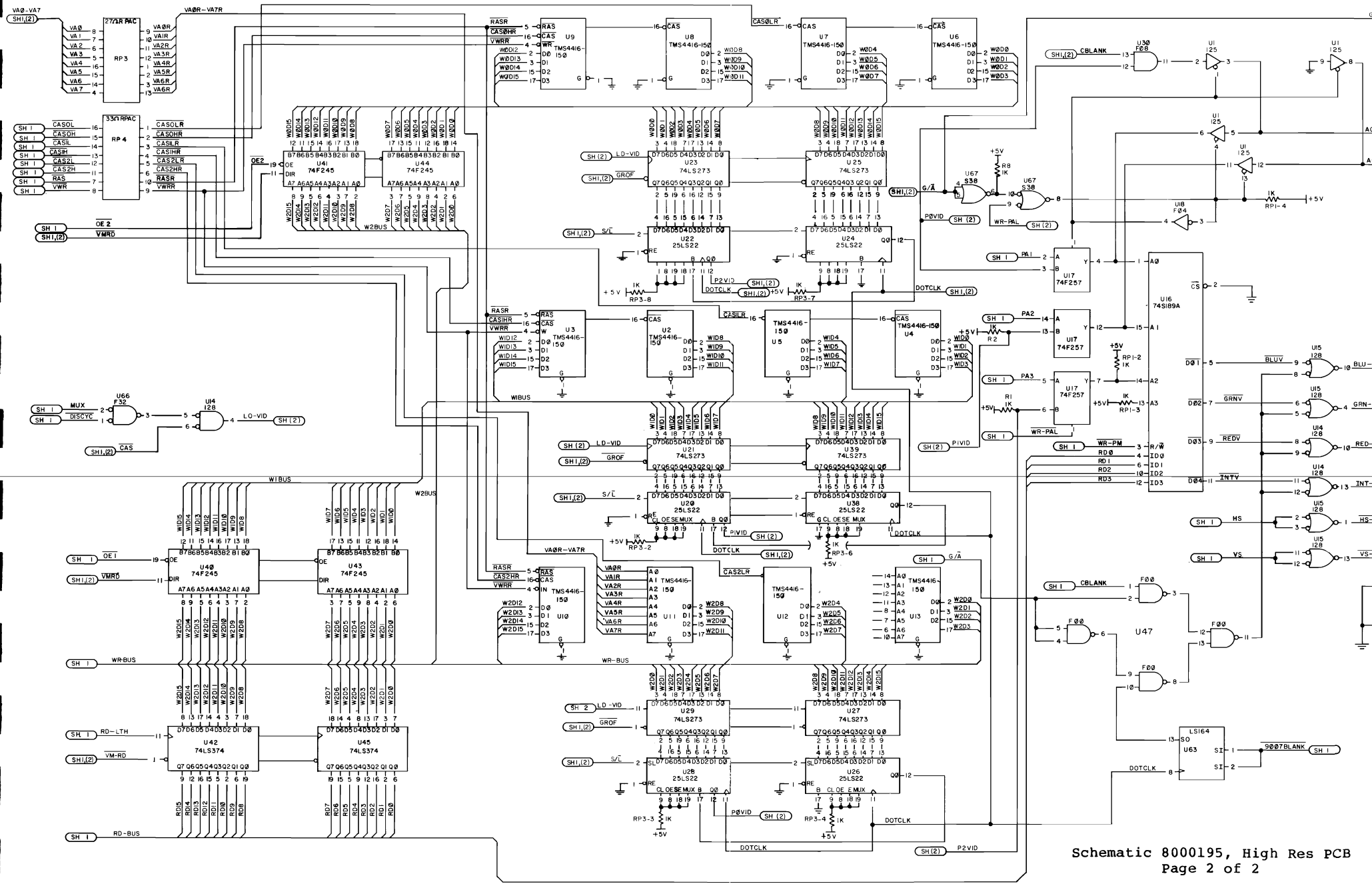
BIT	MEANING
0	0 = Hi-Res board 1 = Not Used
1	0 = Plane 0 only 1 = 3 planes installed
2,3,4	pcb revision
5	future use

Timing Diagram, Hi Res PCB

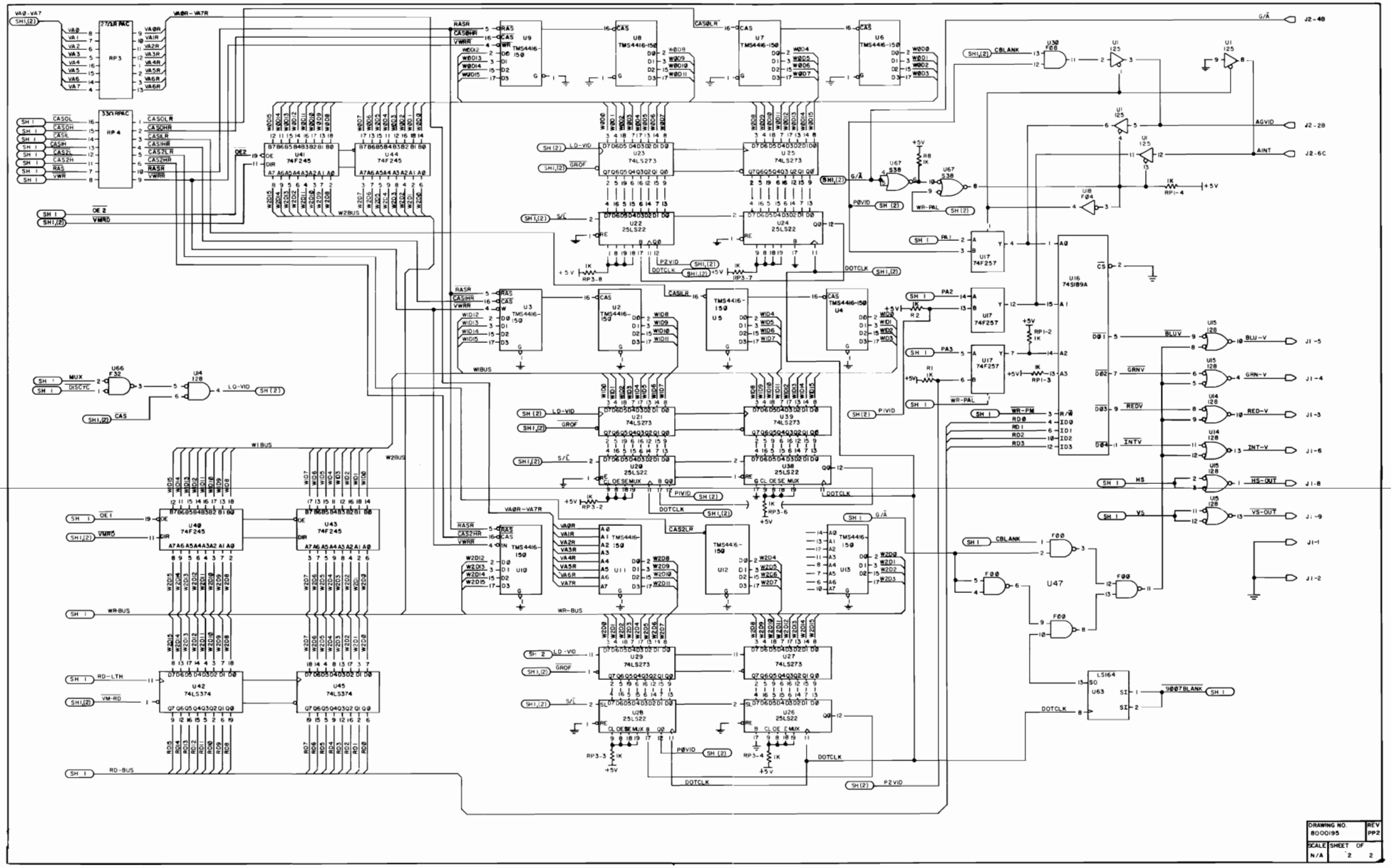


Schematic 8000195, High Res PCB
Page 1 of 2

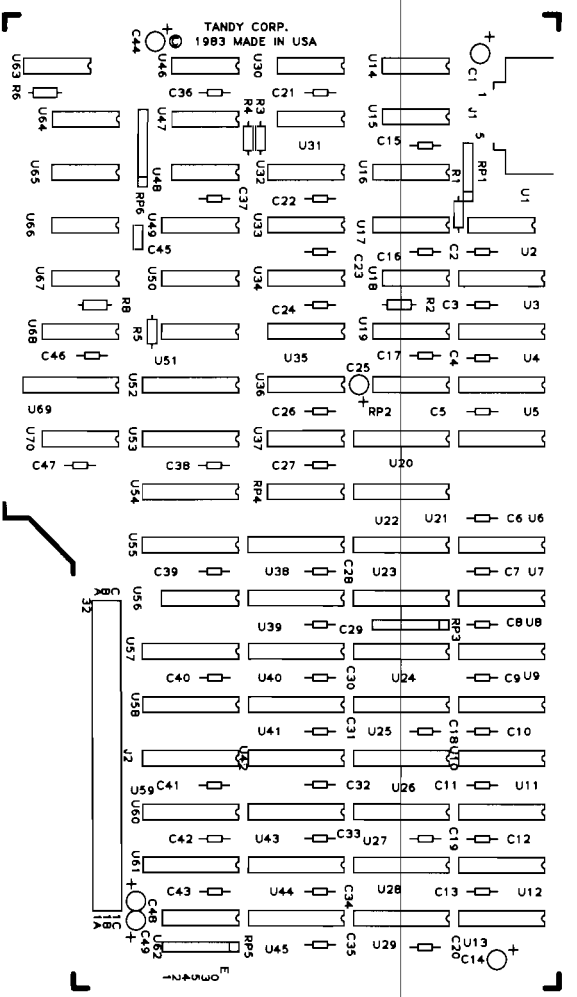

REVISION
ZONE | LTR | DESCRIPTION | DATE | APPD
A | RELEASED FOR PRODUCTION | 12/14/83
A | REVISED PER TCO NO. 11706 | 9/25/84
SCHEMATIC-
HI-RES GRAPHICS
PROJECT J-507
(26-5140)
tandy
DWG NO 8000195
REV A
SIZE D
SCALE N/A
SHEET 1 OF 2
PROPRIETARY INFORMATION



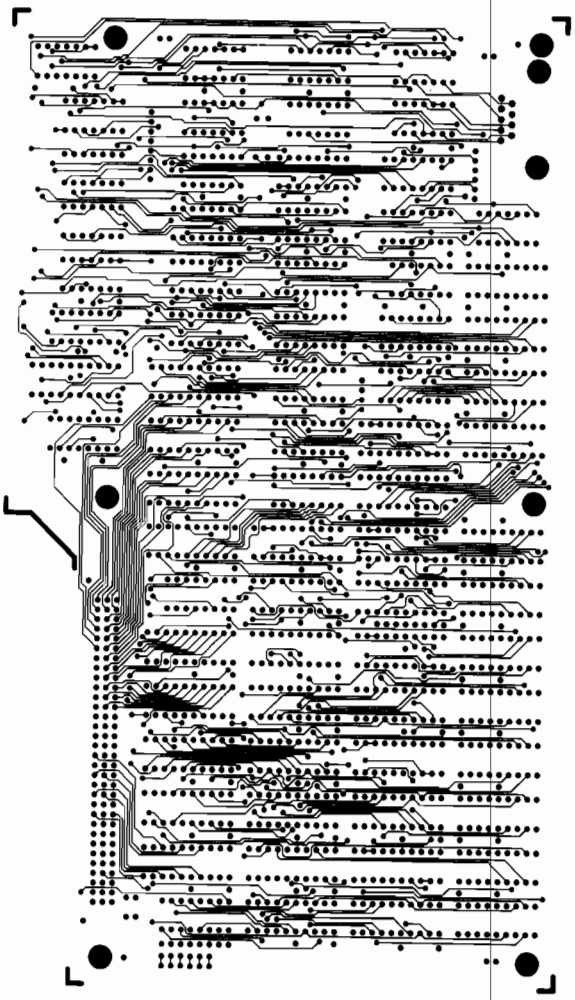
Schematic 8000195, High Res PCB
Page 2 of 2



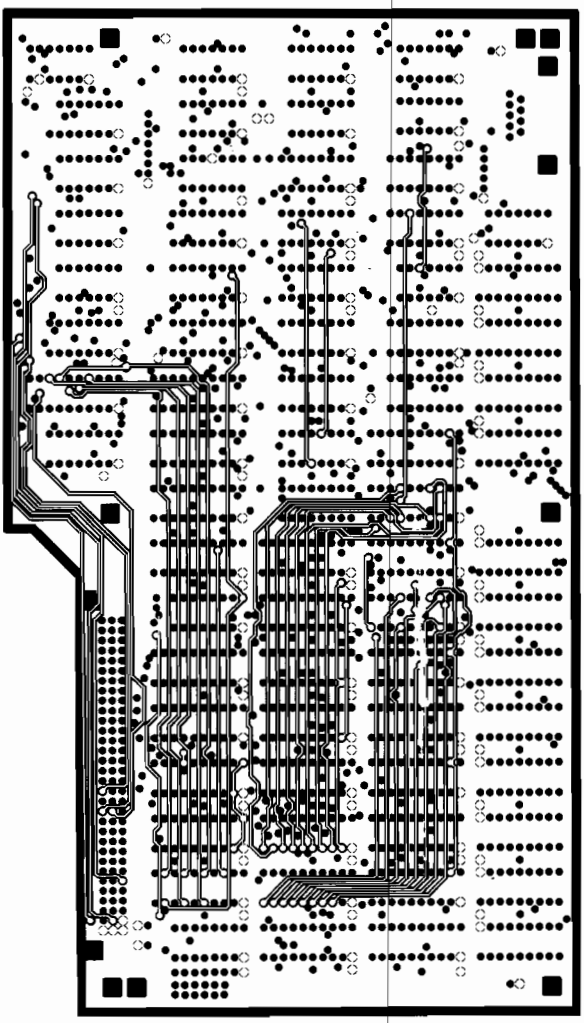
DRAWING NO.	REV
8000195	PP2
SCALE	SHEET OF
N/A	2 2



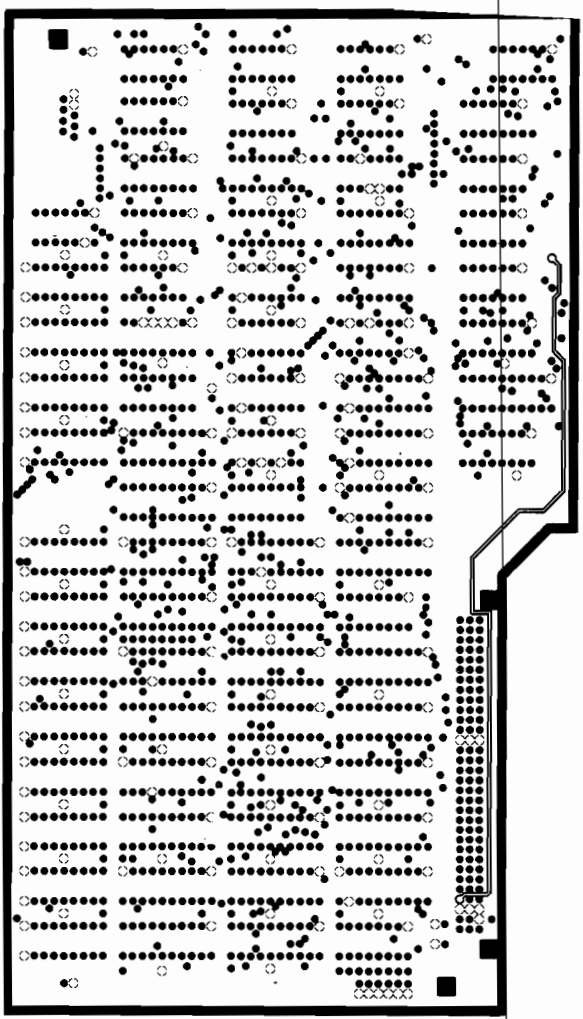
Component Location 1700261, Hi/Lo Res Graphics PCB



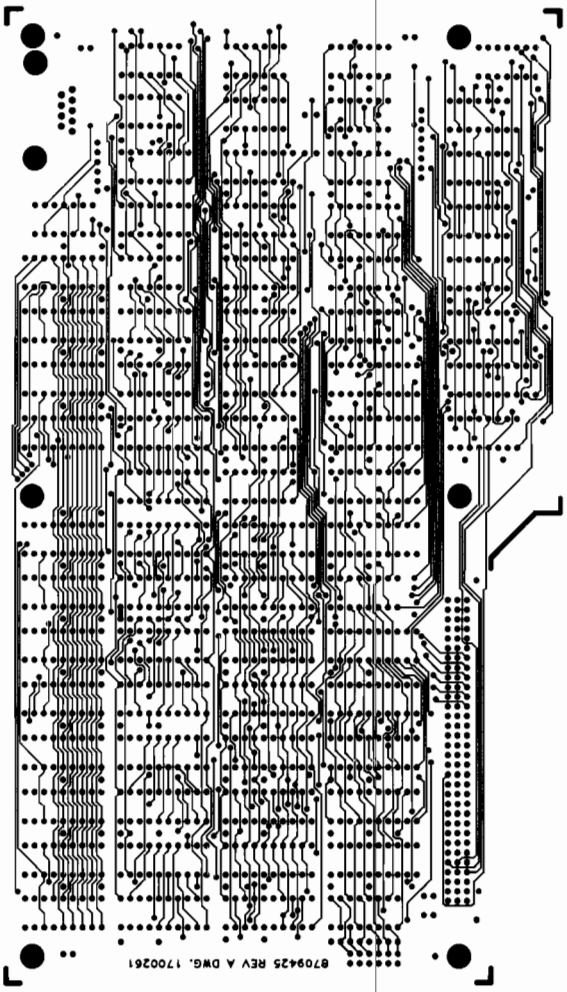
Circuit Trace 1700261, Hi/Lo Res Graphics PCB
Circuit Side



Circuit Trace 1700261, Hi/Lo Res Graphics PCB
+5 Volt Plane



Circuit Trace 1700261, Hi/Lo Res Graphics PCB
Ground Plane



Circuit Trace 1700261, Hi/Lo Res Graphics PCB
Solder Side

Parts List - PCB Assembly 889B010
26-5140 B & W Graphics Option

Item	Sym	Description	Part Number
1	1	Chassis, Graphics Board	8729258
2	2	Plunger, Nylatch	8590149
3	2	Grommet, Nylatch	8590148
4	1	PCB, Graphics Board	8709425
5	1	Connector, DB9 (J1)	8519183
6	1	Connector, 96 Pin (J2)	8519181
7	12	Socket, 18-Pin DIP (U2-U13)	8509006
8	11	Socket, 20-Pin DIP (U20,22,24, 38,40,41,43,44,55,69)	8509009
9	2	Screw, #2-56 x 3/8" PPH (J2)	8569201
10	2	Nut, #2 (J2)	8579042
11	6	Screw, #4-40 x 3/16" PPH MS	8569272
12	1	Label, PCB Serial	8789140
	C1	Capacitor, 22 mfd, 6.3V Elec Radial	8326221
	C2	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C3	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C4	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C5	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C6	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C7	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C8	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C9	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C10	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C11	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C12	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C13	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C14	Capacitor, 22 mfd, 6.3V Elec Radial	8326221
	C15	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C16	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C17	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C18	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C19	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C20	Capacitor, .1 mfd, 50V Mono Axial	8326221
	C21	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C22	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C23	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C24	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C25	Capacitor, 22 mfd, 6.3V Elec Radial	8326221
	C26	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C27	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C28	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C29	Capacitor, .1 mfd, 50V Mono Axial	8374104

Parts List - PCB Assembly 8898801
26-5140 B & W Graphics Option

Item	Sym	Description	Part Number
	C30	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C31	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C32	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C33	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C34	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C35	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C36	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C37	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C38	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C39	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C40	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C41	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C42	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C43	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C44	Capacitor, 22 mfd, 6.3V Elec Radial	8326221
	C45	Not Used	
	C46	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C47	Capacitor, .1 mfd, 50V Mono Axial	8374104
	C48	Capacitor, 22 mfd, 6.3V Elec Radial	6326221
	C49	Capacitor, 22 mfd, 6.3V Elec Radial	6326221
	R1	Resistor, 4.7 kohm, 1/4W 5%	8207247
	R2	Resistor, 330 ohm, 1/4W 5%	8207133
	RP1	Resistor Pak, 1 kohm, SIP 6 Pin	8290210
	RP2	Resistor Pak, 27 ohm, DIP 16 Pin	8290027
	RP3	Resistor Pak, 1 kohm, SIP 10 Pin	
	RP4	Resistor Pak, 33 ohm, DIP 16 Pin	8290044
	RP5	Resistor Pak, 1 kohm, SIP 10 Pin	
	RP6	Resistor Pak, 1 kohm, SIP 10 Pin	
	U1	IC, 74LS125, Bus Buffer	8020125
	U2	Not Used	
	U3	Not Used	
	U4	Not Used	
	U5	Not Used	
	U6	IC, TMS4416-15 RAM	8040416
	U7	IC, TMS4416-15 RAM	8040416
	U8	IC, TMS4416-15 RAM	8040416
	U9	IC, TMS4416-15 RAM	8040416
	U10	Not Used	
	U11	Not Used	
	U12	Not Used	
	U13	Not Used	

Parts List - PCB Assembly 8898801
26-5140 B & W Graphics Option

Item	Sym	Description	Part Number
	U14	IC, 74128, 50 ohm Line Driver	8000128
	U15	IC, 74128, 50 ohm Line Driver	8000128
	U16	IC, 74S189, RAM	8010189
	U17	IC, 74F257, Multiplexer	8015257
	U18	IC, 74F04, Hex Inverter	8015004
	U19	IC, 74F161, Counter	8015161
	U20	Not Used	
	U21	IC, 74LS273, Octal Flip Flop	8020273
	U22	Not Used	
	U23	IC, 74LS273, Octal Flip Flop	8020273
	U24	Not Used	
	U25	IC, 74LS273, Octal Flip Flop	8020273
	U26	IC, 25LS22, 8-bit Shift Register	8020022
	U27	IC, 74LS273, Octal Flip Flop	8020273
	U28	IC, 25LS22, 8-Bit Shift Register	8020022
	U29	IC, 74LS273, Octal Flip Flop	8020273
	U30	IC, 74F08, Quad 2-Input NAND	8015008
	U31	IC, DDU4-5200 Delay Line, 200nsec	8429010
	U32	IC, 74F161, Counter	8015161
	U33	IC, 74F161, Counter	8015161
	U34	IC, 74F153, Multiplexer	8015153
	U35	IC, 74F153, Multiplexer	8015153
	U36	IC, 74F153, Multiplexer	8015153
	U37	IC, 74F153, Multiplexer	8015153
	U38	Not Used	
	U39	IC, 74LS273, Octal Flip Flop	8020273
	U40	Not Used	
	U41	Not Used	
	U42	IC, 74LS374, Flip Flop	8020374
	U43	Not Used	
	U44	Not Used	
	U45	IC, 74LS374, Flip Flop	8020374
	U46	IC, 74LS00, Quad 2-Input NAND	8020000
	U47	IC, 74F00, Quad 2-Input NAND	8015000
	U48	IC, 74LS73, Flip Flop	8020073
	U49	IC, 74F161, Counter	8015161
	U50	IC, 74F161, Counter	8015161
	U51	IC, 74LS85, Comparator	8020085
	U52	IC, 74LS244, Octal Buffer	8020244
	U53	IC, 74LS244, Octal Buffer	8020244
	U54	IC, 74LS244, Octal Buffer	8020244
	U55	IC, PAL16L8A, Mono	
	U56	IC, 74LS174, Hex Flip Flop	8020174

Parts List - PCB Assembly 8898801
26-5140 B & W Graphics Option

Item	Sym	Description	Part Number
	U57	IC, 8304B, Bus Transceiver	8060304
	U58	IC, 8304B, Bus Transceiver	8060304
	U59	IC, 74LS244, Octal Buffer	8020244
	U60	IC, 74LS244, Octal Buffer	8020244
	U61	IC, 74LS244, Octal Buffer	8020244
	U62	IC, 74LS367, Hex Driver	8020367
	U63	IC, 74LS164, Shift Register	8020164
	U64	IC, 74F74, Flip Flop	8015074
	U65	IC, 74F32, Quad 2-Input OR	8015032
	U66	IC, 74F32, Quad 2-Input OR	8015032
	U67	IC, 74S38, Quad 2-Input NAND	8010038
	U68	IC, 74F139, Decoder	8015139
	U69	IC, 82S153, IFL Decode	
	U70	IC, 74LS175, Flip Flop	8020175

Parts List

26-5141 Color Video Upgrade

Item	Sym	Description	Part Number

Note: This kit requires the 26-5140 B & W Graphics option (see Paragraph 9.4) in addition to the parts noted below.

	U2	IC, RAM TMS4416-15	8040416
	U3	IC, RAM TMS4416-15	8040416
	U4	IC, RAM TMS4416-15	8040416
	U5	IC, RAM TMS4416-15	8040416
	U10	IC, RAM TMS4416-15	8040416
	U11	IC, RAM TMS4416-15	8040416
	U12	IC, RAM TMS4416-15	8040416
	U13	IC, RAM TMS4416-15	8040416
	U20	IC, 25LS22, 8-bit Shift Register	8020022
	U22	IC, 25LS22, 8-bit Shift Register	8020022
	U24	IC, 25LS22, 8-bit Shift Register	8020022
	U38	IC, 25LS22, 8-bit Shift Register	8020022
	U40	IC, 74F245, Octal Buffer	8015245
	U41	IC, 74F245, Octal Buffer	8015245
	U43	IC, 74F245, Octal Buffer	8015245
	U44	IC, 74F245, Octal Buffer	8015245
	U55	IC, PAL16L8A Color	

APPENDICES

The following sections contain reprints of manufacturer's documentation of components used in the Model 2000 Computer.

Tandy Corporation gratefully acknowledges permission by the following to reprint their copyrighted material in this manual.

Mitsubishi Electric Corporation
2-3 Marunouchi 2-Chome
Chiyoda-Ku, Tokyo 100, Japan

Tandon Corporation
20320 Prarie Street
Chatsworth, California 91311

Intel Corporation
3065 Bowers Avenue
Santa Clara, California 95051

Standard Microsystems Corporation
35 Marcus Blvd.
Hauppauge, New York 11787

iAPX 186
HIGH INTEGRATION 16-BIT MICROPROCESSOR

- **Integrated Feature Set**
  - —Enhanced 8086-2 CPU
  - —Clock Generator
  - —2 Independent, High-Speed DMA Channels
  - —Programmable Interrupt Controller
  - —3 Programmable 16-bit Timers
  - —Programmable Memory and Peripheral Chip-Select Logic
  - —Programmable Wait State Generator
  - —Local Bus Controller
- **Available in 8 MHz (80186) and cost effective 6 MHz (80186-6) versions.**
- **High-Performance Processor**
  - —2 Times the Performance of the Standard iAPX 86
  - —4 MByte/Sec Bus Bandwidth Interface
- **Direct Addressing Capability to 1 MByte of Memory**
- **Completely Object Code Compatible with All Existing iAPX 86, 88 Software**
  - —10 New Instruction Types
- **Complete System Development Support**
  - —Development Software: Assembler, PL/M, Pascal, Fortran, and System Utilities
  - —In-Circuit-Emulator (I²ICE™-186)
  - —iRMX™ 86, 88 Compatible (80130 OSF)
- **Optional Numeric Processor Extension**
  - —iAPX 186/20 High-Performance 80-bit Numeric Data Processor

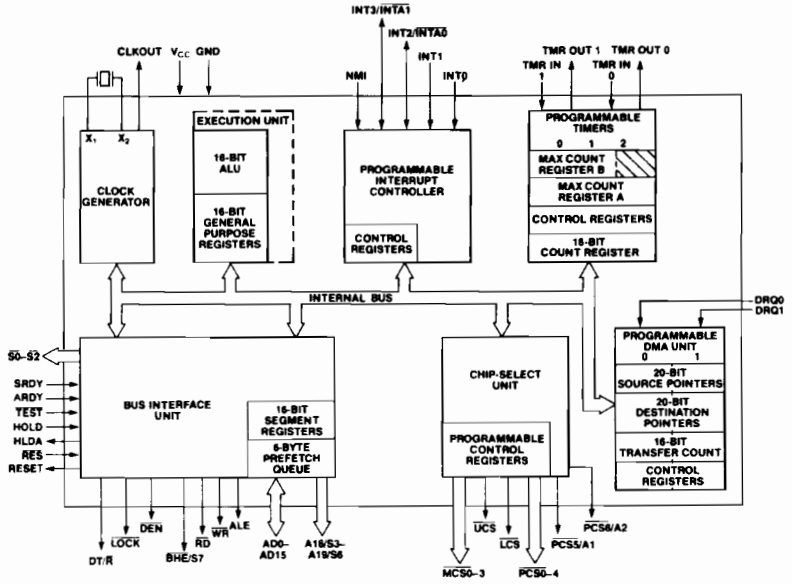


Figure 1. iAPX 186 Block Diagram

JULY 1983
ORDER NUMBER: 210451-003

The Intel iAPX 186 (80186 part number) is a highly integrated 16-bit microprocessor. The iAPX 186 effectively combines 15–20 of the most common iAPX 86 system components onto one. The 80186 provides two times greater throughput than the standard 5 MHz iAPX 86. The iAPX 186 is upward compatible with iAPX 86 and 88 software and adds 10 new instruction types to the existing set.

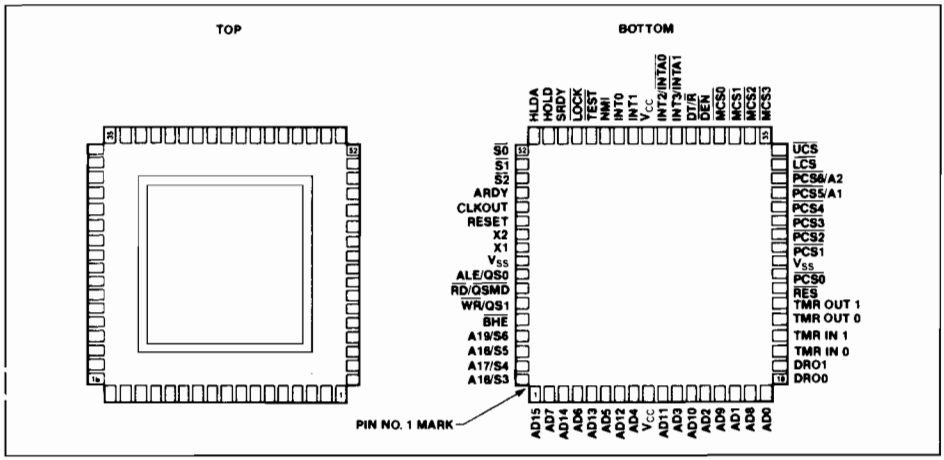


Figure 2. 80186 Pinout Diagram

Table 1. 80186 Pin Description

Symbol	Pin No.	Type	Name and Function
V_{CC}, V_{CC}	9,43	I	System Power: +5 volt power supply.
V_{SS}, V_{SS}	26,60	I	System Ground.
RESET	57	O	Reset Output indicates that the 80186 CPU is being reset, and can be used as a system reset. It is active HIGH, synchronized with the processor clock, and lasts an integer number of clock periods corresponding to the length of the $\overline{RES}$ signal.
X1, X2	59,58	I	Crystal Inputs, X1 and X2, provide an external connection for a fundamental mode parallel resonant crystal for the internal crystal oscillator. X1 can interface to an external clock instead of a crystal. The input or oscillator frequency is internally divided by two to generate the clock signal (CLKOUT).
CLKOUT	56	O	Clock Output provides the system with a 50% duty cycle waveform. All device pin timings are specified relative to CLKOUT. CLKOUT has sufficient MOS drive capabilities for the 8087 Numeric Processor Extension.
$\overline{RES}$	24	I	System Reset causes the 80186 to immediately terminate its present activity, clear the internal logic, and enter a dormant state. This signal may be asynchronous to the 80186 clock. The 80186 begins fetching instructions approximately 7 clock cycles after $\overline{RES}$ is returned HIGH. $\overline{RES}$ is required to be LOW for greater than 4 clock cycles and is internally synchronized. For proper initialization, the LOW-to-HIGH transition of $\overline{RES}$ must occur no sooner than 50 microseconds after power up. This input is provided with a Schmitt-trigger to facilitate power-on $\overline{RES}$ generation via an RC network. When $\overline{RES}$ occurs, the 80188 will drive the status lines to an inactive level for one clock, and then tri-state them.

A

Table 1. 80186 Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
$\overline{TEST}$	47	I	$\overline{TEST}$ is examined by the WAIT instruction. If the $\overline{TEST}$ input is HIGH when "WAIT" execution begins, instruction execution will suspend. $\overline{TEST}$ will be resampled until it goes LOW, at which time execution will resume. If interrupts are enabled while the 80186 is waiting for $\overline{TEST}$, interrupts will be serviced. This input is synchronized internally.
TMR IN 0, TMR IN1	20 21	I I	Timer Inputs are used either as clock or control signals, depending upon the programmed timer mode. These inputs are active HIGH (or LOW-to-HIGH transitions are counted) and internally synchronized.
TMR OUT 0, TMR OUT 1	22 23	O O	Timer outputs are used to provide single pulse or continuous waveform generation, depending upon the timer mode selected.
DRQ0 DRQ1	18 19	I I	DMA Request is driven HIGH by an external device when it desires that a DMA channel (Channel 0 or 1) perform a transfer. These signals are active HIGH, level-triggered, and internally synchronized.
NMI	46	I	Non-Maskable Interrupt is an edge-triggered input which causes a type 2 interrupt. NMI is not maskable internally. A transition from a LOW to HIGH initiates the interrupt at the next instruction boundary. NMI is latched internally. An NMI duration of one clock or more will guarantee service. This input is internally synchronized.
INT0, INT1, INT2/$\overline{INTA0}$ INT3/$\overline{INTA1}$	45,44 42 41	I I/O I/O	Maskable Interrupt Requests can be requested by strobing one of these pins. When configured as inputs, these pins are active HIGH. Interrupt Requests are synchronized internally. INT2 and INT3 may be configured via software to provide active-LOW interrupt-acknowledge output signals. All interrupt inputs may be configured via software to be either edge- or level-triggered. To ensure recognition, all interrupt requests must remain active until the interrupt is acknowleged. When iRMX mode is selected, the function of these pins changes (see Interrupt Controller section of this data sheet).
A19/S6, A18/S5, A17/S4, A16/S3	65 66 67 68	O O O O	Address Bus Outputs (16–19) and Bus Cycle Status (3–6) reflect the four most significant address bits during T_1. These signals are active HIGH. During T_2, T_3, T_W, and T_4, status information is available on these lines as encoded below: S3,S4, and S5 are defined as LOW during T_2–T_4.
AD15–AD0	10–17, 1–8	I/O	Address/Data Bus (0–15) signals constitute the time mutiplexed memory or I/O address (T_1) and data (T_2, T_3, T_W, and T_4) bus. The bus is active HIGH. A_0 is analogous to $\overline{BHE}$ for the lower byte of the data bus, pins D_7 through D_0. It is LOW during T_1 when a byte is to be transferred onto the lower portion of the bus in memory or I/O operations.
$\overline{BHE}$/S7	64	O	During T_1 the Bus High Enable signal should be used to determine if data is to be enabled onto the most significant half of the data bus, pins D_{15}–D_8. $\overline{BHE}$ is LOW during T_1 for read, write, and interrupt acknowledge cycles when a byte is to be transferred on the higher half of the bus. The S_7 status information is available during T_2, T_3, and T_4. S_7 is logically equivalent to $\overline{BHE}$. The signal is active LOW, and is tristated OFF during bus HOLD.

	Low	High
S6	Processor Cycle	DMA Cycle

$\overline{BHE}$ and A0 Encodings		
$\overline{BHE}$ Value	A0 Value	Function
0	0	Word Transfer
0	1	Byte Transfer on upper half of data bus (D15–D8)
1	0	Byte Transfer on lower half of data bus (D_7–D_0)
1	1	Reserved

Table 1. 80186 Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
ALE/QS0	61	O	Address Latch Enable/Queue Status 0 is provided by the 80186 to latch the address into the 8282/8283 address latches. ALE is active HIGH. Addresses are guaranteed to be valid on the trailing edge of ALE. The ALE rising edge is generated off the rising edge of the CLKOUT immediately preceding T_1 of the associated bus cycle, effectively one-half clock cycle earlier than in the standard 8086. The trailing edge is generated off the CLKOUT rising edge in T_1 as in the 8086. Note that ALE is never floated.
$\overline{WR}$/QS1	63	O	Write Strobe/Queue Status 1 indicates that the data on the bus is to be written into a memory or an I/O device. $\overline{WR}$ is active for T_2, T_3, and T_W of any write cycle. It is active LOW, and floats during "HOLD." It is driven HIGH for one clock during Reset, and then floated. When the 80186 is in queue status mode, the ALE/QS0 and $\overline{WR}$/QS1 pins provide information about processor/instruction queue interaction.

QS1	QS0	Queue Operation
0	0	No queue operation
0	1	First opcode byte fetched from the queue
1	1	Subsequent byte fetched from the queue
1	0	Empty the queue

$\overline{RD}$/QSMD	62	O	Read Strobe indicates that the 80186 is performing a memory or I/O read cycle. $\overline{RD}$ is active LOW for T_2, T_3, and T_W of any read cycle. It is guaranteed not to go LOW in T_2 until after the Address Bus is floated. $\overline{RD}$ is active LOW, and floats during "HOLD." $\overline{RD}$ is driven HIGH for one clock during Reset, and then the output driver is floated. A weak internal pull-up mechanism on the $\overline{RD}$ line holds it HIGH when the line is not driven. During RESET the pin is sampled to determine whether the 80186 should provide ALE, $\overline{WR}$, and $\overline{RD}$, or if the Queue-Status should be provided. $\overline{RD}$ should be connected to GND to provide Queue-Status data.
ARDY	55	I	Asynchronous Ready informs the 80186 that the addressed memory space or I/O device will complete a data transfer. The ARDY input pin will accept an asynchronous input, and is active HIGH. Only the rising edge is internally synchronized by the 80186. This means that the falling edge of ARDY must be synchronized to the 80186 clock. If connected to V_{CC}, no WAIT states are inserted. Asynchronous ready (ARDY) or synchronous ready (SRDY) must be active to terminate a bus cycle.
SRDY	49	I	Synchronous Ready must be synchronized externally to the 80186. The use of SRDY provides a relaxed system-timing specification on the Ready input. This is accomplished by eliminating the one-half clock cycle which is required for internally resolving the signal level when using the ARDY input. This line is active HIGH. If this line is connected to V_{CC}, no WAIT states are inserted. Asynchronous ready (ARDY) or synchronous ready (SRDY) must be active before a bus cycle is terminated. If unused, this line should be tied LOW.
$\overline{LOCK}$	48	O	$\overline{LOCK}$ output indicates that other system bus masters are not to gain control of the system bus while $\overline{LOCK}$ is active LOW. The $\overline{LOCK}$ signal is requested by the LOCK prefix instruction and is activated at the beginning of the first data cycle associated with the instruction following the LOCK prefix. It remains active until the completion of the instruction following the LOCK prefix. No prefetches will occur while $\overline{LOCK}$ is asserted. $\overline{LOCK}$ is active LOW, is driven HIGH for one clock during RESET, and then floated. If unused, this line should be tied LOW.

Table 1. 80186 Pin Description (Continued)

Symbol	Pin No.	Type	Name and Function
$\overline{S0}$,$\overline{S1}$,$\overline{S2}$	52-54	O	Bus cycle status $\overline{S0}$-$\overline{S2}$ are encoded to provide bus-transaction information: 80186 Bus Cycle Status Information $\overline{S2}$ / S1 / S0 / Bus Cycle Initiated 0 / 0 / 0 / Interrupt Acknowledge 0 / 0 / 1 / Read I/O 0 / 1 / 0 / Write I/O 0 / 1 / 1 / Halt 1 / 0 / 0 / Instruction Fetch 1 / 0 / 1 / Read Data from Memory 1 / 1 / 0 / Write Data to Memory 1 / 1 / 1 / Passive (no bus cycle) The status pins float during "HOLD." $\overline{S2}$ may be used as a logical M/$\overline{IO}$ indicator, and $\overline{S1}$ as a DT/$\overline{R}$ indicator. The status lines are driven HIGH for one clock during Reset, and then floated until a bus cycle begins.
HOLD (input) HLDA (output)	50 51	I O	HOLD indicates that another bus master is requesting the local bus. The HOLD input is active HIGH. HOLD may be asynchronous with respect to the 80186 clock. The 80186 will issue a HLDA (HIGH) in response to a HOLD request at the end of T_4 or T_1. Simultaneous with the issuance of HLDA, the 80186 will float the local bus and control lines. After HOLD is detected as being LOW, the 80186 will lower HLDA. When the 80186 needs to run another bus cycle, it will again drive the local bus and control lines.
$\overline{UCS}$	34	O	Upper Memory Chip Select is an active LOW output whenever a memory reference is made to the defined upper portion (1K-256K block) of memory. This line is not floated during bus HOLD. The address range activating $\overline{UCS}$ is software programmable.
$\overline{LCS}$	33	O	Lower Memory Chip Select is active LOW whenever a memory reference is made to the defined lower portion (1K-256K) of memory. This line is not floated during bus HOLD. The address range activating $\overline{LCS}$ is software programmable.
$\overline{MCS0}$-3	38,37,36,35	O	Mid-Range Memory Chip Select signals are active LOW when a memory reference is made to the defined mid-range portion of memory (8K-512K). These lines are not floated during bus HOLD. The address ranges activating $\overline{MCS0}$-3 are software programmable.
$\overline{PCS0}$ $\overline{PCS1}$-4	25 27,28,29,30	O O	Peripheral Chip Select signals 0-4 are active LOW when a reference is made to the defined peripheral area (64K byte I/O space). These lines are not floated during bus HOLD. The address ranges activating $\overline{PCS0}$-4 are software programmable.
$\overline{PCS5}$/A1	31	O	Peripheral Chip Select 5 or Latched A1 may be programmed to provide a sixth peripheral chip select, or to provide an internally latched A1 signal. The address range activating $\overline{PCS5}$ is software programmable. When programmed to provide latched A1, rather than $\overline{PCS5}$, this pin will retain the previously latched value of A1 during a bus HOLD. A1 is active HIGH.
$\overline{PCS6}$/A2	32	O	Peripheral Chip Select 6 or Latched A2 may be programmed to provide a seventh peripheral chip select, or to provide an internally latched A2 signal. The address range activating $\overline{PCS6}$ is software programmable. When programmed to provide latched A2, rather than $\overline{PCS6}$, this pin will retain the previously latched value of A2 during a bus HOLD. A2 is active HIGH.
DT/$\overline{R}$	40	O	Data Transmit/Receive controls the direction of data flow through the external 8286/8287 data bus transceiver. When LOW, data is transferred to the 80186. When HIGH the 80186 places write data on the data bus.
$\overline{DEN}$	39	O	Data Enable is provided as an 8286/8287 data bus transceiver output enable. $\overline{DEN}$ is active LOW during each memory and I/O access. $\overline{DEN}$ is HIGH whenever DT/$\overline{R}$ changes state.

FUNCTIONAL DESCRIPTION

Introduction

The following Functional Description describes the base architecture of the iAPX 186. This architecture is common to the iAPX 86, 88, and 286 microprocessor families as well. The iAPX 186 is a very high integration 16-bit microprocessor. It combines 15–20 of the most common microprocessor system components onto one chip while providing twice the performance of the standard iAPX 86. The 80186 is object code compatible with the iAPX 86, 88 microprocessors and adds 10 new instruction types to the existing iAPX 86, 88 instruction set.

iAPX 186 BASE ARCHITECTURE

The iAPX 86, 88, 186, and 286 family all contain the same basic set of registers, instructions, and addressing modes. The 80186 processor is upward compatible with the 8086, 8088, and 80286 CPUs.

Register Set

The 80186 base architecture has fourteen registers as shown in Figures 3a and 3b. These registers are grouped into the following categories.

General Registers
Eight 16-bit general purpose registers used to contain arithmetic and logical operands. Four of these (AX, BX, CX, and DX) can be used as 16-bit registers or split into pairs of separate 8-bit registers.

Segment Registers
Four 16-bit special purpose registers select, at any given time, the segments of memory that are immediately addressable for code, stack, and data. (For usage, refer to Memory Organization.)

Base and Index Registers
Four of the general purpose registers may also be used to determine offset addresses of operands in memory. These registers may contain base addresses or indexes to particular locations within a segment. The addressing mode selects the specific registers for operand and address calculations.

Status and Control Registers
Two 16-bit special purpose registers record or alter certain aspects of the 80186 processor state. These are the Instruction Pointer Register, which contains the offset address of the next sequential instruction to be executed, and the Status Word Register, which contains status and control flag bits (see Figures 3a and 3b).

Status Word Description

The Status Word records specific characteristics of the result of logical and arithmetic instructions (bits 0, 2, 4, 6, 7, and 11) and controls the operation of the 80186 within a given operating mode (bits 8, 9, and 10). The Status Word Register is 16-bits wide. The function of the Status Word bits is shown in Table 2.

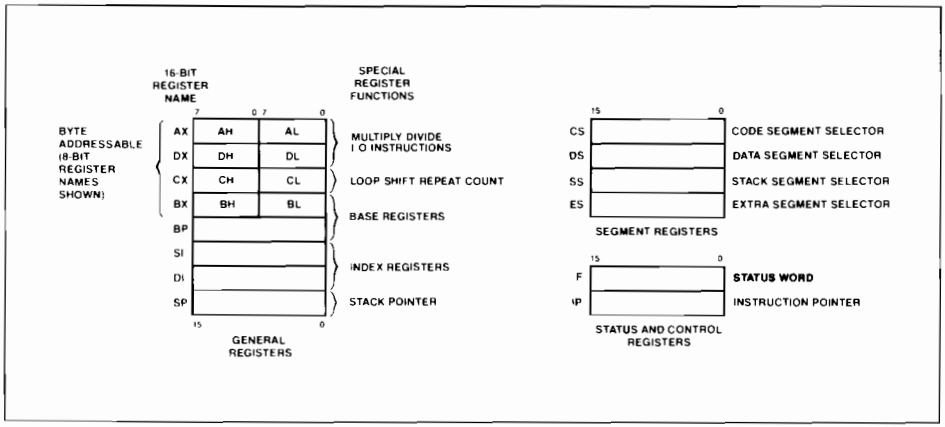


Figure 3a. 80186 General Purpose Register Set

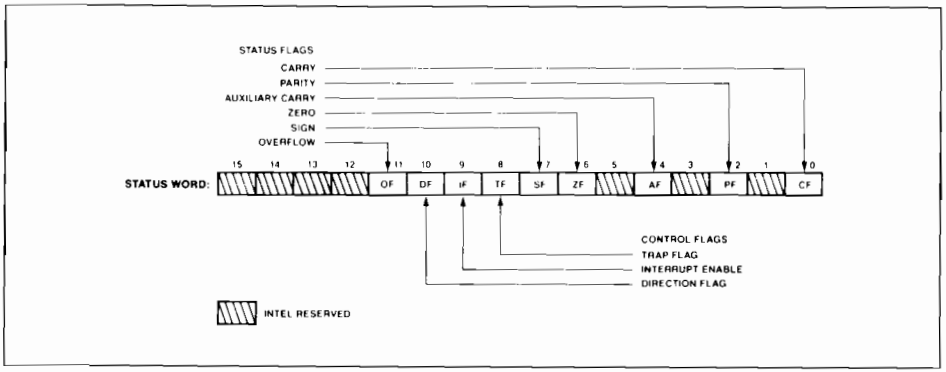


Figure 3b. Status Word Format

Table 2. Status Word Bit Functions

Bit Position	Name	Function
0	CF	Carry Flag—Set on high-order bit carry or borrow, cleared otherwise
2	PF	Parity Flag—Set if low-order 8 bits of result contain an even number of 1-bits, cleared otherwise
4	AF	Set on carry from or borrow to the low order four bits of AL; cleared otherwise
6	ZF	Zero Flag–Set if result is zero; cleared otherwise
7	SF	Sign Flag—Set equal to high-order bit of result (0 if positive, 1 if negative)
8	TF	Single Step Flag—Once set, a single step interrupt occurs after the next instruction executes. TF is cleared by the single step interrupt.
9	IF	Interrupt-enable Flag—When set, maskable interrupts will cause the CPU to transfer control to an interrupt vector specified location
10	DF	Direction Flag—Causes string instructions to auto decrement the appropriate index register when set. Clearing DF causes auto increment.
11	OF	Overflow Flag—Set if the signed result cannot be expressed within the number of bits in the destination operand; cleared otherwise

Instruction Set

The instruction set is divided into seven categories: data transfer, arithmetic, shift/rotate/logical, string manipulation, control transfer, high-level instructions, and processor control. These categories are summarized in Figure 4.

An 80186 instruction can reference anywhere from zero to several operands. An operand can reside in a register, in the instruction itself, or in memory. Specific operand addressing modes are discussed later in this data sheet.

Memory Organization

Memory is organized in sets of segments. Each segment is a linear contiguous sequence of up to 64K (2^{16}) 8-bit bytes. Memory is addressed using a two-component address (a pointer) that consists of a 16-bit base segment and a 16-bit offset. The 16-bit base values are contained in one of four internal segment registers (code, data, stack, extra). The physical address is calculated by shifting the base value LEFT by four bits and adding the 16-bit offset value to yield a 20-bit physical address (see Figure 5). This allows for a 1 MByte physical address size.

All instructions that address operands in memory must specify the base segment and the 16-bit offset value. For speed and compact instruction encoding, the segment register used for physical address generation is implied by the addressing mode used (see Table 3). These rules follow the way programs are written (see Figure 6) as independent modules that require areas for code and data, a stack, and access to external data areas.

Special segment override instruction prefixes allow the implicit segment register selection rules to be overridden for special cases. The stack, data, and extra segments may coincide for simple programs.

GENERAL PURPOSE	
MOV	Move byte or word
PUSH	Push word onto stack
POP	Pop word off stack
PUSHA	Push all registers on stack
POPA	Pop all registers from stack
XCHG	Exchange byte or word
XLAT	Translate byte
INPUT/OUTPUT	
IN	Input byte or word
OUT	Output byte or word
ADDRESS OBJECT	
LEA	Load effective address
LDS	Load pointer using DS
LES	Load pointer using ES
FLAG TRANSFER	
LAHF	Load AH register from flags
SAHF	Store AH register in flags
PUSHF	Push flags onto stack
POPF	Pop flags off stack

ADDITION	
ADD	Add byte or word
ADC	Add byte or word with carry
INC	Increment byte or word by 1
AAA	ASCII adjust for addition
DAA	Decimal adjust for addition
SUBTRACTION	
SUB	Subtract byte or word
SBB	Subtract byte or word with borrow
DEC	Decrement byte or word by 1
NEG	Negate byte or word
CMP	Compare byte or word
AAS	ASCII adjust for subtraction
DAS	Decimal adjust for subtraction
MULTIPLICATION	
MUL	Multiply byte or word unsigned
IMUL	Integer multiply byte or word
AAM	ASCII adjust for multiply
DIVISION	
DIV	Divide byte or word unsigned
IDIV	Integer divide byte or word
AAD	ASCII adjust for division
CBW	Convert byte to word
CWD	Convert word to doubleword

MOVS	Move byte or word string
INS	Input bytes or word string
OUTS	Output bytes or word string
CMPS	Compare byte or word string
SCAS	Scan byte or word string
LODS	Load byte or word string
STOS	Store byte or word string
REP	Repeat
REPE/REPZ	Repeat while equal/zero
REPNE/REPNZ	Repeat while not equal not zero

LOGICALS	
NOT	"Not" byte or word
AND	"And" byte or word
OR	"Inclusive or" byte or word
XOR	"Exclusive or" byte or word
TEST	"Test" byte or word
SHIFTS	
SHL/SAL	Shift logical/arithmetic left byte or word
SHR	Shift logical right byte or word
SAR	Shift arithmetic right byte or word
ROTATES	
ROL	Rotate left byte or word
ROR	Rotate right byte or word
RCL	Rotate through carry left byte or word
RCR	Rotate through carry right byte or word

FLAG OPERATIONS	
STC	Set carry flag
CLC	Clear carry flag
CMC	Complement carry flag
STD	Set direction flag
CLD	Clear direction flag
STI	Set interrupt enable flag
CLI	Clear interrupt enable flag
EXTERNAL SYNCHRONIZATION	
HLT	Halt until interrupt or reset
WAIT	Wait for $\overline{TEST}$ pin active
ESC	Escape to extension processor
LOCK	Lock bus during next instruction
NO OPERATION	
NOP	No operation
HIGH LEVEL INSTRUCTIONS	
ENTER	Format stack for procedure entry
LEAVE	Restore stack for procedure exit
BOUND	Detects values outside prescribed range

Figure 4. iAPX 186 Instruction Set

CONDITIONAL TRANSFERS		UNCONDITIONAL TRANSFERS	
JA JNBE	Jump if above not below nor equal	CALL	Call procedure
JAE JNB	Jump if above or equal not below	RET	Return from procedure
JB JNAE	Jump if below not above nor equal	JMP	Jump
JBE JNA	Jump if below or equal not above		
JC	Jump if carry	**ITERATION CONTROLS**	
JE JZ	Jump if equal zero		
JG JNLE	Jump if greater not less nor equal	LOOP	Loop
JGE JNL	Jump if greater or equal not less	LOOPE LOOPZ	Loop if equal zero
JL JNGE	Jump if less not greater nor equal	LOOPNE LOOPNZ	Loop if not equal not zero
JLE JNG	Jump if less or equal not greater	JCXZ	Jump if register CX = 0
JNC	Jump if not carry		
JNE JNZ	Jump if not equal not zero	**INTERRUPTS**	
JNO	Jump if not overflow		
JNP JPO	Jump if not parity parity odd	INT	Interrupt
JNS	Jump if not sign	INTO	Interrupt if overflow
JO	Jump if overflow	IRET	Interrupt return
JP JPE	Jump if parity parity even		
JS	Jump if sign		

Figure 4. iAPX 186 Instruction Set (continued)

To access operands that do not reside in one of the four immediately available segments, a full 32-bit pointer can be used to reload both the base (segment) and offset values.

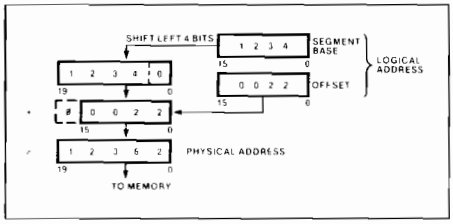


Figure 5. Two Component Address

Table 3. Segment Register Selection Rules

Memory Reference Needed	Segment Register Used	Implicit Segment Selection Rule
Instructions	Code (CS)	Instruction prefetch and immediate data.
Stack	Stack (SS)	All stack pushes and pops; any memory references which use BP Register as a base register.
External Data (Global)	Extra (ES)	All string instruction references which use the DI register as an index.
Local Data	Data (DS)	All other data references.

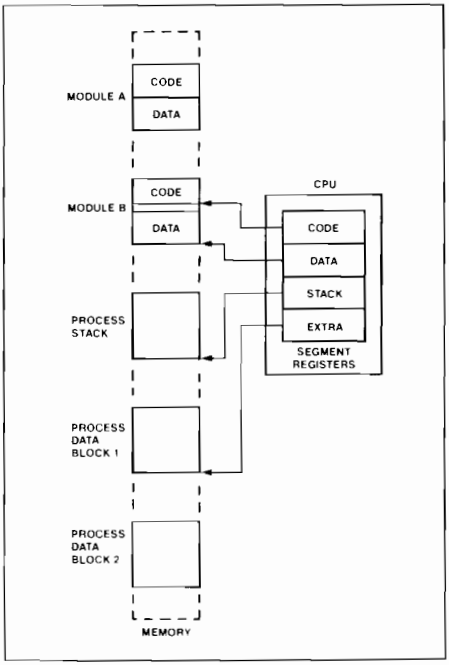


Figure 6. Segmented Memory Helps Structure Software

Addressing Modes

The 80186 provides eight categories of addressing modes to specify operands. Two addressing modes are provided for instructions that operate on register or immediate operands:

- *Register Operand Mode:* The operand is located in one of the 8- or 16-bit general registers.
- *Immediate Operand Mode:* The operand is included in the instruction.

Six modes are provided to specify the location of an operand in a memory segment. A memory operand address consists of two 16-bit components: a segment base and an offset. The segment base is supplied by a 16-bit segment register either implicity chosen by the addressing mode or explicitly chosen by a segment override prefix. The offset, also called the effective address, is calculated by summing any combination of the following three address elements:

- the *displacement* (an 8- or 16-bit immediate value contained in the instruction);
- the *base* (contents of either the BX or BP base registers); and
- the *index* (contents of either the SI or DI index registers).

Any carry out from the 16-bit addition is ignored. Eight-bit displacements are sign extended to 16-bit values.

Combinations of these three address elements define the six memory addressing modes, described below.

- *Direct Mode:* The operand's offset is contained in the instruction as an 8- or 16-bit displacement element.
- *Register Indirect Mode:* The operand's offset is in one of the registers SI, DI, BX, or BP.
- *Based Mode:* The operand's offset is the sum of an 8- or 16-bit displacement and the contents of a base register (BX or BP).
- *Indexed Mode:* The operand's offset is the sum of an 8- or 16-bit displacement and the contents of an index register (SI or DI).
- *Based Indexed Mode:* The operand's offset is the sum of the contents of a base register and an index register.
- *Based Indexed Mode with Displacement:* The operand's offset is the sum of a base register's contents, an index register's contents, and an 8- or 16-bit displacement.

Data Types

The 80186 directly supports the following data types:

- *Integer:* A signed binary numeric value contained in an 8-bit byte or a 16-bit word. All operations assume a 2's complement representation. Signed 32- and 64-bit integers are supported using the iAPX 186/20 Numeric Data Processor.
- *Ordinal:* An unsigned binary numeric value contained in an 8-bit byte or a 16-bit word.
- *Pointer:* A 16- or 32-bit quantity, composed of a 16-bit offset component or a 16-bit segment base component in addition to a 16-bit offset component.
- *String:* A contiguous sequence of bytes or words. A string may contain from 1 to 64K bytes.
- *ASCII:* A byte representation of alphanumeric and control characters using the ASCII standard of character representation.
- *BCD:* A byte (unpacked) representation of the decimal digits 0–9.
- *Packed BCD:* A byte (packed) representation of two decimal digits (0–9). One digit is stored in each nibble (4-bits) of the byte.
- *Floating Point:* A signed 32-, 64-, or 80-bit real number representation. (Floating point operands are supported using the iAPX 186/20 Numeric Data Processor configuration.)

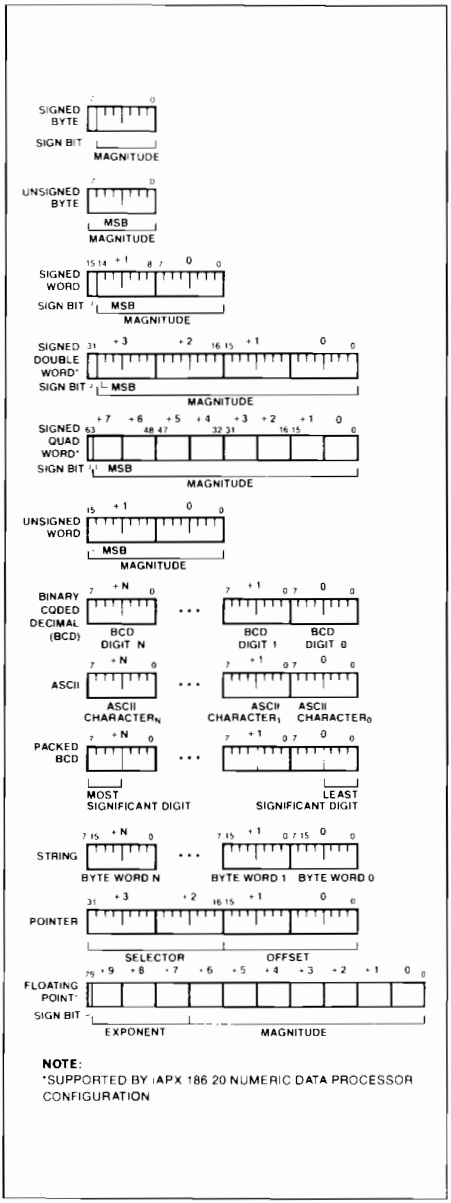
In general, individual data elements must fit within defined segment limits. Figure 7 graphically represents the data types supported by the iAPX 186.

I/O Space

The I/O space consists of 64K 8-bit or 32K 16-bit ports. Separate instructions address the I/O space with either an 8-bit port address, specified in the instruction, or a 16-bit port address in the DX register. 8-bit port addresses are zero extended such that A_{15}-A_8 are LOW. I/O port addresses 00F8(H) through 00FF(H) are reserved.

Interrupts

An interrupt transfers execution to a new program location. The old program address (CS:IP) and machine state (Status Word) are saved on the stack to allow resumption of the interrupted program. Interrupts fall into three classes: hardware initiated, INT instructions, and instruction exceptions. Hardware initiated interrupts occur in response to an external input and are classified as non-maskable or maskable.



NOTE:
*SUPPORTED BY iAPX 186 20 NUMERIC DATA PROCESSOR CONFIGURATION

Figure 7. iAPX 186 Supported Data Types

Programs may cause an interrupt with an INT instruction. Instruction exceptions occur when an unusual condition, which prevents further instruction processing, is detected while attempting to execute an instruction. If the exception was caused by executing an ESC instruction with the ESC trap bit set in the relocation register, the return instruction will point to the ESC instruction, or to the segment override prefix immediately preceding the ESC instruction if the prefix was present. In all other cases, the return address from an exception will point at the instruction immediately following the instruction causing the exception.

A table containing up to 256 pointers defines the proper interrupt service routine for each interrupt. Interrupts 0–31, some of which are used for instruction exceptions, are reserved. Table 4 shows the 80186 predefined types and default priority levels. For each interrupt, an 8-bit vector must be supplied to the 80186 which identifies the appropriate table entry. Exceptions supply the interrupt vector internally. In addition, internal peripherals and non-cascaded external interrupts will generate their own vectors through the internal interrupt controller. INT instructions contain or imply the vector and allow access to all 256 interrupts. Maskable hardware initiated interrupts supply the 8-bit vector to the CPU during an interrupt acknowledge bus sequence. Non-maskable hardware interrupts use a predefined internally supplied vector.

Interrupt Sources

The 80186 can service interrupts generated by software or hardware. The software interrupts are generated by specific instructions (INT, ESC, unused OP, etc.) or the results of conditions specified by instructions (array bounds check, INT0, DIV, IDIV, etc.). All interrupt sources are serviced by an indirect call through an element of a vector table. This vector table is indexed by using the interrupt vector type (Table 4), multiplied by four. All hardware-generated interrupts are sampled at the end of each instruction. Thus, the software interrupts will begin service first. Once the service routine is entered and interrupts are enabled, any hardware source of sufficient priority can interrupt the service routine in progress.

The software generated 80186 interrupts are described below.

DIVIDE ERROR EXCEPTION (TYPE 0)
Generated when a DIV or IDIV instruction quotient cannot be expressed in the number of bits in the destination.

Table 4. 80186 Interrupt Vectors

Interrupt Name	Vector Type	Default Priority	Related Instructions
Divide Error Exception	0	*1	DIV, IDIV
Single Step Interrupt	1	12**2	All
NMI	2	1	All
Breakpoint Interrupt	3	*1	INT
INT0 Detected Overflow Exception	4	*1	INT0
Array Bounds Exception	5	*1	BOUND
Unused-Opcode Exception	6	*1	Undefined Opcodes
ESC Opcode Exception	7	*1***	ESC Opcodes
Timer 0 Interrupt	8	2A****	
Timer 1 Interrupt	18	2B****	
Timer 2 Interrupt	19	2C****	
Reserved	9	3	
DMA 0 Interrupt	10	4	
DMA 1 Interrupt	11	5	
INT0 Interrupt	12	6	
INT1 Interrupt	13	7	
INT2 Interrupt	14	8	
INT3 Interrupt	15	9	

NOTES:

*1 These are generated as the result of an instruction execution.

**2. This is handled as in the 8086.

****3. All three timers constitute one source of request to the interrupt controller. The Timer interrupts all have the same default priority level with respect to all other interrupt sources. However, they have a defined priority ordering amongst themselves. (Priority 2A is higher priority than 2B.) Each Timer interrupt has a separate vector type number.

4 Default priorities for the interrupt sources are used only if the user does not program each source into a unique priority level.

***5. An escape opcode will cause a trap only if the proper bit is set in the peripheral control block relocation register.

SINGLE-STEP INTERRUPT (TYPE 1)
Generated after most instructions if the TF flag is set. Interrupts will not be generated after prefix instructions (e.g., REP), instructions which modify segment registers (e.g., POP DS), or the WAIT instruction.

NON-MASKABLE INTERRUPT—NMI (TYPE 2)
An external interrupt source which cannot be masked.

BREAKPOINT INTERRUPT (TYPE 3)
A one-byte version of the INT instruction. It uses 12 as an index into the service routine address table (because it is a type 3 interrupt).

INT0 DETECTED OVERFLOW EXCEPTION (TYPE 4)
Generated during an INT0 instruction if the 0F bit is set.

ARRAY BOUNDS EXCEPTION (TYPE 5)
Generated during a BOUND instruction if the array index is outside the array bounds. The array bounds are located in memory at a location indicated by one of the instruction operands. The other operand indicates the value of the index to be checked.

UNUSED OPCODE EXCEPTION (TYPE 6)
Generated if execution is attempted on undefined opcodes.

ESCAPE OPCODE EXCEPTION (TYPE 7)
Generated if execution is attempted of ESC opcodes (D8H–DFH). This exception will only be generated if a bit in the relocation register is set. The return address of this exception will point to the ESC instruction causing the exception. If a segment override prefix preceded the ESC instruction, the return address will point to the segment override prefix.

Hardware-generated interrupts are divided into two groups: maskable interrupts and non-maskable interrupts. The 80186 provides maskable hardware interrupt request pins INT0–INT3. In addition, maskable interrupts may be generated by the 80186 integrated DMA controller and the integrated timer unit. The vector types for these interrupts is shown in Table 4. Software enables these inputs by setting the interrupt flag bit (IF) in the Status Word. The interrupt controller is discussed in the peripheral section of this data sheet.

Further maskable interrupts are disabled while servicing an interrupt because the IF bit is reset as part of the response to an interrupt or exception. The saved Status Word will reflect the enable status of the processor prior to the interrupt. The interrupt flag will remain zero unless specifically set. The interrupt return instruction restores the Status Word, thereby restoring the original status of IF bit. If the interrupt return re-enables interrupts, and another interrupt is pending, the 80186 will immediately service the highest-priority interrupt pending, i.e., no instructions of the main line program will be executed.

Non-Maskable Interrupt Request (NMI)

A non-maskable interrupt (NMI) is also provided. This interrupt is serviced regardless of the state of the IF bit. A typical use of NMI would be to activate a power failure routine. The activation of this input

causes an interrupt with an internally supplied vector value of 2. No external interrupt acknowledge sequence is performed. The IF bit is cleared at the beginning of an NMI interrupt to prevent maskable interrupts from being serviced.

Single-Step Interrupt

The 80186 has an internal interrupt that allows programs to execute one instruction at a time. It is called the single-step interrupt and is controlled by the single-step flag bit (TF) in the Status Word. Once this bit is set, an internal single-step interrupt will occur after the next instruction has been executed. The interrupt clears the TF bit and uses an internally supplied vector of 1. The IRET instruction is used to set the TF bit and transfer control to the next instruction to be single-stepped.

Initialization and Processor Reset

Processor initialization or startup is accomplished by driving the $\overline{RES}$ input pin LOW. $\overline{RES}$ forces the 80186 to terminate all execution and local bus activity. No instruction or bus activity will occur as long as $\overline{RES}$ is active. After $\overline{RES}$ becomes inactive and an internal processing interval elapses, the 80186 begins execution with the instruction at physical location FFFF0(H). $\overline{RES}$ also sets some registers to predefined values as shown in Table 5.

Table 5. 80186 Initial Register State after RESET

Status Word	F002(H)
Instruction Pointer	0000(H)
Code Segment	FFFF(H)
Data Segment	0000(H)
Extra Segment	0000(H)
Stack Segment	0000(H)
Relocation Register	20FF(H)
UMCS	FFFB(H)

iAPX 186 CLOCK GENERATOR

The iAPX 186 provides an on-chip clock generator for both internal and external clock generation. The clock generator features a crystal oscillator, a divide-by-two counter, synchronous and asynchronous ready inputs, and reset circuitry.

Oscillator

The oscillator circuit of the iAPX 186 is designed to be used with a parallel resonant fundamental mode crystal. This is used as the time base for the iAPX 186. The crystal frequency selected will be double the CPU clock frequency. Use of an LC or RC circuit is not recommended with this oscillator. If an external oscillator is used, it can be connected directly to input pin X1 in lieu of a crystal. The output of the oscillator is not directly available outside the iAPX 186. The recommended crystal configuration is shown in Figure 8.

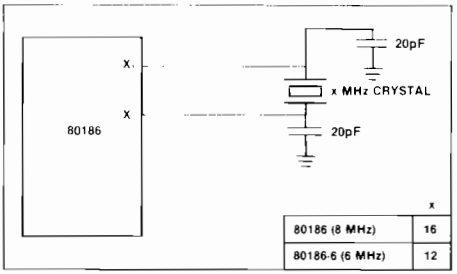


Figure 8. Recommended iAPX 186 Crystal Configuration

Clock Generator

The iAPX 186 clock generator provides the 50% duty cycle processor clock for the iAPX 186. It does this by dividing the oscillator output by 2 forming the symmetrical clock. If an external oscillator is used, the state of the clock generator will change on the falling edge of the oscillator signal. The CLKOUT pin provides the processor clock signal for use outside the iAPX 186. This may be used to drive other system components. All timings are referenced to the output clock.

READY Synchronization

The iAPX 186 provides both synchronous and asynchronous ready inputs. Asynchronous ready synchronization is accomplished by circuitry which samples ARDY in the middle of T_2, T_3 and again in the middle of each T_W until ARDY is sampled HIGH. One-half CLKOUT cycle of resolution time is used. Full synchronization is performed only on the rising edge of ARDY, i.e., the falling edge of ARDY must be synchronized to the CLKOUT signal if it will occur during T_2, T_3 or T_W. High-to-LOW transitions of ARDY must be performed synchronously to the CPU clock.

A second ready input (SRDY) is provided to interface with externally synchronized ready signals. This input is sampled at the end of T_2, T_3 and again at the end of each T_W until it is sampled HIGH. By using this input rather than the asynchronous ready input, the half-clock cycle resolution time penalty is eliminated.

This input must satisfy set-up and hold times to guarantee proper operation of the circuit.

In addition, the iAPX 186, as part of the integrated chip-select logic, has the capability to program WAIT states for memory and peripheral blocks. This is discussed in the Chip Select/Ready Logic description.

RESET Logic

The iAPX 186 provides both a $\overline{RES}$ input pin and a synchronized RESET pin for use with other system components. The $\overline{RES}$ input pin on the iAPX 186 is provided with hysteresis in order to facilitate power-on Reset generation via an RC network. RESET is guaranteed to remain active for at least five clocks given a $\overline{RES}$ input of at least six clocks. RESET may be delayed up to two and one-half clocks behind $\overline{RES}$.

Multiple iAPX 186 processors may be synchronized through the $\overline{RES}$ input pin, since this input resets both the processor and divide-by-two internal counter in the clock generator. In order to insure that the divide-by-two counters all begin counting at the same time, the active going edge of $\overline{RES}$ must satisfy a 25 ns setup time before the falling edge of the 80186 clock input. In addition, in order to insure that all CPUs begin executing in the same clock cycle, the reset must satisfy a 25 ns setup time before the rising edge of the CLKOUT signal of all the processors.

LOCAL BUS CONTROLLER

The iAPX 186 provides a local bus controller to generate the local bus control signals. In addition, it employs a HOLD/HLDA protocol for relinquishing the local bus to other bus masters. It also provides control lines that can be used to enable external buffers and to direct the flow of data on and off the local bus.

Memory/Peripheral Control

The iAPX 186 provides ALE, $\overline{RD}$, and $\overline{WR}$ bus control signals. The $\overline{RD}$ and $\overline{WR}$ signals are used to strobe data from memory to the iAPX 186 or to strobe data from the iAPX 186 to memory. The ALE line provides a strobe to address latches for the multiplexed address/data bus. The iAPX 186 local bus controller does not provide a memory/$\overline{I/O}$ signal. If this is required, the user will have to use the $\overline{S2}$ signal (which will require external latching), make the memory and I/O spaces nonoverlapping, or use only the integrated chip-select circuitry.

Transceiver Control

The iAPX 186 generates two control signals to be connected to 8286/8287 transceiver chips. This capability allows the addition of transceivers for extra buffering without adding external logic. These control lines, DT/$\overline{R}$ and $\overline{DEN}$, are generated to control the flow of data through the transceivers. The operation of these signals is shown in Table 6.

Table 6. Transceiver Control Signals Description

Pin Name	Function
$\overline{DEN}$ (Data Enable)	Enables the output drivers of the transceivers. It is active LOW during memory, I/O, or INTA cycles.
DT/$\overline{R}$ (Data Transmit/Receive)	Determines the direction of travel through the transceivers. A HIGH level directs data away from the processor during write operations, while a LOW level directs data toward the processor during a read operation.

Local Bus Arbitration

The iAPX 186 uses a HOLD/HLDA system of local bus exchange. This provides an asynchronous bus exchange mechanism. This means multiple masters utilizing the same bus can operate at separate clock frequencies. The iAPX 186 provides a single HOLD/HLDA pair through which all other bus masters may gain control of the local bus. This requires external circuitry to arbitrate which external device will gain control of the bus from the iAPX 186 when there is more than one alternate local bus master. When the iAPX 186 relinquishes control of the local bus, it floats $\overline{DEN}$, $\overline{RD}$, $\overline{WR}$, $\overline{S0}$–$\overline{S2}$, $\overline{LOCK}$, AD0–AD15, A16–A19, $\overline{BHE}$, and DT/$\overline{R}$ to allow another master to drive these lines directly.

The iAPX 186 HOLD latency time, i.e., the time between HOLD request and HOLD acknowledge, is a function of the activity occurring in the processor when the HOLD request is received. A HOLD request is the highest-priority activity request which the processor may receive: higher than instruction fetching or internal DMA cycles. However, if a DMA cycle is in progress, the iAPX 186 will complete the transfer before relinquishing the bus. This implies that if a HOLD request is received just as a DMA transfer begins, the HOLD latency time can be as great as 4 bus cycles. This will occur if a DMA word transfer operation is taking place from an odd address to an odd address. This is a total of 16 clocks or more, if WAIT states are required. In addition, if locked transfers are performed, the HOLD latency time will be increased by the length of the locked transfer.

Local Bus Controller and Reset

Upon receipt of a RESET pulse from the $\overline{RES}$ input, the local bus controller will perform the following actions:

- Drive $\overline{DEN}$, $\overline{RD}$, and $\overline{WR}$ HIGH for one clock cycle, then float.

  NOTE: $\overline{RD}$ is also provided with an internal pull-up device to prevent the processor from inadvertently entering Queue Status mode during reset.

- Drive $\overline{S0}$–$\overline{S2}$ to the passive state (all HIGH) and then float.
- Drive $\overline{LOCK}$ HIGH and then float.
- Tristate AD0–15, A16–19, $\overline{BHE}$, DT/$\overline{R}$.
- Drive ALE LOW (ALE is never floated).
- Drive HLDA LOW.

INTERNAL PERIPHERAL INTERFACE

All the iAPX 186 integrated peripherals are controlled via 16-bit registers contained within an internal 256-byte control block. This control block may be mapped into either memory or I/O space. Internal logic will recognize the address and respond to the bus cycle. During bus cycles to internal registers, the bus controller will signal the operation externally (i.e., the $\overline{RD}$, $\overline{WR}$, status, address, data, etc., lines will be driven as in a normal bus cycle), but D_{15-0}, SRDY, and ARDY will be ignored. The base address of the control block must be on an even 256-byte boundary (i.e., the lower 8 bits of the base address are all zeros). All of the defined registers within this control block may be read or written by the 80186 CPU at any time. The location of any register contained within the 256-byte control block is determined by the current base address of the control block.

The control block base address is programmed via a 16-bit relocation register contained within the control block at offset FEH from the base address of the control block (see Figure 9). It provides the upper 12 bits of the base address of the control block. Note that mapping the control register block into an address range corresponding to a chip-select range is not recommended (the chip select circuitry is discussed later in this data sheet). In addition, bit 12 of this register determines whether the control block will be mapped into I/O or memory space. If this bit is 1, the control block will be located in memory space, whereas if the bit is 0, the control block will be located in I/O space. If the control register block is mapped into I/O space, the upper 4 bits of the base address must be programmed as 0 (since I/O addresses are only 16 bits wide).

In addition to providing relocation information for the control block, the relocation register contains bits which place the interrupt controller into iRMX mode, and cause the CPU to interrupt upon encountering ESC instructions. At RESET, the relocation register is set to 20FFH. This causes the control block to start at FF00H in I/O space. An offset map of the 256-byte control register block is shown in Figure 10.

The integrated iAPX 186 peripherals operate semi-autonomously from the CPU. Access to them for the most part is via software read/write of the control and data locations in the control block. Most of these registers can be both read and written. A few dedicated lines, such as interrupts and DMA request provide real-time communication between the CPU and peripherals as in a more conventional system utilizing discrete peripheral blocks. The overall interaction and function of the peripheral blocks has not substantially changed.

CHIP-SELECT/READY GENERATION LOGIC

The iAPX 186 contains logic which provides programmable chip-select generation for both memories and peripherals. In addition, it can be programmed to provide READY (or WAIT state) generation. It can also provide latched address bits A1 and A2. The chip-select lines are active for all memory and I/O cycles in their programmed areas, whether they be generated by the CPU or by the integrated DMA unit.

Memory Chip Selects

The iAPX 186 provides 6 memory chip select outputs for 3 address areas: upper memory, lower memory, and midrange memory. One each is provided for upper memory and lower memory, while four are provided for midrange memory.

The range for each chip select is user-programmable and can be set to 2K, 4K, 8K, 16K, 32K, 64K, 128K (plus 1K and 256K for upper and lower chip selects). In addition, the beginning or base address of the midrange memory chip select may also be selected. Only one chip select may be programmed to be active for any memory location at a time. All chip select sizes are in bytes, whereas iAPX 186 memory is arranged in words. This means that if, for example, 16 64K x 1 memories are used, the memory block size will be 128K, not 64K.

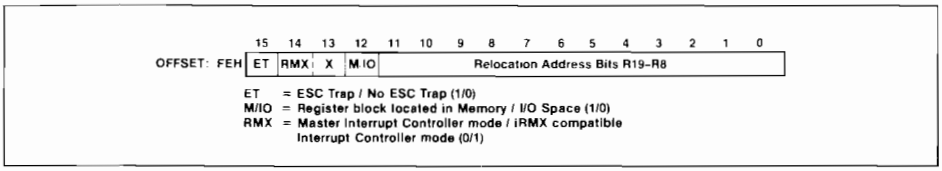


Figure 9. Relocation Register

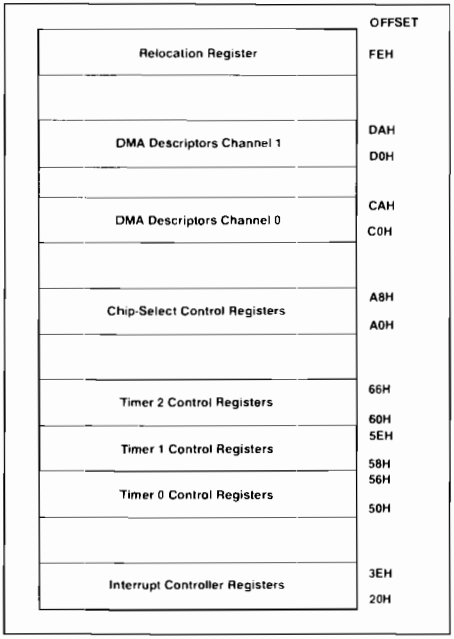


Figure 10. Internal Register Map

Upper Memory $\overline{CS}$

The iAPX 186 provides a chip select, called UCS, for the top of memory. The top of memory is usually used as the system memory because after reset the iAPX 186 begins executing at memory location FFFF0H.

The upper limit of memory defined by this chip select is always FFFFFH, while the lower limit is programmable. By programming the lower limit, the size of the select block is also defined. Table 7 shows the relationship between the base address selected and the size of the memory block obtained.

Table 7. UMCS Programming Values

Starting Address (Base Address)	Memory Block Size	UMCS Value (Assuming R0=R1=R2=0)
FFC00	1K	FFF8H
FF800	2K	FFB8H
FF000	4K	FF38H
FE000	8K	FE38H
FC000	16K	FC38H
F8000	32K	F838H
F0000	64K	F038H
E0000	128K	E038H
C0000	256K	C038H

The lower limit of this memory block is defined in the UMCS register (see Figure 11). This register is at offset A0H in the internal control block. The legal values for bits 6–13 and the resulting starting address and memory block sizes are given in Table 7. Any combination of bits 6–13 not shown in Table 7 will result in undefined operation. After reset, the UMCS register is programmed for a 1K area. It must be reprogrammed if a larger upper memory area is desired.

Any internally generated 20-bit address whose upper 16 bits are greater than or equal to UMCS (with bits 0–5 "0") will cause UCS to be activated. UMCS bits R2–R0 are used to specify READY mode for the area of memory defined by this chip-select register, as explained below.

Lower Memory $\overline{CS}$

The iAPX 186 provides a chip select for low memory called $\overline{LCS}$. The bottom of memory contains the interrupt vector table, starting at location 00000H.

The lower limit of memory defined by this chip select is always 0H, while the upper limit is programmable. By programming the upper limit, the size of the memory block is also defined. Table 8 shows the relationship between the upper address selected and the size of the memory block obtained.

Table 8. LMCS Programming Values

Upper Address	Memory Block Size	LMCS Value (Assuming R0=R1 R2 0)
003FFH	1K	0038H
007FFH	2K	0078H
00FFFH	4K	00F8H
01FFFH	8K	01F8H
03FFFH	16K	03F8H
07FFFH	32K	07F8H
0FFFFH	64K	0FF8H
1FFFFH	128K	1FF8H
3FFFFH	256K	3FF8H

The upper limit of this memory block is defined in the LMCS register (see Figure 12). This register is at offset A2H in the internal control block. The legal values for bits 6–15 and the resulting upper address and memory block sizes are given in Table 8. Any combination of bits 6–15 not shown in Table 8 will result in undefined operation. After reset, the LMCS register value is undefined. However, the $\overline{LCS}$ chip-select line will not become active until the LMCS register is accessed.

Any internally generated 20-bit address whose upper 16 bits are less than or equal to LMCS (with bits 0–5 "1") will cause $\overline{LCS}$ to be active. LMCS register bits R2–R0 are used to specify the READY mode for the area of memory defined by this chip-select register.

Mid-Range Memory $\overline{CS}$

The iAPX 186 provides four $\overline{MCS}$ lines which are active within a user-locatable memory block. This block can be located anywhere within the iAPX 186 1M byte memory address space exclusive of the areas defined by $\overline{UCS}$ and $\overline{LCS}$. Both the base address and size of this memory block are programmable.

The size of the memory block defined by the mid-range select lines, as shown in Table 9, is determined by bits 8–14 of the MPCS register (see Figure 13). This register is at location A8H in the internal control block. One and only one of bits 8–14 must be set at a time. Unpredictable operation of the $\overline{MCS}$ lines will otherwise occur. Each of the four chip-select lines is active for one of the four equal contiguous divisions of the mid-range block. Thus, if the total block size is 32K, each chip select is active for 8K of memory with $\overline{MCS0}$ being active for the first range and MCS3 being active for the last range.

The EX and MS in MPCS relate to peripheral functionality as descibed a later section.

Table 9. MPCS Programming Values

Total Block Size	Individual Select Size	MPCS Bits 14–8
8K	2K	0000001B
16K	4K	0000010B
32K	8K	0000100B
64K	16K	0001000B
128K	32K	0010000B
256K	64K	0100000B
512K	128K	1000000B

The base address of the mid-range memory block is defined by bits 15–9 of the MMCS register (see Figure 14). This register is at offset A6H in the internal control block. These bits correspond to bits A19–A13 of the 20-bit memory address. Bits A12–A0 of the base address are always 0. The base address may be set at any integer multiple of the size of the total memory block selected. For example, if the mid-range block size is 32K (or the size of the block for which each $\overline{MCS}$ line is active is 8K), the block could be located at 10000H or 18000H, but not at 14000H, since the first few integer multiples of a 32K memory block are 0H, 8000H, 10000H, 18000H, etc. After reset, the contents of both of these registers is undefined. However, none of the $\overline{MCS}$ lines will be active until both the MMCS and MPCS registers are accessed.

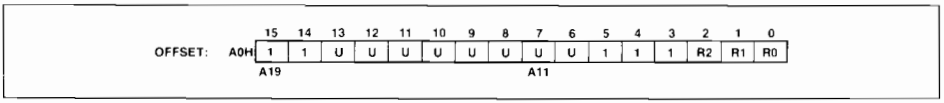


Figure 11. UMCS Register

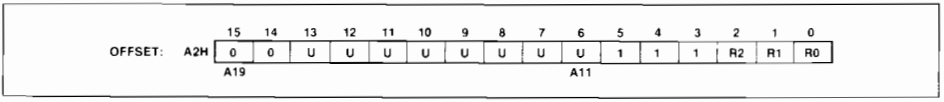


Figure 12. LMCS Register

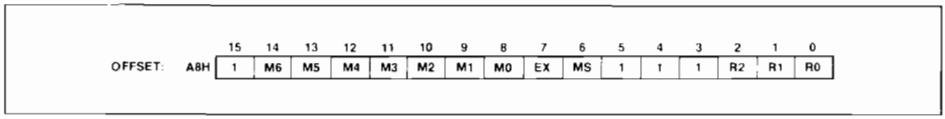


Figure 13. MPCS Register

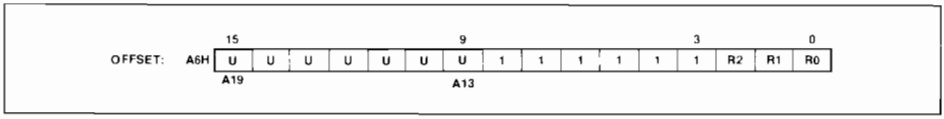


Figure 14. MMCS Register

MMCS bits R2–R0 specify READY mode of operation for all mid-range chip selects. All devices in mid-range memory must use the same number of WAIT states.

The 512K block size for the mid-range memory chip selects is a special case. When using 512K, the base address would have to be at either locations 00000H or 80000H. If it were to be programmed at 00000H when the $\overline{LCS}$ line was programmed, there would be an internal conflict between the $\overline{LCS}$ ready generation logic and the $\overline{MCS}$ ready generation logic. Likewise, if the base address were programmed at 80000H, there would be a conflict with the $\overline{UCS}$ ready generation logic. Since the $\overline{LCS}$ chip-select line does not become active until programmed, while the $\overline{UCS}$ line is active at reset, the memory base can be set only at 00000H. If this base address is selected, however, the $\overline{LCS}$ range must not be programmed.

Peripheral Chip Selects

The iAPX 186 can generate chip selects for up to seven peripheral devices. These chip selects are active for seven contiguous blocks of 128 bytes above a programmable base address. This base address may be located in either memory or I/O space.

Seven $\overline{CS}$ lines called $\overline{PCS0}$–6 are generated by the iAPX 186. The base address is user-programmable; however it can only be a multiple of 1K bytes, i.e., the least significant 10 bits of the starting address are always 0.

$\overline{PCS5}$ and $\overline{PCS6}$ can also be programmed to provide latched address bits A1, A2. If so programmed, they cannot be used as peripheral selects. These outputs can be connected directly to the A0, A1 pins used for selecting internal registers of 8-bit peripheral chips. This scheme simplifies the hardware interface because the 8-bit registers of peripherals are simply treated as 16-bit registers located on even boundaries in I/O space or memory space where only the lower 8-bits of the register are significant: the upper 8-bits are "don't cares."

The starting address of the peripheral chip-select block is defined by the PACS register (see Figure 15). This register is located at offset A4H in the internal control block. Bits 15–6 of this register correspond to bits 19–10 of the 20-bit Programmable Base Address (PBA) of the peripheral chip-select block. Bits 9–0 of the PBA of the peripheral chip-select block are all zeros. If the chip-select block is located in I/O space, bits 12–15 must be programmed zero, since the I/O address is only 16 bits wide. Table 10 shows the address range of each peripheral chip select with respect to the PBA contained in PACS register.

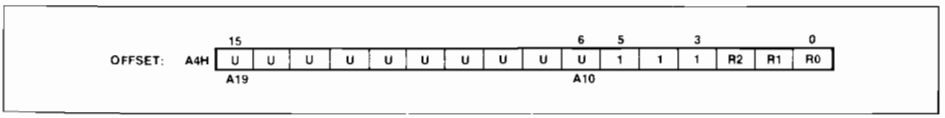


Figure 15. PACS Register

The user should program bits 15–6 to correspond to the desired peripheral base location. PACS bits 0–2 are used to specify READY mode for $\overline{PCS0}$–$\overline{PCS3}$.

Table 10. PCS Address Ranges

PCS Line	Active between Locations
PCS0	PBA — PBA+127
PCS1	PBA+128 — PBA+255
PCS2	PBA+256 — PBA+383
PCS3	PBA+384 — PBA+511
PCS4	PBA+512 — PBA+639
PCS5	PBA+640 — PBA+767
PCS6	PBA+768 — PBA+895

The mode of operation of the peripheral chip selects is defined by the MPCS register (which is also used to set the size of the mid-range memory chip-select block, see Figure 16). This register is located at offset A8H in the internal control block. Bit 7 is used to select the function of $\overline{PCS5}$ and $\overline{PCS6}$, while bit 6 is used to select whether the peripheral chip selects are mapped into memory or I/O space. Table 11 describes the programming of these bits. After reset, the contents of both the MPCS and the PACS registers are undefined, however none of the PCS lines will be active until both of the MPCS and PACS registers are accessed.

Table 11. MS, EX Programming Values

Bit	Description
MS	1 = Peripherals mapped into memory space. 0 = Peripherals mapped into I/O space.
EX	0 = 5 $\overline{PCS}$ lines. A1, A2 provided. 1 = 7 $\overline{PCS}$ lines. A1, A2 are not provided.

MPCS bits 0–2 are used to specify READY mode for $\overline{PCS4}$–$\overline{PCS6}$ as outlined below.

READY Generation Logic

The iAPX 186 can generate a "READY" signal internally for each of the memory or peripheral $\overline{CS}$ lines. The number of WAIT states to be inserted for each peripheral or memory is programmable to provide 0–3 wait states for all accesses to the area for which the chip select is active. In addition, the iAPX 186 may be programmed to either ignore external READY for each chip-select range individually or to factor external READY with the integrated ready generator.

READY control consists of 3 bits for each $\overline{CS}$ line or group of lines generated by the iAPX 186. The interpretation of the ready bits is shown in Table 12.

Table 12. READY Bits Programming

R2	R1	R0	Number of WAIT States Generated
0	0	0	0 wait states, external RDY also used.
0	0	1	1 wait state inserted, external RDY also used.
0	1	0	2 wait states inserted, external RDY also used.
0	1	1	3 wait states inserted, external RDY also used.
1	0	0	0 wait states, external RDY ignored.
1	0	1	1 wait state inserted, external RDY ignored.
1	1	0	2 wait states inserted, external RDY ignored.
1	1	1	3 wait states inserted, external RDY ignored.

The internal ready generator operates in parallel with external READY, not in series if the external READY is used (R2 = 0). This means, for example, if the internal generator is set to insert two wait states, but activity on the external READY lines will insert four wait states, the processor will only insert four wait states, not six. This is because the two wait states generated by the internal generator overlapped the first two wait states generated by the external ready signal. Note that the external ARDY and SRDY lines are always ignored during cycles accessing internal peripherals.

R2–R0 of each control word specifies the READY mode for the corresponding block, with the exception of the peripheral chip selects: R2–R0 of PACS set the $\overline{PCS0}$–3 READY mode, R2–R0 of MPCS set the $\overline{PCS4}$–6 READY mode.

Chip Select/Ready Logic and Reset

Upon reset, the Chip-Select/Ready Logic will perform the following actions:

- All chip-select outputs will be driven HIGH.
- Upon leaving RESET, the $\overline{UCS}$ line will be programmed to provide chip selects to a 1K block with the accompanying READY control bits set at 011 to

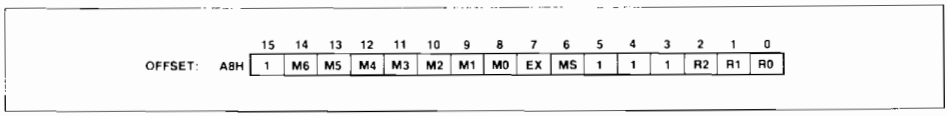


Figure 16. MPCS Register

allow the maximum number of internal wait states in conjunction with external Ready consideration (i.e., UMCS resets to FFFBH).

- No other chip select or READY control registers have any predefined values after RESET. They will not become active until the CPU accesses their control registers. Both the PACS and MPCS registers must be accessed before the $\overline{PCS}$ lines will become active.

DMA CHANNELS

The 80186 DMA controller provides two independent high-speed DMA channels. Data transfers can occur between memory and I/O spaces (e.g., Memory to I/O) or within the same space (e.g., Memory to Memory or I/O to I/O). Data can be transferred either in bytes (8 bits) or in words (16 bits) to or from even or odd addresses. Each DMA channel maintains both a 20-bit source and destination pointer which can be optionally incremented or decremented after each data transfer (by one or two depending on byte or word transfers). Each data transfer consumes 2 bus cycles (a minimum of 8 clocks), one cycle to fetch data and the other to store data. This provides a maximum data transfer rate of one Mword/sec or 2 MBytes/sec.

DMA Operation

Each channel has six registers in the control block which define each channel's specific operation. The control registers consist of a 20-bit Source pointer (2 words), a 20-bit Destination pointer (2 words), a 16-bit Transfer Counter, and a 16-bit Control Word. The format of the DMA Control Blocks is shown in Table 13. The Transfer Count Register (TC) specifies the number of DMA transfers to be performed. Up to 64K byte or word transfers can be performed with automatic termination. The Control Word defines the channel's operation (see Figure 18). All registers may be modified or altered during any DMA activity. Any changes made to these registers will be reflected immediately in DMA operation.

Table 13. DMA Control Block Format

Register Name	Register Address	
	Ch. 0	Ch. 1
Control Word	CAH	DAH
Transfer Count	C8H	D8H
Destination Pointer (upper 4 bits)	C6H	D6H
Destination Pointer	C4H	D4H
Source Pointer (upper 4 bits)	C2H	D2H
Source Pointer	C0H	D0H

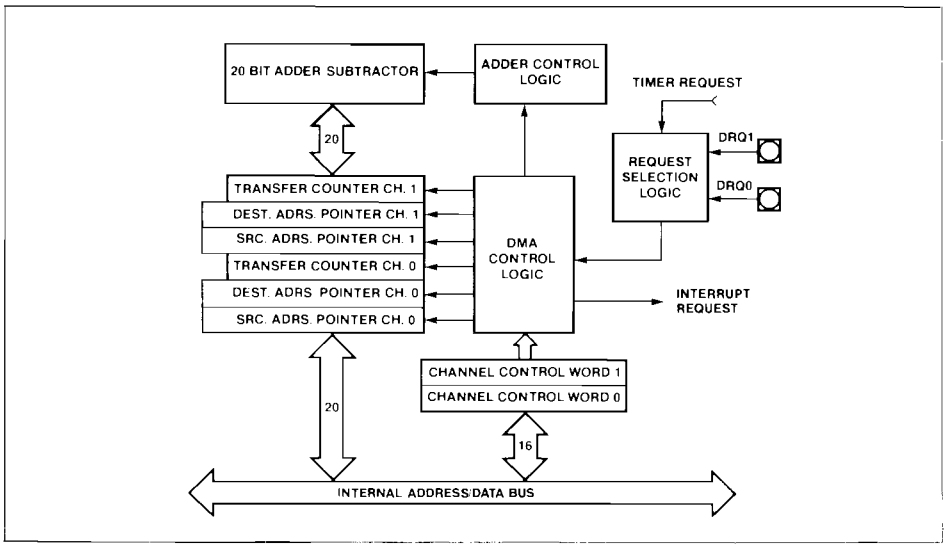


Figure 17. DMA Unit Block Diagram

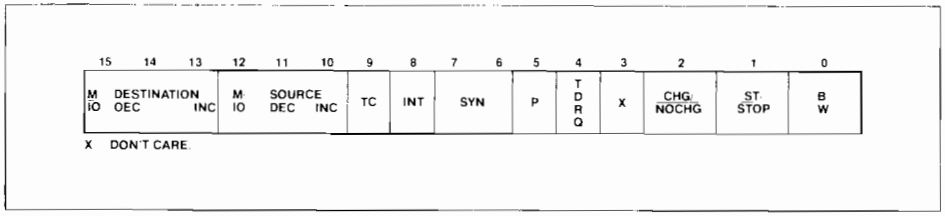


Figure 18. DMA Control Register

DMA Channel Control Word Register

Each DMA Channel Control Word determines the mode of operation for the particular 80186 DMA channel. This register specifies:

- the mode of synchronization;
- whether bytes or words will be transferred;
- whether interrupts will be generated after the last transfer;
- whether DMA activity will cease after a programmed number of DMA cycles;
- the relative priority of the DMA channel with respect to the other DMA channel;
- whether the source pointer will be incremented, decremented, or maintained constant after each transfer;
- whether the source pointer addresses memory or I/O space;
- whether the destination pointer will be incremented, decremented, or maintained constant after each transfer; and
- whether the destination pointer will address memory or I/O space.

The DMA channel control registers may be changed while the channel is operating. However, any changes made during operation will affect the current DMA transfer.

DMA Control Word Bit Descriptions

$\overline{B}$/W: Byte/Word (0/1) Transfers.

ST/$\overline{STOP}$: Start/stop (1/0) Channel.

CHG/$\overline{NOCHG}$: Change/Do not change (1/0) ST/$\overline{STOP}$ bit. If this bit is set when writing to the control word, the ST/$\overline{STOP}$ bit will be programmed by the write to the control word. If this bit is cleared when writing the control word, the ST/$\overline{STOP}$ bit will not be altered. This bit is not stored; it will always be a 0 on read.

INT: Enable Interrupts to CPU on Transfer Count termination.

TC: If set, DMA will terminate when the contents of the Transfer Count register reach zero. The ST/$\overline{STOP}$ bit will also be reset at this point if TC is set. If this bit is cleared, the DMA unit will decrement the transfer count register for each DMA cycle, but the DMA transfer will not stop when the contents of the TC register reach zero.

SYN: (2 bits)
- 00 No synchronization.
  NOTE: The ST bit will be cleared automatically when the contents of the TC register reach zero regardless of the state of the TC bit.
- 01 Source synchronization.
- 10 Destination synchronization.
- 11 Unused.

SOURCE:INC Increment source pointer by 1 or 2 (depends on $\overline{B}$/W) after each transfer.

M/$\overline{IO}$ Source pointer is in M/$\overline{IO}$ space (1/0).

DEC Decrement source pointer by 1 or 2 (depends on B/W) after each transfer.

DEST: INC Increment destination pointer by 1 or 2 ($\overline{B}$/W) after each transfer.

M/$\overline{IO}$ Destination pointer is in M/$\overline{IO}$ space (1/0).

DEC Decrement destination pointer by 1 or 2 (depending on $\overline{B}$/W) after each transfer.

P Channel priority—relative to other channel.
- 0 low priority.
- 1 high priority.

Channels will alternate cycles if both set at same priority level.

TDRQ	0: Disable DMA requests from timer 2. 1: Enable DMA requests from timer 2.
Bit 3	Bit 3 is not used.

If both INC and DEC are specified for the same pointer, the pointer will remain constant after each cycle.

DMA Destination and Source Pointer Registers

Each DMA channel maintains a 20-bit source and a 20-bit destination pointer. Each of these pointers takes up two full 16-bit registers in the peripheral control block. The lower four bits of the upper register contain the upper four bits of the 20-bit physical address (see Figure 18a). These pointers may be individually incremented or decremented after each transfer. If word transfers are performed the pointer is incremented or decremented by two. Each pointer may point into either memory or I/O space. Since the DMA channels can perform transfers to or from odd addresses, there is no restriction on values for the pointer registers. Higher transfer rates can be obtained if all word transfers are performed to even addresses, since this will allow data to be accessed in a single memory access.

DMA Transfer Count Register

Each DMA channel maintains a 16-bit transfer count register (TC). This register is decremented after every DMA cycle, regardless of the state of the TC bit in the DMA Control Register. If the TC bit in the DMA control word is set or unsynchronized transfers are programmed, however, DMA activity will terminate when the transfer count register reaches zero.

DMA Requests

Data transfers may be either source or destination synchronized, that is either the source of the data or the destination of the data may request the data transfer. In addition, DMA transfers may be unsynchronized; that is, the transfer will take place continually until the correct number of transfers has occurred. When source or unsynchronized transfers are performed, the DMA channel may begin another transfer immediately after the end of a previous DMA transfer. This allows a complete transfer to take place every 2 bus cycles or eight clock cycles (assuming no wait states). No prefetching occurs when destination synchronization is performed, however. Data will not be fetched from the source address until the destination device signals that it is ready to receive it. When destination synchronized transfers are requested, the DMA controller will relinquish control of the bus after every transfer. If no other bus activity is initiated, another DMA cycle will begin after two processor clocks. This is done to allow the destination device time to remove its request if another transfer is not desired. Since the DMA controller will relinquish the bus, the CPU can initiate a bus cycle. As a result, a complete bus cycle will often be inserted between destination synchronized transfers. These lead to the maximum DMA transfer rates shown in Table 14.

Table 14. Maximum DMA Transfer Rates

Type of Synchronization Selected	CPU Running	CPU Halted
Unsynchronized	2MBytes/sec	2MBytes/sec
Source Synch	2MBytes/sec	2MBytes/sec
Destination Synch	1.3MBytes/sec	1.5MBytes/sec

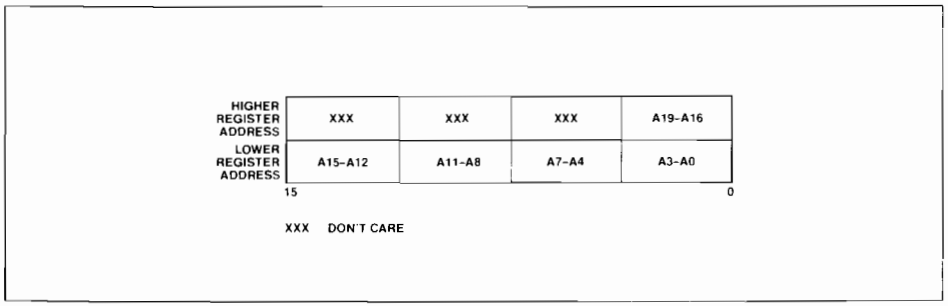


Figure 18a. DMA Memory Pointer Register Format

DMA Acknowledge

No explicit DMA acknowledge pulse is provided. Since both source and destination pointers are maintained, a read from a requesting source, or a write to a requesting destination, should be used as the DMA acknowledge signal. Since the chip-select lines can be programmed to be active for a given block of memory or I/O space, and the DMA pointers can be programmed to point to the same given block, a chip-select line could be used to indicate a DMA acknowledge.

DMA Priority

The DMA channels may be programmed such that one channel is always given priority over the other, or they may be programmed such as to alternate cycles when both have DMA requests pending. DMA cycles always have priority over internal CPU cycles except between locked memory accesses or word accesses the odd memory locations; however, an external bus hold takes priority over an internal DMA cycle. Because an interrupt request cannot suspend a DMA operation and the CPU cannot access memory during a DMA cycle, interrupt latency time will suffer during sequences of continuous DMA cycles. An NMI request, however, will cause all internal DMA activity to halt. This allows the CPU to quickly respond to the NMI request.

DMA Programming

DMA cycles will occur whenever the ST/STOP bit of the Control Register is set. If synchronized transfers are programmed, a DRQ must also have been generated. Therefore, the source and destination transfer pointers, and the transfer count register (if used) must be programmed before this bit is set.

Each DMA register may be modified while the channel is operating. If the CHG/NOCHG bit is cleared when the control register is written, the ST/STOP bit of the control register will not be modified by the write. If multiple channel registers are modified, it is recommended that a LOCKED string transfer be used to prevent a DMA transfer from occurring between updates to the channel registers.

DMA Channels and Reset

Upon RESET, the DMA channels will perform the following actions:

- The Start/Stop bit for each channel will be reset to STOP.
- Any transfer in progress is aborted.

TIMERS

The 80186 provides three internal 16-bit programmable timers (see Figure 19). Two of these are highly flexible and are connected to four external pins (2 per timer). They can be used to count external events, time external events, generate nonrepetitive waveforms, etc. The third timer is not connected to any external pins, and is useful for real-time coding and time delay applications. In addition, this third timer can be used as a prescaler to the other two, or as a DMA request source.

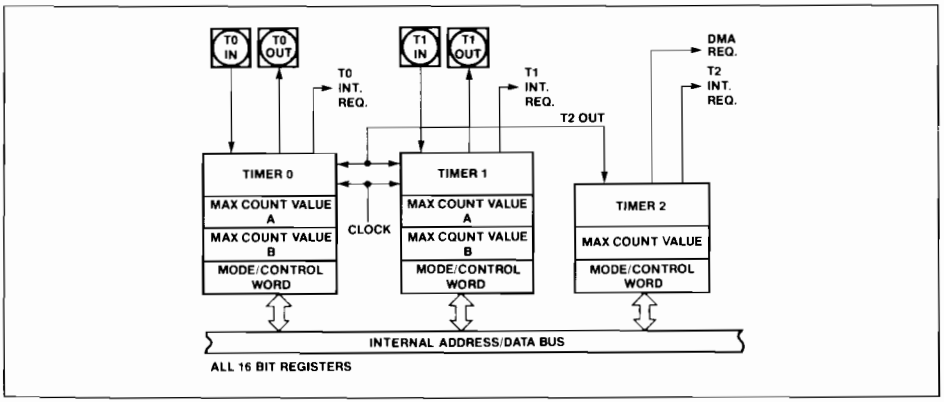


Figure 19. Timer Block Diagram

Timer Operation

The timers are controlled by 11 16-bit registers in the internal peripheral control block. The configuration of these registers is shown in Table 15. The count register contains the current value of the timer. It can be read or written at any time independent of whether the timer is running or not. The value of this register will be incremented for each timer event. Each of the timers is equipped with a MAX COUNT register, which defines the maximum count the timer will reach. After reaching the MAX COUNT register value, the timer count value will reset to zero during that same clock, i.e., the maximum count value is never stored in the count register itself. Timers 0 and 1 are, in addition, equipped with a second MAX COUNT register, which enables the timers to alternate their count between two different MAX COUNT values programmed by the user. If a single MAX COUNT register is used, the timer output pin will switch LOW for a single clock, 2 clocks after the maximum count value has been reached. In the dual MAX COUNT register mode, the output pin will indicate which MAX COUNT register is currently in use, thus allowing nearly complete freedom in selecting waveform duty cycles. For the timers with two MAX COUNT registers, the RIU bit in the control register determines which is used for the comparison.

Each timer gets serviced every fourth CPU-clock cycle, and thus can operate at speeds up to one-quarter the internal clock frequency (one-eighth the crystal rate). External clocking of the timers may be done at up to a rate of one-quarter of the internal CPU-clock rate (2 MHz for an 8 MHz CPU clock). Due to internal synchronization and pipelining of the timer circuitry, a timer output may take up to 6 clocks to respond to any individual clock or gate input.

Since the count registers and the maximum count registers are all 16 bits wide, 16 bits of resolution are provided. Any Read or Write access to the timers will add one wait state to the minimum four-clock bus cycle, however. This is needed to synchronize and coordinate the internal data flows between the internal timers and the internal bus.

The timers have several programmable options.

- All three timers can be set to halt or continue on a terminal count.
- Timers 0 and 1 can select between internal and external clocks, alternate between MAX COUNT registers and be set to retrigger on external events.
- The timers may be programmed to cause an interrupt on terminal count.

These options are selectable via the timer mode/control word.

Timer Mode/Control Register

The mode/control register (see Figure 20) allows the user to program the specific mode of operation or check the current programmed status for any of the three integrated timers.

Table 15. Timer Control Block Format

Register Name	Register Offset		
	Tmr. 0	Tmr. 1	Tmr. 2
Mode/Control Word	56H	5EH	66H
Max Count B	54H	5CH	not present
Max Count A	52H	5AH	62H
Count Register	50H	58H	60H

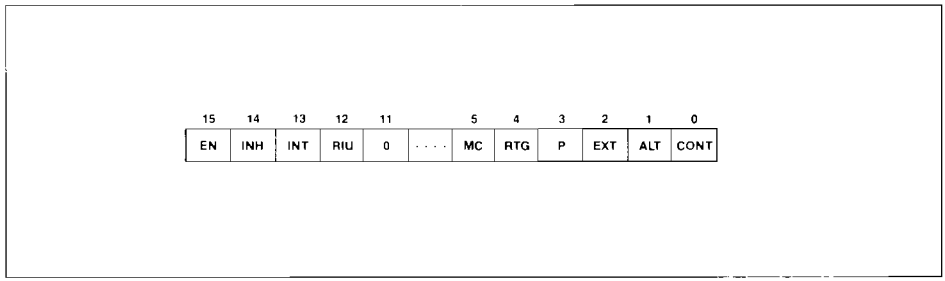


Figure 20. Timer Mode/Control Register

ALT:
The ALT bit determines which of two MAX COUNT registers is used for count comparison. If ALT = 0, register A for that timer is always used, while if ALT = 1, the comparison will alternate between register A and register B when each maximum count is reached. This alternation allows the user to change one MAX COUNT register while the other is being used, and thus provides a method ot generating non-repetitive waveforms. Square waves and pulse outputs of any duty cycle are a subset of available signals obtained by not changing the final count registers. The ALT bit also determines the function of the timer output pin. If ALT is zero, the output pin will go LOW for one clock, the clock after the maximum count is reached. If ALT is one, the output pin will reflect the current MAX COUNT register being used (0/1 for B/A).

CONT:
Setting the CONT bit causes the associated timer to run continuously, while resetting it causes the timer to halt upon maximum count. If CONT = 0 and ALT = 1, the timer will count to the MAX COUNT register A value, reset, count to the register B value, reset, and halt.

EXT:
The external bit selects between internal and external clocking for the timer. The external signal may be asynchronous with respect to the 80186 clock. If this bit is set, the timer will count LOW-to-HIGH transitions on the input pin. If cleared, it will count an internal clock while using the input pin for control. In this mode, the function of the external pin is defined by the RTG bit. The maximum input to output transition latency time may be as much as 6 clocks. However, clock inputs may be pipelined as closely together as every 4 clocks without losing clock pulses.

P:
The prescaler bit is ignored unless internal clocking has been selected (EXT = 0). If the P bit is a zero, the timer will count at one-fourth the internal CPU clock rate. If the P bit is a one, the output of timer 2 will be used as a clock for the timer. Note that the user must initialize and start timer 2 to obtain the prescaled clock.

RTG:
Retrigger bit is only active for internal clocking (EXT = 0). In this case it determines the control function provided by the input pin.

If RTG = 0, the input level gates the internal clock on and off. If the input pin is HIGH, the timer will count; if the input pin is LOW, the timer will hold its value. As indicated previously, the input signal may be asynchronous with respect to the 80186 clock.

When RTG = 1, the input pin detects LOW-to-HIGH transitions. The first such transition starts the timer running, clearing the timer value to zero on the first clock, and then incrementing thereafter. Further transitions on the input pin will again reset the timer to zero, from which it will start counting up again. If CONT = 0, when the timer has reached maximum count, the EN bit will be cleared, inhibiting further timer activity.

EN:
The enable bit provides programmer control over the timer's RUN/HALT status. When set, the timer is enabled to increment subject to the input pin constraints in the internal clock mode (discussed previously). When cleared, the timer will be inhibited from counting. All input pin transitions during the time EN is zero will be ignored. If CONT is zero, the EN bit is automatically cleared upon maximum count.

INH:
The inhibit bit allows for selective updating of the enable (EN) bit. If INH is a one during the write to the mode/control word, then the state of the EN bit will be modified by the write. If INH is a zero during the write, the EN bit will be unaffected by the operation. This bit is not stored; it will always be a 0 on a read.

INT:
When set, the INT bit enables interrupts from the timer, which will be generated on every terminal count. If the timer is configured in dual MAX COUNT register mode, an interrupt will be generated each time the value in MAX COUNT register A is reached, and each time the value in MAX COUNT register B is reached. If this enable bit is cleared after the interrupt request has been generated, but before a pending interrupt is serviced, the interrupt request will still be in force. (The request is latched in the Interrupt Controller.)

MC:
The Maximum Count bit is set whenever the timer reaches its final maximum count value. If the timer is configured in dual MAX COUNT register mode, this bit will be set each time the value in MAX COUNT register A is reached, and each time the value in MAX COUNT register B is reached. This bit is set regardless of the timer's interrupt-enable bit. The MC bit gives the user the ability to monitor timer status through software instead of through interrupts. Programmer intervention is required to clear this bit.

RIU:
The Register In Use bit indicates which MAX COUNT register is currently being used for comparison to the timer count value. A zero value indicates register A. The RIU bit cannot be written, i.e., its value is not affected when the control register is written. It is always cleared when the ALT bit is zero.

Not all mode bits are provided for timer 2. Certain bits are hardwired as indicated below:

ALT = 0, EXT = 0, P = 0, RTG = 0, RIU = 0

Count Registers

Each of the three timers has a 16-bit count register. The current contents of this register may be read or written by the processor at any time. If the register is written into while the timer is counting, the new value will take effect in the current count cycle.

Max Count Registers

Timers 0 and 1 have two MAX COUNT registers, while timer 2 has a single MAX COUNT register. These contain the number of events the timer will count. In timers 0 and 1, the MAX COUNT register used can alternate between the two max count values whenever the current maximum count is reached. The condition which causes a timer to reset is equivalent between the current count value and the max count being used. This means that if the count is changed to be above the max count value, or if the max count value is changed to be below the current value, the timer will not reset to zero, but rather will count to its maximum value, "wrap around" to zero, then count until the max count is reached.

Timers and Reset

Upon RESET, the Timers will perform the following actions:

- All EN (Enable) bits are reset preventing timer counting.
- All SEL (Select) bits are reset to zero. This selects MAX COUNT register A, resulting in the Timer Out pins going HIGH upon RESET.

INTERRUPT CONTROLLER

The 80186 can receive interrupts from a number of sources, both internal and external. The internal interrupt controller serves to merge these requests on a priority basis, for individual service by the CPU. Internal interrupt sources (Timers and DMA channels) can be disabled by their own control registers or by mask bits within the interrupt controller. The 80186 interrupt controller has its own control registers that set the mode of operation for the controller.

The interrupt controller will resolve priority among requests that are pending simultaneously. Nesting is provided so interrupt service routines for lower priority interrupts may themselves be interrupted by higher priority interrupts. A block diagram of the interrupt controller is shown in Figure 21.

The interrupt controller has a special iRMX 86 compatibility mode that allows the use of the 80186 within the iRMX 86 operating system interrupt structure. The controller is set in this mode by setting bit 14 in the peripheral control block relocation register (see iRMX 86 Compatibility Mode section). In this mode, the internal 80186 interrupt controller functions as a "slave" controller to an external "master" controller. Special initialization software must be included to properly set up the 80186 interrupt controller in iRMX 86 mode.

MASTER MODE OPERATION

Interrupt Controller External Interface

For external interrupt sources, five dedicated pins are provided. One of these pins is dedicated to NMI, non-maskable interrupt. This is typically used for power-fail interrupts, etc. The other four pins may function either as four interrupt input lines with internally generated interrupt vectors, as an interrupt line and an interrupt acknowledge line (called the "cascade mode") along with two other input lines with internally generated interrupt vectors, or as two interrupt input lines and two dedicated interrupt acknowledge ouput lines. When the interrupt lines are configured in cascade mode, the 80186 interrupt controller will not generate internal interrupt vectors.

External sources in the cascade mode use externally generated interrupt vectors. When an interrupt is acknowledged, two $\overline{\text{INTA}}$ cycles are initiated and the vector is read into the 80186 on the second cycle. The capability to interface to external 8259A programmable interrupt controllers is thus provided when the inputs are configured in cascade mode.

A

Interrupt Controller Modes of Operation

The basic modes of operation of the interrupt controller in master mode are similar to the 8259A. The interrupt controller responds identically to internal interrupts in all three modes: the difference is only in the interpretation of function of the four external interrupt pins. The interrupt controller is set into one of these three modes by programming the correct bits in the INT0 and INT1 control registers. The modes of interrupt controller operation are as follows:

Fully Nested Mode

When in the fully nested mode four pins are used as direct interrupt requests. The vectors for these four inputs are generated internally. An in-service bit is provided for every interrupt source. If a lower-priority device requests an interrupt while the in-service bit (IS) is set, no interrupt will be generated by the interrupt controller. In addition, if another interrupt request occurs from the same interrupt source while the inservice bit is set, no interrupt will be generated by the interrupt controller. This allows interrupt service routines to operate with interrupts enabled without being themselves interrupted by lower-priority interrupts. Since interrupts are enabled, higher-priority interrupts will be serviced.

When a service routine is completed, the proper IS bit must be reset by writing the proper pattern to the EOI register. This is required to allow subsequent interrupts from this interrupt source and to allow servicing of lower-priority interrupts. An EOI command is issued at the end of the service routine just before the issuance of the return from interrupt instruction. If the fully nested structure has been upheld, the next highest-priority source with its IS bit set is then serviced.

Cascade Mode

The 80186 has four interrupt pins and two of them have dual functions. In the fully nested mode the four pins are used as direct interrupt inputs and the corresponding vectors are generated internally. In the cascade mode, the four pins are configured into interrupt input-dedicated acknowledge signal pairs. The interconnection is shown in Figure 22. INT0 is an interrupt input interfaced to an 8259A, while INT2/$\overline{\text{INTA0}}$ serves as the dedicated interrupt acknowledge signal to that peripheral. The same is true for INT1 and INT3/$\overline{\text{INTA1}}$. Each pair can selectively be placed in the cascade or non-cascade mode by programming the proper value into INT0 and INT1 control registers. The use of the dedicated acknowledge signals eliminates the need for the use of external logic to generate $\overline{\text{INTA}}$ and device select signals.

The primary cascade mode allows the capability to serve up to 128 external interrupt sources through the use of external master and slave 8259As. Three levels of priority are created, requiring priority resolution in the 80186 interrupt controller, the master 8259As, and the slave 8259As. If an external interrupt is serviced, one IS bit is set at each of these levels. When the interrupt service routine is completed, up to three end-of-interrupt commands must be issued by the programmer.

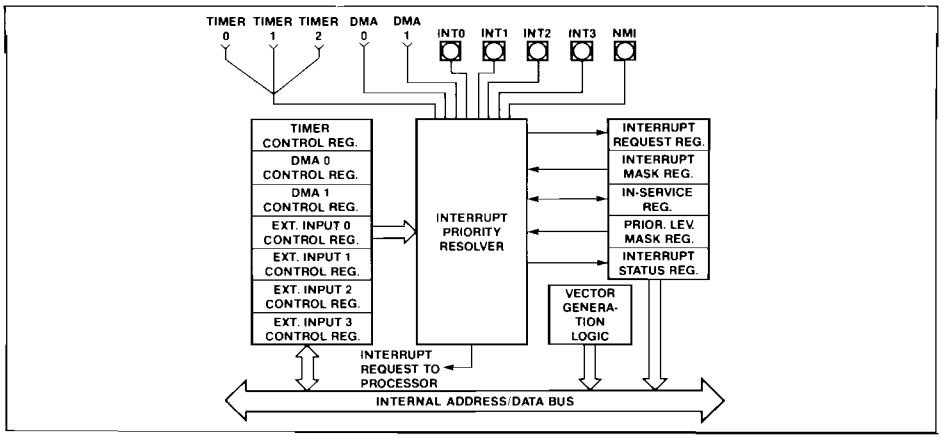


Figure 21. Interrupt Controller Block Diagram

Special Fully Nested Mode
This mode is entered by setting the SFNM bit in INT0 or INT1 control register. It enables complete nestability with external 8259A masters. Normally, an interrupt request from an interrupt source will not be recognized unless the in-service bit for that source is reset. If more than one interrupt source is connected to an external interrupt controller, all of the interrupts will be funneled through the same 80186 interrupt request pin. As a result, if the external interrupt controller receives a higher-priority interrupt, its interrupt will not be recognized by the 80186 controller until the 80186 in-service bit is reset. In special fully nested mode, the 80186 interrupt controller will allow interrupts from an external pin regardless of the state of the in-service bit for an interrupt source in order to allow multiple interrupts from a single pin. An in-service bit will continue to be set, however, to inhibit interrupts from other lower-priority 80186 interrupt sources.

Special procedures should be followed when resetting IS bits at the end of interrupt service routines. Software polling of the external master's IS register is required to determine if there is more than one bit set. If so, the IS bit in the 80186 remains active and the next interrupt service routine is entered.

Operation in a Polled Environment

The controller may be used in a polled mode if interrupts are undesirable. When polling, the processor disables interrupts and then polls the interrupt controller whenever it is convenient. Polling the interrupt controller is accomplished by reading the Poll Word (Figure 31). Bit 15 in the poll word indicates to the processor that an interrupt of high enough priority is requesting service. Bits 0–4 indicate to the processor the type vector of the highest-priority source requesting service. Reading the Poll Word causes the In-Service bit of the highest-priority source to be set.

It is desirable to be able to read the Poll Word information without guaranteeing service of any pending interrupt, i.e., not set the indicated in-service bit. The 80186 provides a Poll Status Word in addition to the conventional Poll Word to allow this to be done. Poll Word information is duplicated in the Poll Status Word, but reading the Poll Status Word does not set the associated in-service bit. These words are located in two adjacent memory locations in the register file.

Master Mode Features

Programmable Priority
The user can program the interrupt sources into any of eight different priority levels. The programming is done by placing a 3-bit priority level (0–7) in the control register of each interrupt source. (A source with a priority level of 4 has higher priority over all priority levels from 5 to 7. Priority registers containing values lower than 4 have greater priority.) All interrupt sources have preprogrammed default priority levels (see Table 4).

If two requests with the same programmed priority level are pending at once, the priority ordering scheme shown in Table 4 is used. If the serviced interrupt routine reenables interrupts, it allows other requests to be serviced.

End-of-Interrupt Command
The end-of-interrupt (EOI) command is used by the programmer to reset the In-Service (IS) bit when an interrupt service routine is completed. The EOI command is issued by writing the proper pattern to the EOI register. There are two types of EOI commands, specific and nonspecific. The nonspecific command does not specify which IS bit is reset. When issued, the interrupt controller automatically resets the IS bit of the highest priority source with an active service routine. A specific EOI command requires that the programmer send the interrupt vector type to the interrupt controller indicating which source's IS bit is to be reset. This command is used when the fully nested structure has been disturbed or the highest priority IS bit that was set does not belong to the service routine in progress.

Trigger Mode
The four external interrupt pins can be programmed in either edge- or level-trigger mode. The control register for each external source has a level-trigger mode (LTM) bit. All interrupt inputs are active HIGH. In the edge sense mode or the level-trigger mode, the interrupt request must remain active (HIGH) until the interrupt request is acknowledged by the 80186 CPU. In the edge-sense mode, if the level remains high after the interrupt is acknowledged, the input is disabled and no further requests will be generated. The input level must go LOW for at least one clock cycle to reenable the input. In the level-trigger mode, no such provision is made: holding the interrupt input HIGH will cause continuous interrupt requests.

Interrupt Vectoring

The 80186 Interrupt Controller will generate interrupt vectors for the integrated DMA channels and the integrated Timers. In addition, the Interrupt Controller will generate interrupt vectors for the external interrupt lines if they are not configured in Cascade or Special Fully Nested Mode. The interrupt vectors generated are fixed and cannot be changed (see Table 4).

Interrupt Controller Registers

The Interrupt Controller register model is shown in Figure 23. It contains 15 registers. All registers can both be read or written unless specified otherwise.

In-Service Register

This register can be read from or written into. The format is shown in Figure 24. It contains the In-Service bit for each of the interrupt sources. The In-Service bit is set to indicate that a source's service routine is in progress. When an In-Service bit is set, the interrupt controller will not generate interrupts to the CPU when it receives interrupt requests from devices with a lower programmed priority level. The TMR bit is the In-Service bit for all three timers; the D0 and D1 bits are the In-Service bits for the two DMA channels; the I0–I3 are the In-Service bits for the external interrupt pins. The IS bit is set when the processor acknowledges an interrupt request either by an interrupt acknowledge or by reading the poll register. The IS bit is reset at the end of the interrupt service routine by an end-of-interrupt command issued by the CPU.

Interrupt Request Register

The internal interrupt sources have interrupt request bits inside the interrupt controller. The format of this register is shown in Figure 24. A read from this register yields the status of these bits. The TMR bit is the logical OR of all timer interrupt requests. D0 and D1 are the interrupt request bits for the DMA channels.

The state of the external interrupt input pins is also indicated. The state of the external interrupt pins is not a stored condition inside the interrupt controller, therefore the external interrupt bits cannot be written. The external interrupt request bits show exactly when an interrupt request is given to the interrupt controller, so if edge-triggered mode is selected, the bit in the register will be HIGH only after an inactive-to-active transition. For internal interrupt sources, the register bits are set when a request arrives and are reset when the processor acknowledges the requests.

Mask Register

This is a 16-bit register that contains a mask bit for each interrupt source. The format for this register is shown in Figure 24. A one in a bit position corresponding to a particular source serves to mask the source from generating interrupts. These mask bits are the exact same bits which are used in the individual control registers; programming a mask bit using the mask register will also change this bit in the individual control registers, and vice versa.

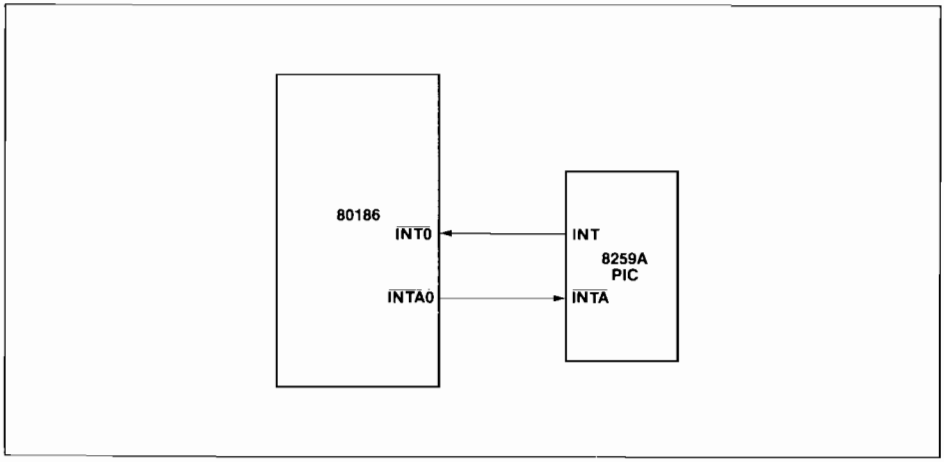


Figure 22. Cascade Mode Interrupt Connection

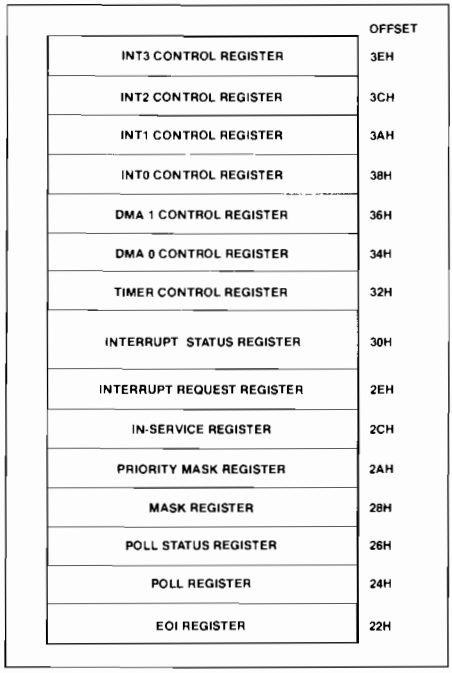


Figure 23. Interrupt Controller Registers (Non-iRMX 86 Mode)

Priority Mask Register

This register is used to mask all interrupts below particular interrupt priority levels. The format of this register is shown in Figure 25. The code in the lower three bits of this register inhibits interrupts of priority lower (a higher priority number) than the code specified. For example, 100 written into this register masks interrupts of level five (101), six (110), and seven (111). The register is reset to seven (111) upon RESET so all interrupts are unmasked.

Interrupt Status Register

This register contains general interrupt controller status information. The format of this register is shown in Figure 26. The bits in the status register have the following functions:

DHLT: DMA Halt Transfer; setting this bit halts all DMA transfers. It is automatically set whenever a non-maskable interrupt occurs, and it is reset when an IRET instruction is executed. The purpose of this bit is to allow prompt service of all non-maskable interrupts. This bit may also be set by the CPU.

IRTx: These three bits represent the individual timer interrupt request bits. These bits are used to differentiate the timer interrupts, since the timer IR bit in the interrupt request register is the "OR" function of all timer interrupt requests. Note that setting any one of these three bits initiates an interrupt request to the interrupt controller.

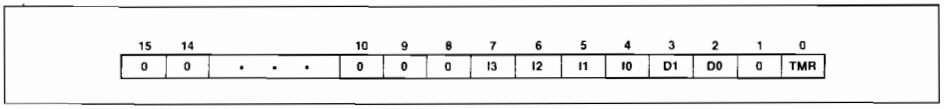


Figure 24. In-Service, Interrupt Request, and Mask Register Formats

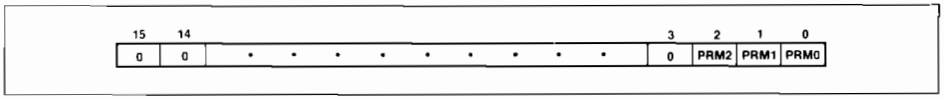


Figure 25. Priority Mask Register Format

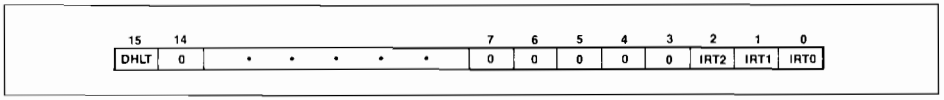


Figure 26. Interrupt Status Register Format

Timer, DMA 0, 1; Control Registers
These registers are the control words for all the internal interrupt sources. The format for these registers is shown in Figure 27. The three bit positions PR0, PR1, and PR2 represent the programmable priority level of the interrupt source. The MSK bit inhibits interrupt requests from the interrupt source. The MSK bits in the individual control registers are the exact same bits as are in the Mask Register; modifying them in the individual control registers will also modify them in the Mask Register, and vice versa.

INT0–INT3 Control Registers
These registers are the control words for the four external input pins. Figure 28 shows the format of the INT0 and INT1 Control registers; Figure 29 shows the format of the INT2 and INT3 Control registers. In cascade mode or special fully nested mode, the control words for INT2 and INT3 are not used.

The bits in the various control registers are encoded as follows:

PRO-2: Priority programming information. Highest Priority = 000, Lowest Priority = 111

LTM: Level-trigger mode bit. 1 = level-triggered; 0 = edge-triggered. Interrupt Input levels are active high. In level-triggered mode, an interrupt is generated whenever the external line is high. In edge-triggered mode, an interrupt will be generated only when this level is preceded by an inactive-to-active transition on the line. In both cases, the level must remain active until the interrupt is acknowledged.

MSK: Mask bit, 1 = mask; 0 = nonmask.

C: Cascade mode bit, 1 = cascade; 0 = direct

SFNM: Special fully nested mode bit, 1 = SFNM

EOI Register
The end of the interrupt register is a command register which can only be written into. The format of this register is shown in Figure 30. It initiates an EOI command when written to by the 80186 CPU.

The bits in the EOI register are encoded as follows:

S_x: Encoded information that specifies an interrupt source vector type as shown in Table 4. For example, to reset the In-Service bit for DMA channel 0, these bits should be set to 01010, since the vector type for DMA channel 0 is 10. Note that to reset the single In-Service bit for any of the three timers, the vector type for timer 0 (8) should be written in this register.

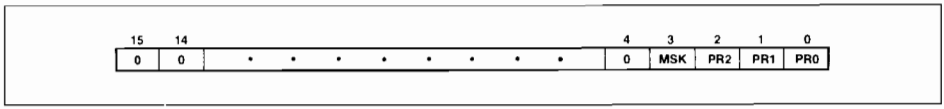


Figure 27. Timer/DMA Control Register Formats

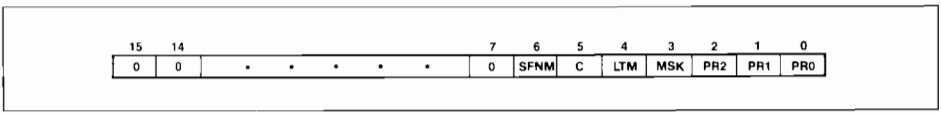


Figure 28. INT0/INT1 Control Register Formats

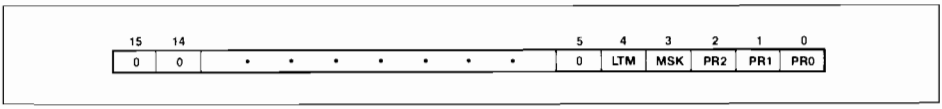


Figure 29. INT2/INT3 Control Register Formats

NSPEC/SPEC: A bit that determines the type of EOI command. Nonspecific = 1, Specific = 0.

Poll and Poll Status Registers

These registers contain polling information. The format of these registers is shown in Figure 31. They can only be read. Reading the Poll register constitutes a software poll. This will set the IS bit of the highest priority pending interrupt. Reading the poll status register will not set the IS bit of the highest priority pending interrupt; only the status of pending interrupts will be provided.

Encoding of the Poll and Poll Status register bits are as follows:

S_x: Encoded information that indicates the vector type of the highest priority interrupting source. Valid only when INTREQ = 1.

INTREQ: This bit determines if an interrupt request is present. Interrupt Request = 1; no Interrupt Request = 0.

iRMX 86 COMPATIBILITY MODE

This mode allows iRMX 86-80186 compatibility. The interrupt model of iRMX 86 requires one master and multiple slave 8259As in cascaded fashion. When iRMX mode is used, the internal 80186 interrupt controller will be used as a slave controller to an external master interrupt controller. The internal 80186 resources will be monitored through the internal interrupt controller, while the external controller functions as the system master interrupt controller.

Upon reset, the 80186 interrupt controller will be in the non-iRMX 86 mode of operation. To set the controller in the iRMX 86 mode, bit 14 of the Relocation Register should be set.

Because of pin limitations caused by the need to interface to an external 8259A master, the internal interrupt controller will no longer accept external inputs. There are however, enough 80186 interrupt controller inputs (internally) to dedicate one to each timer. In this mode, each timer interrupt source has its own mask bit, IS bit, and control word.

The iRMX 86 operating system requires peripherals to be assigned fixed priority levels. This is incompatible with the normal operation of the 80186 interrupt controller. Therefore, the initialization software must program the proper priority levels for each source. The required priority levels for the internal interrupt sources in iRMX mode are shown in Table 16.

Table 16. Internal Source Priority Level

Priority Level	Interrupt Source
0	Timer 0
1	(reserved)
2	DMA 0
3	DMA 1
4	Timer 1
5	Timer 2

These level assignments must remain fixed in the iRMX 86 mode of operation.

iRMX 86 Mode External Interface

The configuration of the 80186 with respect to an external 8259A master is shown in Figure 32. The INT0 input is used as the 80186 CPU interrupt input. INT3 functions as an output to send the 80186 slave-interrupt-request to one of the 8 master-PIC-inputs.

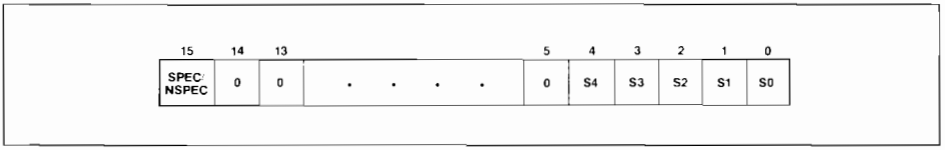


Figure 30. EOI Register Format

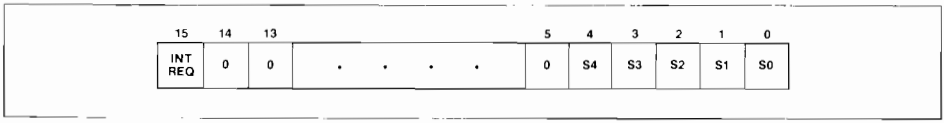


Figure 31. Poll Register Format

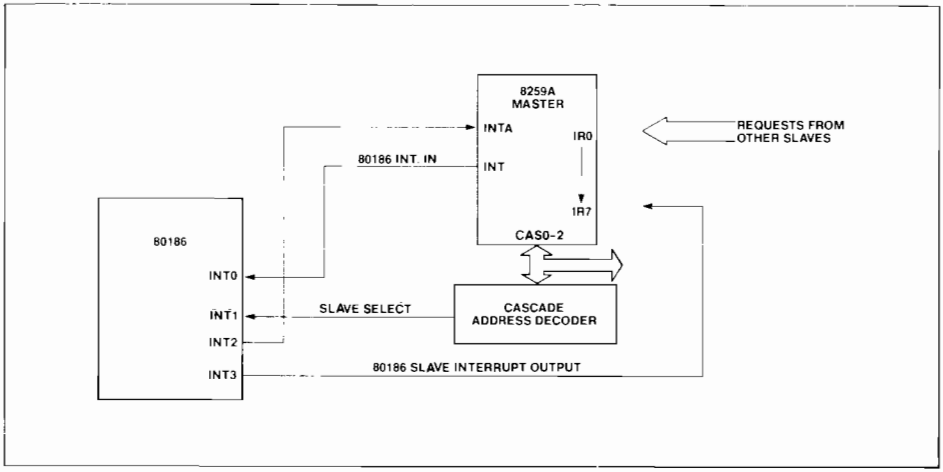


Figure 32. iRMX 86 Interrupt Controller Interconnection

Correct master-slave interface requires decoding of the slave addresses (CAS0–2). Slave 8259As do this internally. Because of pin limitations, the 80186 slave address will have to be decoded externally. $\overline{INT1}$ is used as a slave-select input. Note that the slave vector address is transferred internally, but the READY input must be supplied externally.

$\overline{INT2}$ is used as an acknowledge output, suitable to drive the $\overline{INTA}$ input of an 8259A.

Interrupt Nesting

iRMX 86 mode operation allows nesting of interrupt requests. When an interrupt is acknowledged, the priority logic masks off all priority levels except those with equal or higher priority.

Vector Generation in the iRMX 86 Mode

Vector generation in iRMX mode is exactly like that of an 8259A slave. The interrupt controller generates an 8-bit vector which the CPU multiplies by four and uses as an address into a vector table. The significant five bits of the vector are user-programmable while the lower three bits are generated by the priority logic. These bits represent the encoding of the priority level requesting service. The significant five bits of the vector are programmed by writing to the Interrupt Vector register at offset 20H.

Specific End-of-Interrupt

In iRMX mode the specific EOI command operates to reset an in-service bit of a specific priority. The user supplies a 3-bit priority-level value that points to an in-service bit to be reset. The command is executed by writing the correct value in the Specific EOI register at offset 22H.

Interrupt Controller Registers in the iRMX 86 Mode

All control and command registers are located inside the internal peripheral control block. Figure 33 shows the offsets of these registers.

End-of-Interrupt Register

The end-of-interrupt register is a command register which can only be written. The format of this register is shown in Figure 34. It initiates an EOI command when written by the 80186 CPU.

The bits in the EOI register are encoded as follows:

L_x: Encoded value indicating the priority of the IS bit to be reset.

In-Service Register

This register can be read from or written into. It contains the in-service bit for each of the internal

interrupt sources. The format for this register is shown in Figure 35. Bit positions 2 and 3 correspond to the DMA channels; positions 0, 4, and 5 correspond to the integral timers. The source's IS bit is set when the processor acknowledges its interrupt request.

Interrupt Request Register
This register indicates which internal peripherals have interrupt requests pending. The format of this register is shown in Figure 35. The interrupt request bits are set when a request arrives from an internal source, and are reset when the processor acknowledges the request.

Mask Register
This register contains a mask bit for each interrupt source. The format for this register is shown in Figure 35. If the bit in this register corresponding to a particular interrupt source is set, any interrupts from that source will be masked. These mask bits are exactly the same bits which are used in the individual control registers, i.e., changing the state of a mask bit in this register will also change the state of the mask bit in the individual interrupt control register corresponding to the bit.

Control Registers
These registers are the control words for all the internal interrupt sources. The format of these registers is shown in Figure 36. Each of the timers and both of the DMA channels have their own Control Register.

The bits of the Control Registers are encoded as follows:

pr_x: 3-bit encoded field indicating a priority level for the source; note that each source must be programmed at specified levels.

msk: mask bit for the priority level indicated by pr_x bits.

	OFFSET
LEVEL 5 CONTROL REGISTER (TIMER 2)	3AH
LEVEL 4 CONTROL REGISTER (TIMER 1)	38H
LEVEL 3 CONTROL REGISTER (DMA 1)	36H
LEVEL 2 CONTROL REGISTER (DMA 0)	34H
LEVEL 0 CONTROL REGISTER (TIMER 0)	32H
INTERRUPT STATUS REGISTER	30H
INTERRUPT-REQUEST REGISTER	2EH
IN-SERVICE REGISTER	2CH
PRIORITY-LEVEL MASK REGISTER	2AH
MASK REGISTER	28H
SPECIFIC EOI REGISTER	22H
INTERRUPT VECTOR REGISTER	20H

Figure 33. Interrupt Controller Registers (iRMX 86 Mode)

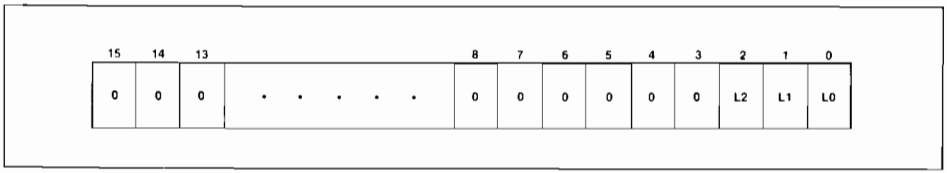


Figure 34. Specific EOI Register Format

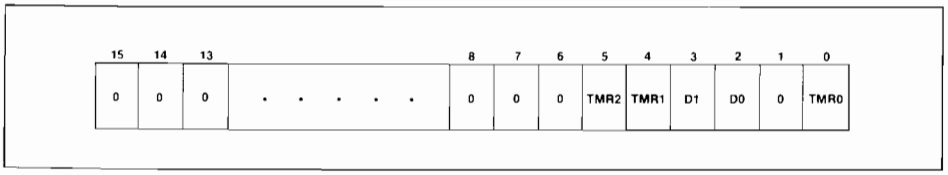


Figure 35. In-Service, Interrupt Request, and Mask Register Format

Interrupt Vector Register
This register provides the upper five bits of the interrupt vector address. The format of this register is shown in Figure 37. The interrupt controller itself provides the lower three bits of the interrupt vector as determined by the priority level of the interrupt request.
The format of the bits in this register is:

t_x: 5-bit field indicating the upper five bits of the vector address.

Priority-Level Mask Register
This register indicates the lowest priority-level interrupt which will be serviced.
The encoding of the bits in this register is:

m_x: 3-bit encoded field indication priority-level value. All levels of lower priority will be masked.

Interrupt Status Register
This register is defined exactly as in Non-iRMX Mode. (See Fig. 26.)

Interrupt Controller and Reset

Upon RESET, the interrupt controller will perform the following actions:

- All SFNM bits reset to 0, implying Fully Nested Mode.
- All PR bits in the various control registers set to 1. This places all sources at lowest priority (level 111).
- All LTM bits reset to 0, resulting in edge-sense mode.
- All Interrupt Service bits reset to 0.
- All Interrupt Request bits reset to 0.
- All MSK (Interrupt Mask) bits set to 1 (mask).
- All C (Cascade) bits reset to 0 (non-cascade).
- All PRM (Priority Mask) bits set to 1, implying no levels masked.
- Initialized to non-iRMX 86 mode.

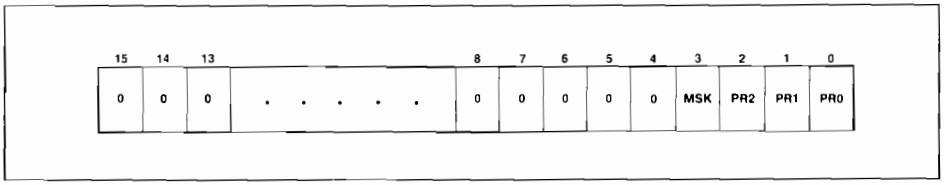


Figure 36. Control Word Format

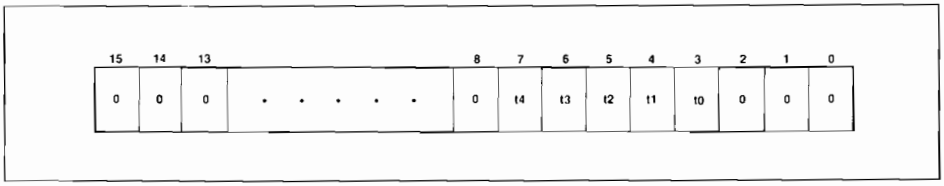


Figure 37. Interrupt Vector Register Format

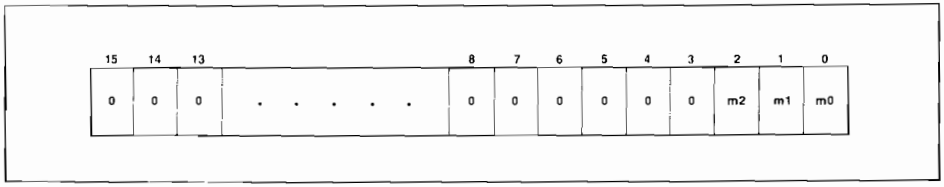


Figure 38. Priority Level Mask Register

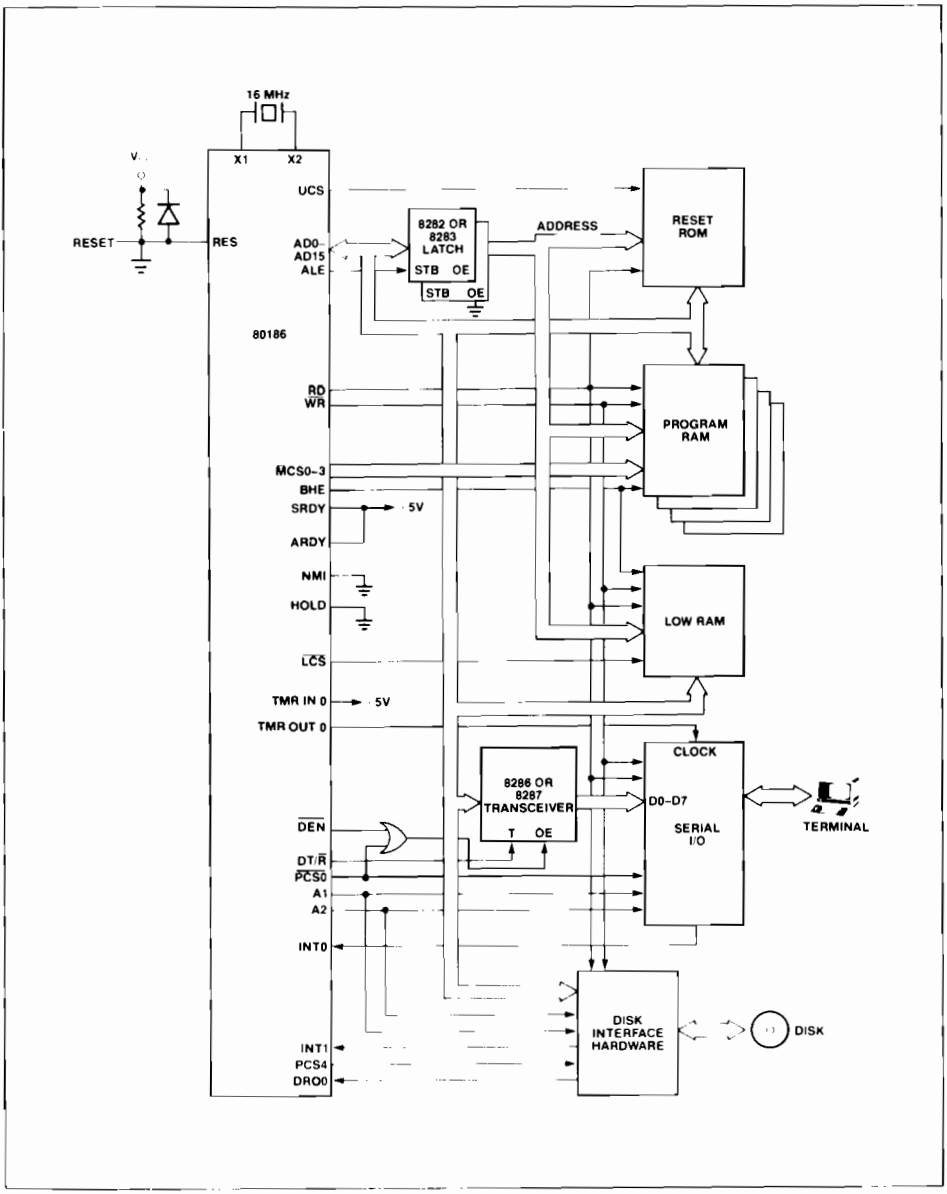


Figure 39. Typical iAPX 186 Computer

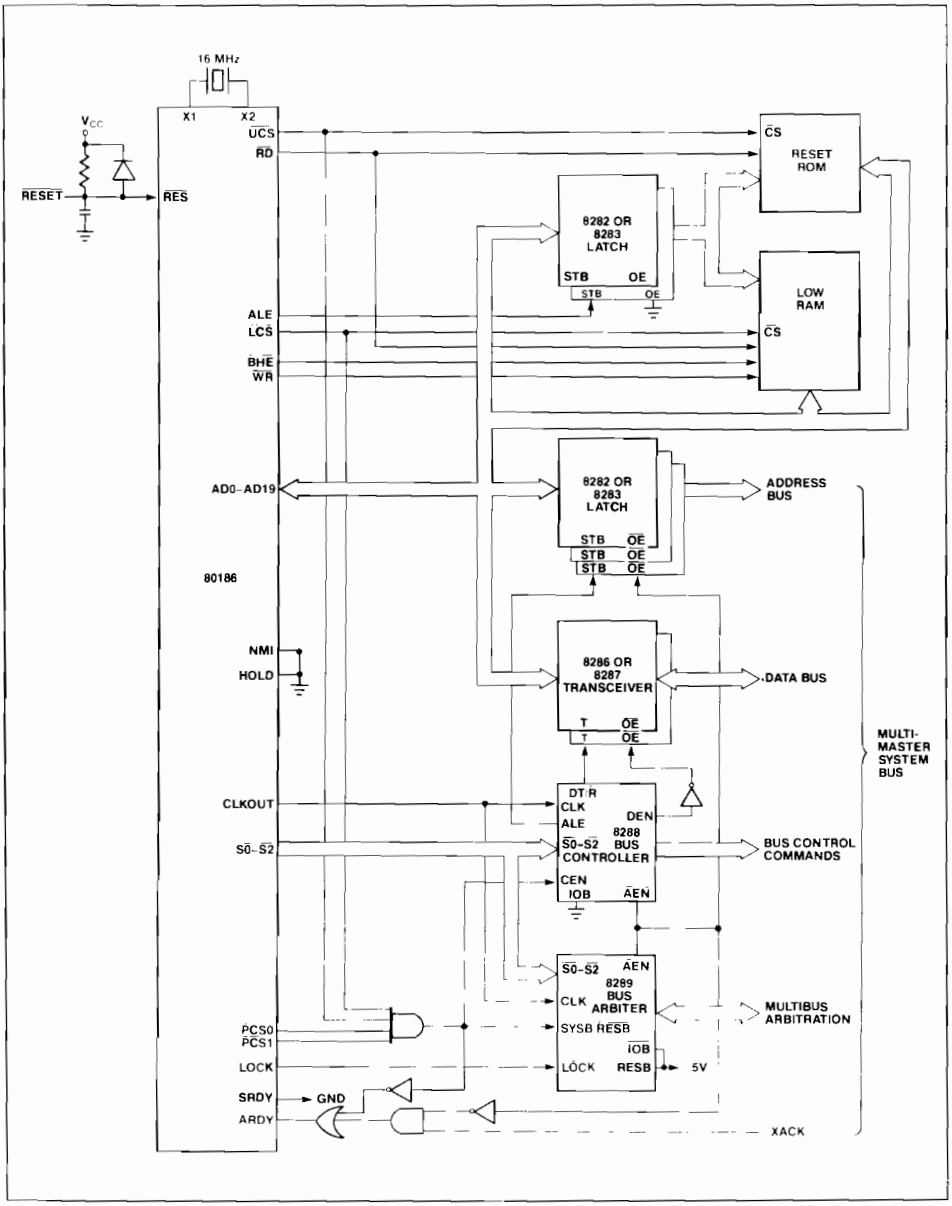


Figure 40. Typical iAPX 186 Multi-Master Bus Interface

PACKAGE

The 80186 is housed in a 68-pin, leadless JEDEC type A hermetic chip carrier. Figure 41 illustrates the package dimensions.

NOTE: The IDT 3M Textool 68-pin JEDEC Socket is required for I²ICE™-186 operation. See Figure 42 for details.

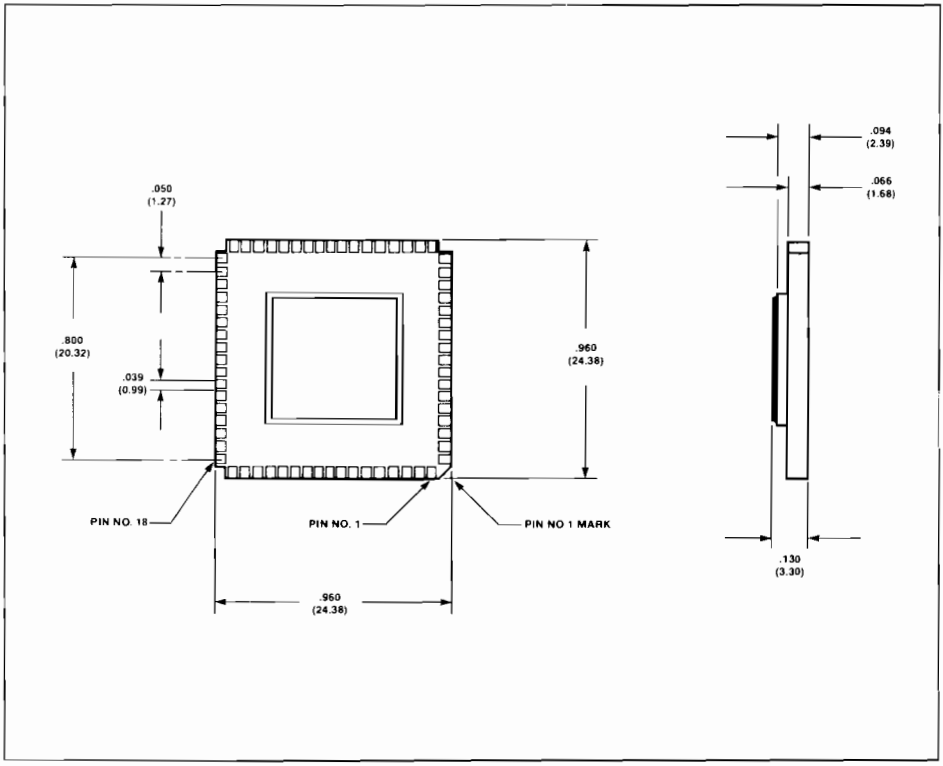


Figure 41. 80186 JEDEC Type A Package

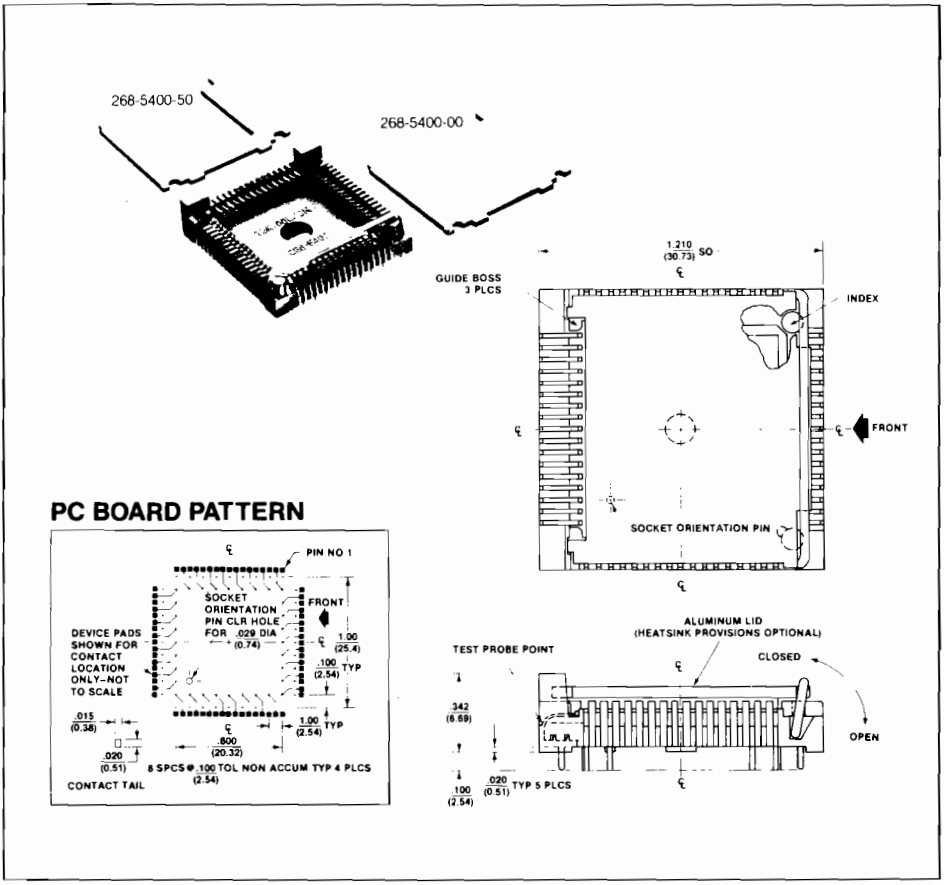


Figure 42. Textool 68 Lead Chip Carrier Socket

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature under Bias ..... 0°C to 70°C
Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin with
Respect to Ground ..... −1.0V to +7V
Power Dissipation ..... 3 Watt

NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (T_A = 0°–70°C, V_{CC} = 5V ±10%)
Applicable to 80186 (8 MHz) and 80186-6 (6 MHz)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
V_{IL}	Input Low Voltage	−0.5	+0.8	Volts	
V_{IH}	Input High Voltage (All except X1 and $\overline{RES}$)	2.0	V_{CC} + 0.5	Volts	
V_{IH1}	Input High Voltage ($\overline{RES}$)	3.0	V_{CC} + 0.5	Volts	
V_{OL}	Output Low Voltage		0.45	Volts	I_a = 2.5 mA for $\overline{S0}$–$\overline{S2}$ I_a = 2.0 mA for all other outputs
V_{OH}	Output High Voltage		2.4	Volts	I_{oa} = −400 μA
I_{CC}	Power Supply Current		550	mA	T_A = 0°C
I_{LI}	Input Leakage Current		±10	μA	$0V < V_{IN} < V_{CC}$
I_{LO}	Output Leakage Current		±10	μA	$0.45V < V_{OUT} < V_{CC}$
V_{CLO}	Clock Output Low		0.6	Volts	I_a = 2.5 mA
V_{CHO}	Clock Output High	4.0		Volts	I_{oa} = −200 μA
V_{CLI}	Clock Input Low Voltage	−0.5	0.6	Volts	
V_{CHI}	Clock Input High Voltage	3.9	V_{CC} + 1.0	Volts	
C_{IN}	Input Capacitance		10	pF	
C_{IO}	I/O Capacitance		20	pF	

PIN TIMINGS

A.C. CHARACTERISTICS (T_A = 0°–70°C, V_{CC} = 5V ± 10%)
80186 Timing Requirements All Timings Measured At 1.5 Volts Unless Otherwise Noted.
Applicable to 80186 (8 MHz) and 80186-6 (6 MHz)

Symbol	Parameter	Min.	Max.	Units	Test Conditions
TDVCL	Data in Setup (A/D)	20		ns	
TCLDX	Data in Hold (A/D)	10		ns	
TARYHCH	Asynchronous Ready (AREADY) active setup time*	20		ns	
TARYLCL	AREADY inactive setup time	35		ns	
TCHARYX	AREADY hold time	15		ns	
TSRYCL	Synchronous Ready (SREADY) transition setup time	35		ns	
TCLSRY	SREADY transition hold time	15		ns	
THVCL	HOLD Setup*	25		ns	
TINVCH	INTR, NMI, $\overline{TEST}$, TIMERIN, Setup*	25		ns	
TINVCL	DRQ0, DRQ1, Setup*	25		ns	

*To guarantee recognition at next clock.

A

A.C. CHARACTERISTICS (Continued)

80186 Master Interface Timing Responses

		80186 (8 MHz)		80186-6 (6 MHz)			
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**	**Test Conditions**
TCLAV	Address Valid Delay	10	44	10	63	ns	C_L = 20-200 pF all outputs
TCLAX	Address Hold	10		10		ns	
TCLAZ	Address Float Delay	TCLAX	35	TCLAX	44	ns	
TCHCZ	Command Lines Float Delay		45		56	ns	
TCHCV	Command Lines Valid Delay (after float)		55		TCHCL	ns	
TLHLL	ALE Width	TCLCL-35		TCLCL-35		ns	
TCHLH	ALE Active Delay		35		44	ns	
TCHLL	ALE Inactive Delay		35		44	ns	
TLLAX	Address Hold to ALE Inactive	TCHCL-25		TCHCL-30		ns	
TCLDV	Data Valid Delay	10	44	10	55	ns	
TCLDOX	Data Hold Time	10		10		ns	
TWHDX	Data Hold after WR	TCLCL-40		TCLCL-50		ns	
TCVCTV	Control Active Delay1	10	70	10	87	ns	
TCHCTV	Control Active Delay2	10	55	10	TCHCL	ns	
TCVCTX	Control Inactive Delay	10	55	10	TCLCH	ns	
TCVDEX	$\overline{DEN}$ Inactive Delay (Non-Write Cycle)		70		87	ns	
TAZRL	Address Float to $\overline{RD}$ Active	0		0		ns	
TCLRL	$\overline{RD}$ Active Delay	10	70	10	87	ns	
TCLRH	$\overline{RD}$ Inactive Delay	10	55	10	TCLCH	ns	
TRHAV	$\overline{RD}$ Inactive to Address Active	TCLCL-40		TCLCL-50		ns	
TCLHAV	HLDA Valid Delay	10	50	10	67	ns	
TRLRH	$\overline{RD}$ Width	2TCLCL-50		2TCLCL-50		ns	
TWLWH	$\overline{WR}$ Width	2TCLCL-40		2TCLCL-40		ns	
TAVAL	Address Valid to ALE Low	TCLCH-25		TCLCH-45		ns	
TCHSV	Status Active Delay	10	55	10	TCHCL	ns	
TCLSH	Status Inactive Delay	10	55	10	TCLCH	ns	
TCLTMV	Timer Output Delay		60		75	ns	100 pf max
TCLRO	Reset Delay		60		75	ns	
TCHQSV	Queue Status Delay		35		44	ns	

80186 Chip-Select Timing Responses

Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**	**Test Conditions**
TCLCSV	Chip-Select Active Delay		66		80	ns	
TCXCSX	Chip-Select Hold from Command Inactive	35		35		ns	
TCHCSX	Chip-Select Inactive Delay	10	35	10	47	ns	

A.C. CHARACTERISTICS (Continued)

80186 CLKIN Requirements

		80186 (8 MHz)		80186-6 (6 MHz)			
Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**	**Test Conditions**
TCKIN	CLKIN Period	62.5	250	83	250	ns	
TCKHL	CLKIN Fall Time		10		10	ns	3.5 to 1.0 volts
TCKLH	CLKIN Rise Time		10		10	ns	1.0 to 3.5 volts
TCLCK	CLKIN Low Time	25		33		ns	1.5 volts
TCHCK	CLKIN High Time	25		33		ns	1.5 volts

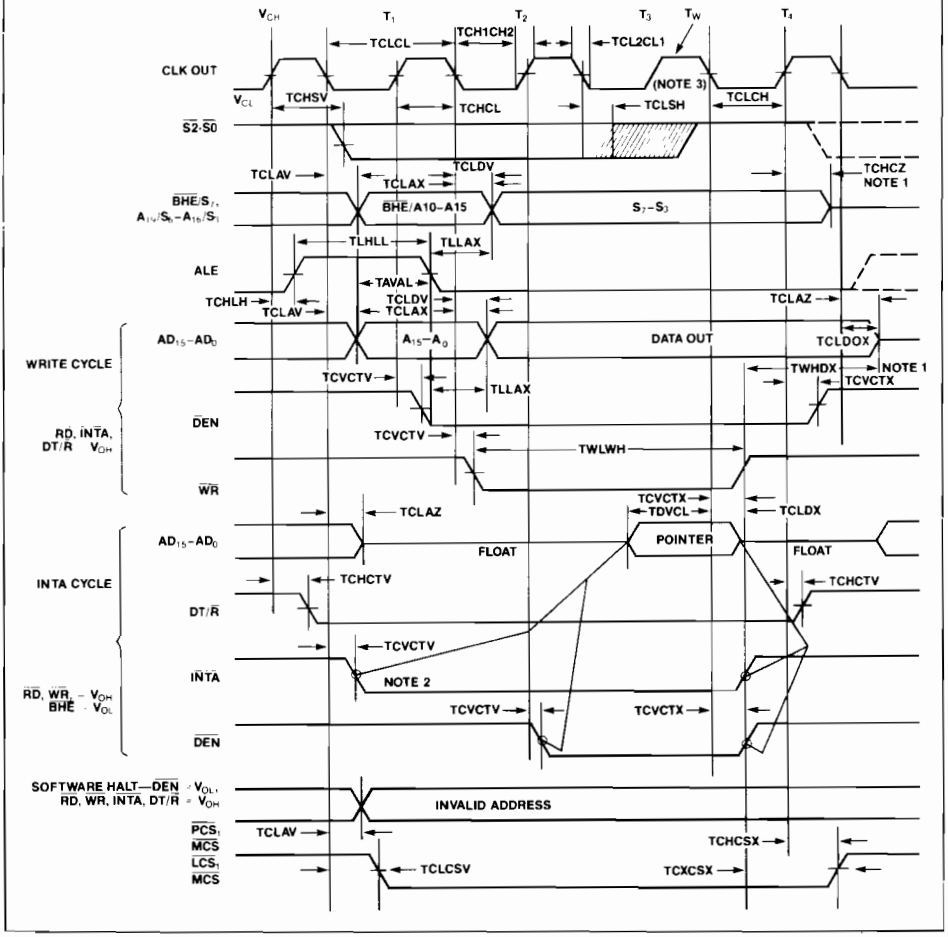
80186 CLKOUT Timing (200 pF load)

Symbol	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Units**	**Test Conditions**
TCICO	CLKIN to CLKOUT Skew		50		62.5	ns	
TCLCL	CLKOUT Period	125	500	167	500	ns	
TCLCH	CLKOUT Low Time	½ TCLCL-7.5		½ TCLCL-7.5		ns	1.5 volts
TCHCL	CLKOUT High Time	½ TCLCL-7.5		½ TCLCL-7.5		ns	1.5 volts
TCH1CH2	CLKOUT Rise Time		15		15	ns	1.0 to 3.5 volts
TCL2CL1	CLKOUT Fall Time		15		15	ns	3.5 to 1. volts

A

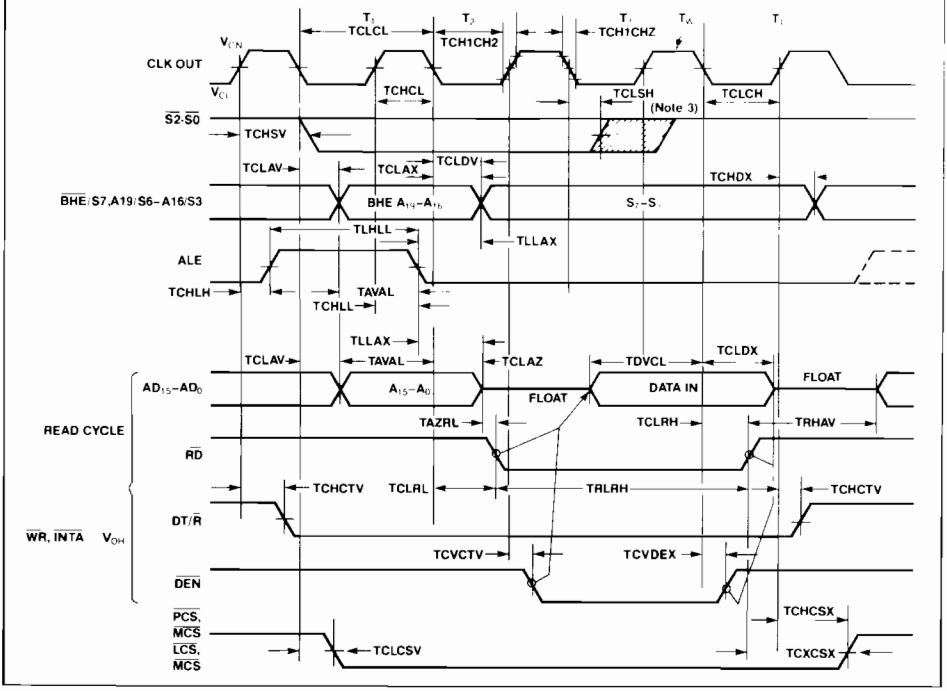
WAVEFORMS

MAJOR CYCLE TIMING



WAVEFORMS (Continued)

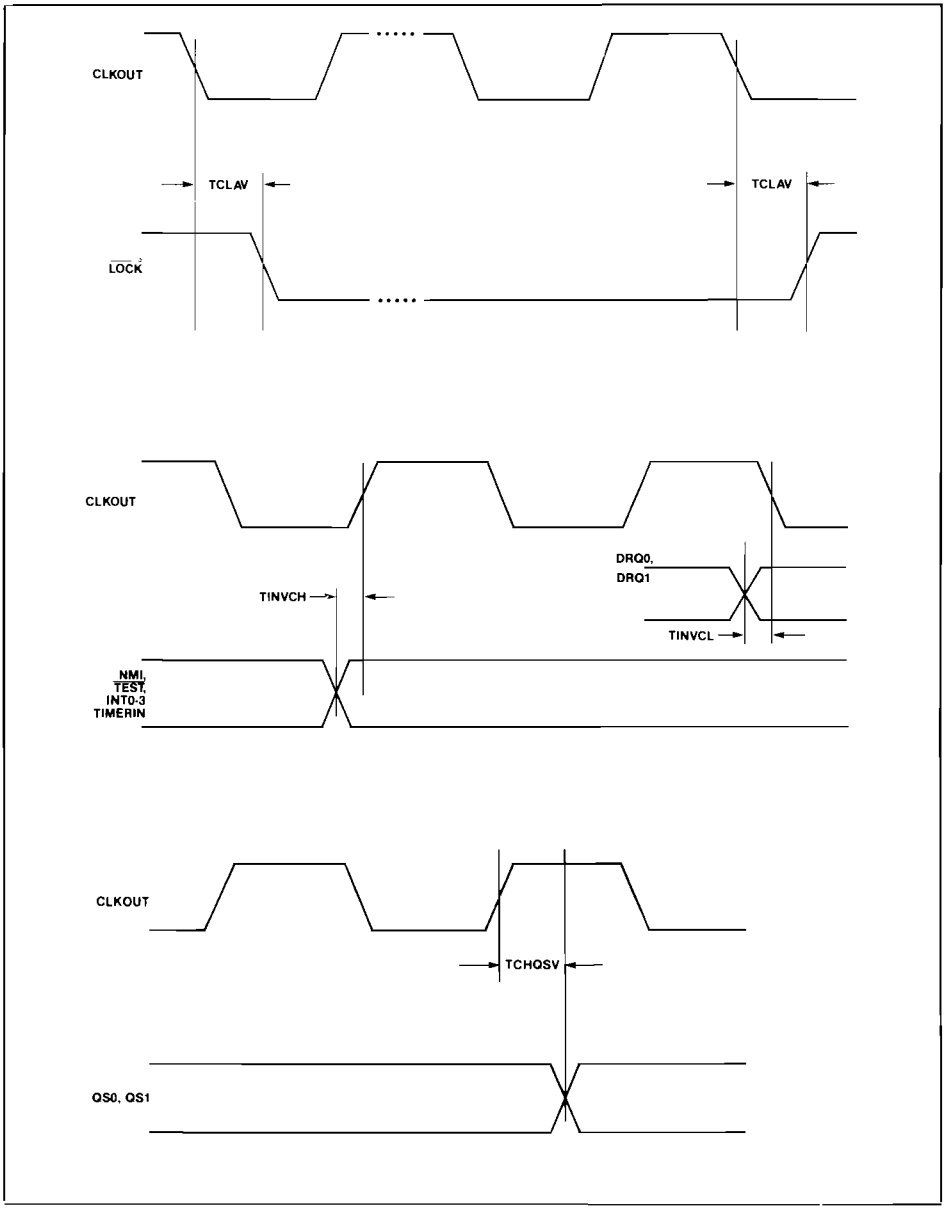
MAJOR CYCLE TIMING (Continued)



NOTES:
1. Following a Write cycle, the Local Bus is floated by the 80186 only when the 80186 enters a "Hold Acknowledge" state.
2. INTA occurs one clock later in RMX-mode.
3. Status inactive just prior to T_4

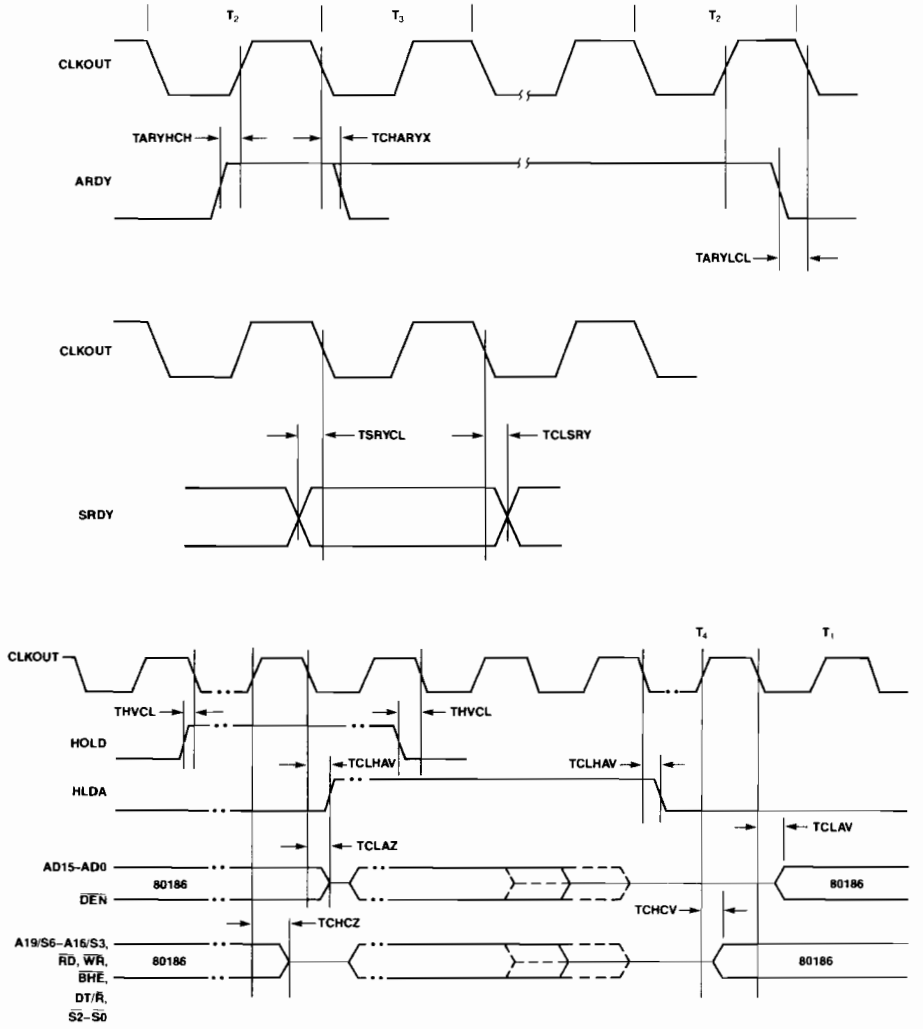
A

WAVEFORMS (Continued)



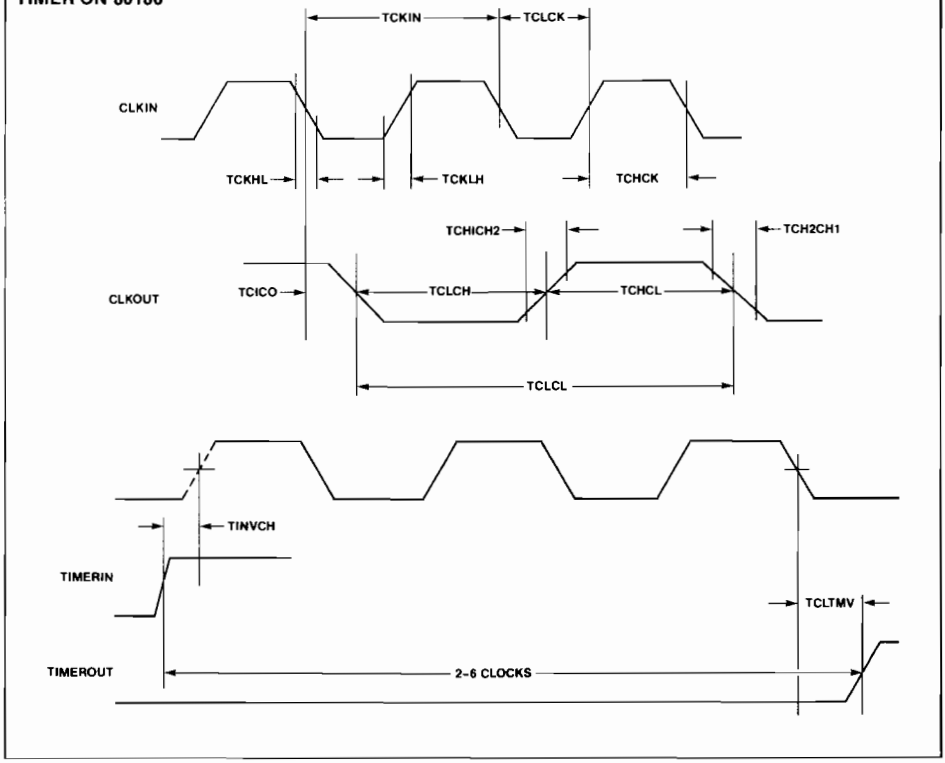
WAVEFORMS (Continued)

HOLD-HLDA TIMING



WAVEFORMS (Continued)

TIMER ON 80186



80186 INSTRUCTION TIMINGS

The following instruction timings represent the minimum execution time in clock cycles for each instruction. The timings given are based on the following assumptions:

- The opcode, along with any data or displacement required for execution of a particular instruction, has been prefetched and resides in the queue at the time it is needed.
- No wait states or bus HOLDS occur.
- All word-data is located on even-address boundaries.

All jumps and calls include the time required to fetch the opcode of the next instruction at the destination address.

All instructions which involve memory reference can require one (and in some cases, two) additional clocks above the minimum timings shown. This is due to the asynchronous nature of the handshake between the BIU and the Execution unit.

INSTRUCTION SET SUMMARY

FUNCTION	FORMAT	Clock Cycles	Comments
DATA TRANSFER			
MOV = Move:			
Register to Register Memory	1 0 0 0 1 0 0 w | mod reg r/m	2/12	
Register memory to register	1 0 0 0 1 0 1 w | mod reg r/m	2/9	
Immediate to register memory	1 1 0 0 0 1 1 w | mod 0 0 0 r/m | data | data if w = 1	12–13	8/16-bit
Immediate to register	1 0 1 1 w reg | data | data if w = 1	3–4	8/16-bit
Memory to accumulator	1 0 1 0 0 0 0 w | addr-low | addr-high	9	
Accumulator to memory	1 0 1 0 0 0 1 w | addr-low | addr-high	8	
Register memory to segment register	1 0 0 0 1 1 1 0 | mod 0 reg r/m	2/9	
Segment register to register/memory	1 0 0 0 1 1 0 0 | mod 0 reg r/m	2/11	
PUSH = Push:			
Memory	1 1 1 1 1 1 1 1 | mod 1 1 0 r/m	16	
Register	0 1 0 1 0 reg	10	
Segment register	0 0 0 reg 1 1 0	9	
Immediate	**0 1 1 0 1 0 s 0 | data | data if s = 0**	**10**	
PUSHA = Push All	**0 1 1 0 0 0 0 0**	**36**	
POP = Pop:			
Memory	1 0 0 0 1 1 1 1 | mod 0 0 0 r/m	20	
Register	0 1 0 1 1 reg	10	
Segment register	0 0 0 reg 1 1 1 (reg ≠ 01)	8	
POPA = Pop All	**0 1 1 0 0 0 0 1**	**51**	
XCHG = Exchange:			
Register/memory with register	1 0 0 0 0 1 1 w | mod reg r/m	4/17	
Register with accumulator	1 0 0 1 0 reg	3	
IN = Input from:			
Fixed port	1 1 1 0 0 1 0 w | port	10	
Variable port	1 1 1 0 1 1 0 w	8	
OUT = Output to:			
Fixed port	1 1 1 0 0 1 1 w | port	9	
Variable port	1 1 1 0 1 1 1 w	7	
XLAT - Translate byte to AL	1 1 0 1 0 1 1 1	11	
LEA - Load EA to register	1 0 0 0 1 1 0 1 | mod reg r/m	6	
LDS - Load pointer to DS	1 1 0 0 0 1 0 1 | mod reg r/m (mod ≠ 11)	18	
LES - Load pointer to ES	1 1 0 0 0 1 0 0 | mod reg r/m (mod ≠ 11)	18	
LAHF - Load AH with flags	1 0 0 1 1 1 1 1	2	
SAHF - Store AH into flags	1 0 0 1 1 1 1 0	3	
PUSHF - Push flags	1 0 0 1 1 1 0 0	9	
POPF - Pop flags	1 0 0 1 1 1 0 1	8	
SEGMENT = Segment Override:			
CS	0 0 1 0 1 1 1 0	2	
SS	0 0 1 1 0 1 1 0	2	
DS	0 0 1 1 1 1 1 0	2	
ES	0 0 1 0 0 1 1 0	2	

Shaded areas indicate instructions not available in iAPX 86, 88 microsystems.

INSTRUCTION SET SUMMARY (Continued)

FUNCTION	FORMAT	Clock Cycles	Comments
ARITHMETIC			
ADD = Add:			
Reg/memory with register to either	0 0 0 0 0 0 d w | mod reg r/m	3/10	
Immediate to register/memory	1 0 0 0 0 0 s w | mod 0 0 0 r/m | data | data if s w = 01	4/16	
Immediate to accumulator	0 0 0 0 0 1 0 w | data | data if w = 1	3/4	8/16-bit
ADC = Add with carry:			
Reg/memory with register to either	0 0 0 1 0 0 d w | mod reg r/m	3/10	
Immediate to register/memory	1 0 0 0 0 0 s w | mod 0 1 0 r/m | data | data if s w = 01	4/16	
Immediate to accumulator	0 0 0 1 0 1 0 w | data | data if w = 1	3/4	8/16-bit
INC = Increment:			
Register/memory	1 1 1 1 1 1 1 w | mod 0 0 0 r/m	3/15	
Register	0 1 0 0 0 reg	3	
SUB = Subtract:			
Reg/memory and register to either	0 0 1 0 1 0 d w | mod reg r/m	3/10	
Immediate from register/memory	1 0 0 0 0 0 s w | mod 1 0 1 r/m | data | data if s w = 01	4/16	
Immediate from accumulator	0 0 1 0 1 1 0 w | data | data if w = 1	3/4	8/16-bit
SBB = Subtract with borrow:			
Reg/memory and register to either	0 0 0 1 1 0 d w | mod reg r/m	3/10	
Immediate from register/memory	1 0 0 0 0 0 s w | mod 0 1 1 r/m | data | data if s w = 01	4/16	
Immediate from accumulator	0 0 0 1 1 1 0 w | data | data if w = 1	3/4	8/16-bit
DEC = Decrement:			
Register/memory	1 1 1 1 1 1 1 w | mod 0 0 1 r/m	3/15	
Register	0 1 0 0 1 reg	3	
CMP = Compare:			
Register/memory with register	0 0 1 1 1 0 d w | mod reg r/m	3/10	
Register with register/memory	0 0 1 1 1 0 0 w | mod reg r/m	3/10	
Immediate with register/memory	1 0 0 0 0 0 s w | mod 1 1 1 r/m | data | data if s w = 01	3/10	
Immediate with accumulator	0 0 1 1 1 1 0 w | data | data if w = 1	3/4	8/16-bit
NEG = Change sign	1 1 1 1 0 1 1 w | mod 0 1 1 r/m	3	
AAA = ASCII adjust for add	0 0 1 1 0 1 1 1	8	
DAA = Decimal adjust for add	0 0 1 0 0 1 1 1	4	
AAS = ASCII adjust for subtract	0 0 1 1 1 1 1 1	7	
DAS = Decimal adjust for subtract	0 0 1 0 1 1 1 1	4	
MUL = Multiply (unsigned):	1 1 1 1 0 1 1 w | mod 1 0 0 r/m		
Register-Byte		26–28	
Register-Word		35–37	
Memory-Byte		32–34	
Memory-Word		41–43	
IMUL = Integer multiply (signed):	1 1 1 1 0 1 1 w | mod 1 0 1 r/m		
Register-Byte		25–28	
Register-Word		34–37	
Memory-Byte		31–34	
Memory-Word		40–43	
IMUL = Integer immediate multiply (signed)	0 1 1 0 1 0 s 1 | mod reg r/m | data | data if s = 0	22–25/29–32	
DIV = Divide (unsigned):	1 1 1 1 0 1 1 w | mod 1 1 0 r/m		
Register-Byte		29	
Register-Word		38	
Memory-Byte		35	
Memory-Word		44	

Shaded areas indicate instructions not available in iAPX 86, 88 microsystems.

INSTRUCTION SET SUMMARY (Continued)

FUNCTION	FORMAT	Clock Cycles	Comments
ARITHMETIC (Continued):			
IDIV = Integer divide (signed)	1 1 1 1 0 1 1 w | mod 1 1 1 r/m		
Register-Byte		44–52	
Register-Word		53–61	
Memory-Byte		50–58	
Memory-Word		59–67	
AAM = ASCII adjust for multiply	1 1 0 1 0 1 0 0 | 0 0 0 0 1 0 1 0	19	
AAD = ASCII adjust for divide	1 1 0 1 0 1 0 1 | 0 0 0 0 1 0 1 0	15	
CBW = Convert byte to word	1 0 0 1 1 0 0 0	2	
CWD = Convert word to double word	1 0 0 1 1 0 0 1	4	
LOGIC			
Shift/Rotate Instructions:			
Register/Memory by 1	1 1 0 1 0 0 0 w | mod TTT r/m	2/15	
Register/Memory by CL	1 1 0 1 0 0 1 w | mod TTT r/m	5+n/17+n	
Register/Memory by Count	1 1 0 0 0 0 0 w | mod TTT r/m | count	5+n/17+n	

TTT	Instruction
0 0 0	ROL
0 0 1	ROR
0 1 0	RCL
0 1 1	RCR
1 0 0	SHL/SAL
1 0 1	SHR
1 1 1	SAR

AND = And:					
Reg/memory and register to either	0 0 1 0 0 0 d w	mod reg r/m		3/10	
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 1 0 0 r/m	data	data if w = 1	4/16
Immediate to accumulator	0 0 1 0 0 1 0 w	data	data if w = 1		3/4	8/16-bit
TEST = And function to flags, no result:					
Register/memory and register	1 0 0 0 0 1 0 w	mod reg r/m			3/10	
Immediate data and register/memory	1 1 1 1 0 1 1 w	mod 0 0 0 r/m	data	data if w = 1	4/10
Immediate data and accumulator	1 0 1 0 1 0 0 w	data	data if w = 1		3/4	8/16-bit
OR = Or:					
Reg/memory and register to either	0 0 0 0 1 0 d w	mod reg r/m			3/10	
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 0 0 1 r/m	data	data if w = 1	4/16
Immediate to accumulator	0 0 0 0 1 1 0 w	data	data if w = 1		3/4	8/16-bit
XOR = Exclusive or:					
Reg/memory and register to either	0 0 1 1 0 0 d w	mod reg r/m			3/10	
Immediate to register/memory	1 0 0 0 0 0 0 w	mod 1 1 0 r/m	data	data if w = 1	4/16
Immediate to accumulator	0 0 1 1 0 1 0 w	data	data if w = 1		3/4	8/16-bit
NOT = Invert register/memory	1 1 1 1 0 1 1 w	mod 0 1 0 r/m			3	
STRING MANIPULATION:					
MOVS = Move byte/word	1 0 1 0 0 1 0 w				14	
CMPS = Compare byte/word	1 0 1 0 0 1 1 w				22	
SCAS = Scan byte/word	1 0 1 0 1 1 1 w				15	
LODS = Load byte/wd to AL/AX	1 0 1 0 1 1 0 w				12	
STOS = Stor byte/wd from AL/A	1 0 1 0 1 0 1 w				10	
INS = Input byte/wd from DX port	0 1 1 0 1 1 0 w				14	
OUTS = Output byte/wd to DX port	0 1 1 0 1 1 1 w				14	

Shaded areas indicate instructions not available in iAPX 86, 88 microsystems.

INSTRUCTION SET SUMMARY (Continued)

FUNCTION	FORMAT	Clock Cycles	Comments
STRING MANIPULATION (Continued):			
Repeated by count in CX			
MOVS Move string	1 1 1 * 0 0 1 0 | 1 0 1 0 0 1 0 w	8+8n	
CMPS Compare string	1 1 1 1 0 0 1 z | 1 0 1 0 0 1 1 w	5+22n	
SCAS Scan string	1 1 1 1 0 0 1 z | 1 0 1 0 1 1 1 w	5+15n	
LODS Load string	1 1 1 1 0 0 1 0 | 1 0 1 0 1 1 0 w	6+11n	
STOS Store string	1 1 1 1 0 0 1 0 | 1 0 1 0 1 0 1 w	6+9n	
INS – Input string	1 1 1 1 0 0 1 0 | 0 1 1 0 1 1 0 w	8+8n	
OUTS – Output string	1 1 1 1 0 0 1 0 | 0 1 1 0 1 1 1 w	8+8n	
CONTROL TRANSFER			
CALL = Call:			
Direct within segment	1 1 1 0 1 0 0 0 | disp-low | disp-high	14	
Register memory indirect within segment	1 1 1 1 1 1 1 1 | mod 0 1 0 r/m	13/19	
Direct intersegment	1 0 0 1 1 0 1 0 | segment offset | segment selector	23	
Indirect intersegment	1 1 1 1 1 1 1 1 | mod 0 1 1 r/m (mod ≠ 11)	38	
JMP = Unconditional jump:			
Short long	1 1 1 0 1 0 1 1 | disp-low	13	
Direct within segment	1 1 1 0 1 0 0 1 | disp-low | disp-high	13	
Register memory indirect within segment	1 1 1 1 1 1 1 1 | mod 1 0 0 r/m	11/17	
Direct intersegment	1 1 1 0 1 0 1 0 | segment offset | segment selector	13	
Indirect intersegment	1 1 1 1 1 1 1 1 | mod 1 0 1 r/m (mod ≠ 11)	26	
RET = Return from CALL:			
Within segment	1 1 0 0 0 0 1 1	16	
Within seg adding immed to SP	1 1 0 0 0 0 1 0 | data-low | data-high	18	
Intersegment	1 1 0 0 1 0 1 1	22	
Intersegment adding immediate to SP	1 1 0 0 1 0 1 0 | data-low | data-high	25	

Shaded areas indicate instructions not available in iAPX 86, 88 microsystems.

INSTRUCTION SET SUMMARY (Continued)

FUNCTION	FORMAT	Clock Cycles	Comments
CONTRDL TRANSFER (Continued):			
JE/JZ – Jump on equal zero	0 1 1 1 0 1 0 0 | disp	4/13	JMP not taken/JMP taken
JL/JNGE – Jump on less not greater or equal	0 1 1 1 1 1 0 0 | disp	4/13	
JLE/JNG – Jump on less or equal not greater	0 1 1 1 1 1 1 0 | disp	4/13	
JB/JNAE – Jump on below not above or equal	0 1 1 1 0 0 1 0 | disp	4/13	
JBE/JNA – Jump on below or equal not above	0 1 1 1 0 1 1 0 | disp	4/13	
JP/JPE – Jump on parity parity even	0 1 1 1 1 0 1 0 | disp	4/13	
JO – Jump on overflow	0 1 1 1 0 0 0 0 | disp	4/13	
JS – Jump on sign	0 1 1 1 1 0 0 0 | disp	4/13	
JNE/JNZ – Jump on not equal not zero	0 1 1 1 0 1 0 1 | disp	4/13	
JNL/JGE – Jump on not less greater or equal	0 1 1 1 1 1 0 1 | disp	4/13	
JNLE/JG – Jump on not less or equal greater	0 1 1 1 1 1 1 1 | disp	4/13	
JNB/JAE – Jump on not below above or equal	0 1 1 1 0 0 1 1 | disp	4/13	
JNBE/JA – Jump on not below or equal above	0 1 1 1 0 1 1 1 | disp	4/13	
JNP/JPO – Jump on not par par odd	0 1 1 1 1 0 1 1 | disp	4/13	
JNO – Jump on not overflow	0 1 1 1 0 0 0 1 | disp	4/13	
JNS – Jump on not sign	0 1 1 1 1 0 0 1 | disp	4/13	
JCXZ – Jump on CX zero	1 1 1 0 0 0 1 1 | disp	5/15	
LOOP – Loop CX times	1 1 1 0 0 0 1 0 | disp	6/16	LOOP not taken/LOOP taken
LOOPZ/LOOPE – Loop while zero equal	1 1 1 0 0 0 0 1 | disp	6/16	
LODPNZ/LOOPNE – Loop while not zero equal	1 1 1 0 0 0 0 0 | disp	6/16	
ENTER = Enter Procedure	1 1 0 0 1 0 0 0 | data-low | data-high | L		
L = 0		15	
L = 1		25	
L > 1		22+16(n−1)	
LEAVE = Leave Procedure	1 1 0 0 1 0 0 1	8	
INT = Interrupt:			
Type specified	1 1 0 0 1 1 0 1 | type	47	
Type 3	1 1 0 0 1 1 0 0	45	if INT. taken/ if INT. not taken
INTO = Interrupt on overflow	1 1 0 0 1 1 1 0	48/4	
IRET = Interrupt return	1 1 0 0 1 1 1 1	28	
BOUND = Detect value out of range	0 1 1 0 0 0 1 0 | mod reg r/m	33–35	

Shaded areas indicate instructions not available in iAPX 86, 88 microsystems.

INSTRUCTION SET SUMMARY (Continued)

FUNCTION	FORMAT	Clock Cycles	Comments
PROCESSOR CONTROL			
CLC = Clear carry	1 1 1 1 1 0 0 0	2	
CMC = Complement carry	1 1 1 1 0 1 0 1	2	
STC = Set carry	1 1 1 1 1 0 0 1	2	
CLD = Clear direction	1 1 1 1 1 1 0 0	2	
STD = Set direction	1 1 1 1 1 1 0 1	2	
CLI = Clear interrupt	1 1 1 1 1 0 1 0	2	
STI = Set interrupt	1 1 1 1 1 0 1 1	2	
HLT = Halt	1 1 1 1 0 1 0 0	2	
WAIT = Wait	1 0 0 1 1 0 1 1	6	if $\overline{\text{test}}$ = 0
LOCK = Bus lock prefix	1 1 1 1 0 0 0 0	2	
ESC = Processor Extension Escape	1 0 0 1 1 T T T | mod LLL r/m (TTT LLL are opcode to processor extension)	6	

Shaded areas indicate instructions not available in iAPX 86, 88 microsystems.

FOOTNOTES

The effective Address (EA) of the memory operand is computed according to the mod and r/m fields:

if mod = 11 then r/m is treated as a REG field
if mod = 00 then DISP = 0*, disp-low and disp-high are absent
if mod = 01 then DISP = disp-low sign-extended to 16-bits, disp-high is absent
if mod = 10 then DISP = disp-high: disp-low

if r/m = 000 then EA = (BX) + (SI) + DISP
if r/m = 001 then EA = (BX) + (DI) + DISP
if r/m = 010 then EA = (BP) + (SI) + DISP
if r/m = 011 then EA = (BP) + (DI) + DISP
if r/m = 100 then EA = (SI) + DISP
if r/m = 101 then EA = (DI) + DISP
if r/m = 110 then EA = (BP) + DISP*
if r/m = 111 then EA = (BX) + DISP

DISP follows 2nd byte of instruction (before data if required)

*except if mod = 00 and r/m = 110 then EA = disp-high: disp-low.

NOTE:
EA CALCULATION TIME IS 4 CLOCK CYCLES FOR ALL MODES, AND IS INCLUDED IN THE EXECUTION TIMES GIVEN WHENEVER APPROPRIATE.

SEGMENT OVERRIDE PREFIX

0	0	1	reg	1	1	0

reg is assigned according to the following:

reg	Segment Register
00	ES
01	CS
10	SS
11	DS

REG is assigned according to the following table:

16-Bit (w = 1)	8-Bit (w = 0)
000 AX	000 AL
001 CX	001 CL
010 DX	010 DL
011 BX	011 BL
100 SP	100 AH
101 BP	101 CH
110 SI	110 DH
111 DI	111 BH

The physical addresses of all operands addressed by the BP register are computed using the SS segment register. The physical addresses of the destination operands of the string primitive operations (those addressed by the DI register) are computed using the ES segment, which may not be overridden.

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Microprocessors

8259A/8259A-2/8259A-8
PROGRAMMABLE INTERRUPT CONTROLLER

- iAPX 86, iAPX 88 Compatible
- MCS-80®, MCS-85® Compatible
- Eight-Level Priority Controller
- Expandable to 64 Levels
- Programmable Interrupt Modes
- Individual Request Mask Capability
- Single +5V Supply (No Clocks)
- 28-Pin Dual-In-Line Package
- Available in EXPRESS
  - Standard Temperature Range
  - Extended Temperature Range

The Intel® 8259A Programmable Interrupt Controller handles up to eight vectored priority interrupts for the CPU. It is cascadable for up to 64 vectored priority interrupts without additional circuitry. It is packaged in a 28-pin DIP, uses NMOS technology and requires a single +5V supply. Circuitry is static, requiring no clock input.

The 8259A is designed to minimize the software and real time overhead in handling multi-level priority interrupts. It has several modes, permitting optimization for a variety of system requirements.

The 8259A is fully upward compatible with the Intel® 8259. Software originally written for the 8259 will operate the 8259A in all 8259 equivalent modes (MCS-80/85, Non-Buffered, Edge Triggered).

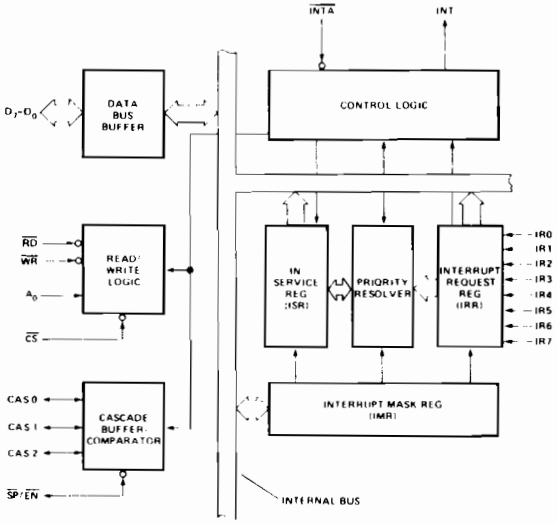


Figure 1. Block Diagram

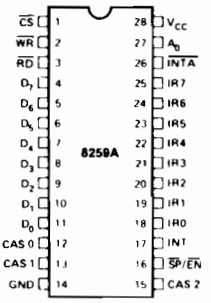


Figure 2. Pin Configuration

Table 1. Pin Description

Symbol	Pin No.	Type	Name and Function
V_{CC}	28	I	**Supply:** +5V Supply.
GND	14	I	**Ground.**
$\overline{CS}$	1	I	**Chip Select:** A low on this pin enables $\overline{RD}$ and $\overline{WR}$ communication between the CPU and the 8259A. INTA functions are independent of CS.
$\overline{WR}$	2	O	**Write:** A low on this pin when CS is low enables the 8259A to accept command words from the CPU.
$\overline{RD}$	3	I	**Read:** A low on this pin when CS is low enables the 8259A to release status onto the data bus for the CPU.
D_7–D_0	4–11	I/O	**Bidirectional Data Bus:** Control, status and interrupt-vector information is transferred via this bus.
CAS_0–CAS_2	12, 13, 15	I/O	**Cascade Lines:** The CAS lines form a private 8259A bus to control a multiple 8259A structure. These pins are outputs for a master 8259A and inputs for a slave 8259A.
$\overline{SP}/\overline{EN}$	16	I/O	**Slave Program/Enable Buffer:** This is a dual function pin. When in the Buffered Mode it can be used as an output to control buffer transceivers (EN). When not in the buffered mode it is used as an input to designate a master (SP = 1) or slave (SP = 0).
INT	17	O	**Interrupt:** This pin goes high whenever a valid interrupt request is asserted. It is used to interrupt the CPU, thus it is connected to the CPU's interrupt pin.
IR_0–IR_7	18–25	I	**Interrupt Requests:** Asynchronous inputs. An interrupt request is executed by raising an IR input (low to high), and holding it high until it is acknowledged (Edge Triggered Mode), or just by a high level on an IR input (Level Triggered Mode).
$\overline{INTA}$	26	I	**Interrupt Acknowledge:** This pin is used to enable 8259A interrupt-vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.
A_0	27	I	**A0 Address Line:** This pin acts in conjunction with the $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ pins. It is used by the 8259A to decipher various Command Words the CPU writes and status the CPU wishes to read. It is typically connected to the CPU A0 address line (A1 for iAPX 86, 88).

FUNCTIONAL DESCRIPTION

Interrupts in Microcomputer Systems

Microcomputer system design requires that I/O devices such as keyboards, displays, sensors and other components receive servicing in an efficient manner so that large amounts of the total system tasks can be assumed by the microcomputer with little or no effect on throughput.

The most common method of servicing such devices is the *Polled* approach. This is where the processor must test each device in sequence and in effect "ask" each one if it needs servicing. It is easy to see that a large portion of the main program is looping through this continuous polling cycle and that such a method would have a serious, detrimental effect on system throughput, thus limiting the tasks that could be assumed by the microcomputer and reducing the cost effectiveness of using such devices.

A more desirable method would be one that would allow the microprocessor to be executing its main program and only stop to service peripheral devices when it is told to do so by the device itself. In effect, the method would provide an external asynchronous input that would inform the processor that it should complete whatever instruction that is currently being executed and fetch a new routine that will service the requesting device. Once this servicing is complete, however, the processor would resume exactly where it left off.

This method is called *Interrupt*. It is easy to see that system throughput would drastically increase, and thus more tasks could be assumed by the microcomputer to further enhance its cost effectiveness.

The Programmable Interrupt Controller (PIC) functions as an overall manager in an Interrupt-Driven system environment. It accepts requests from the peripheral equipment, determines which of the incoming requests is of the highest importance (priority), ascertains whether the incoming request has a higher priority value than the level currently being serviced, and issues an interrupt to the CPU based on this determination.

Each peripheral device or structure usually has a special program or "routine" that is associated with its specific functional or operational requirements; this is referred to as a "service routine". The PIC, after issuing an Interrupt to the CPU, must somehow input information into the CPU that can "point" the Program Counter to the service routine associated with the requesting device. This "pointer" is an address in a vectoring table and will often be referred to, in this document, as vectoring data.

The 8259A

The 8259A is a device specifically designed for use in real time, interrupt driven microcomputer systems. It manages eight levels or requests and has built-in features for expandability to other 8259A's (up to 64 levels). It is programmed by the system's software as an I/O peripheral. A selection of priority modes is available to the programmer so that the manner in which the requests are processed by the 8259A can be configured to match his system requirements. The priority modes can be changed or reconfigured dynamically at any time during the main program. This means that the complete interrupt structure can be defined as required, based on the total system environment.

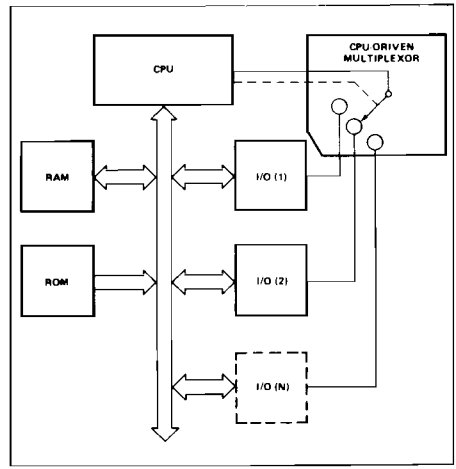


Figure 3a. Polled Method

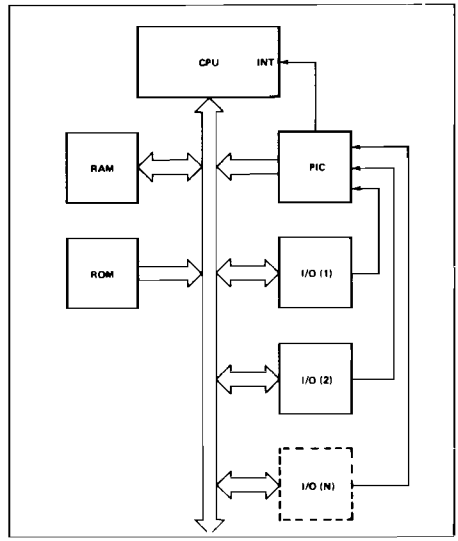


Figure 3b. Interrupt Method

INTERRUPT REQUEST REGISTER (IRR) AND IN-SERVICE REGISTER (ISR)

The interrupts at the IR input lines are handled by two registers in cascade, the Interrupt Request Register (IRR) and the In-Service Register (ISR). The IRR is used to store all the interrupt levels which are requesting service; and the ISR is used to store all the interrupt levels which are being serviced.

PRIORITY RESOLVER

This logic block determines the priorities of the bits set in the IRR. The highest priority is selected and strobed into the corresponding bit of the ISR during $\overline{INTA}$ pulse.

INTERRUPT MASK REGISTER (IMR)

The IMR stores the bits which mask the interrupt lines to be masked. The IMR operates on the IRR. Masking of a higher priority input will not affect the interrupt request lines of lower priority.

INT (INTERRUPT)

This output goes directly to the CPU interrupt input. The V_{OH} level on this line is designed to be fully compatible with the 8080A, 8085A and 8086 input levels.

$\overline{INTA}$ (INTERRUPT ACKNOWLEDGE)

$\overline{INTA}$ pulses will cause the 8259A to release vectoring information onto the data bus. The format of this data depends on the system mode (μPM) of the 8259A.

DATA BUS BUFFER

This 3-state, bidirectional 8-bit buffer is used to interface the 8259A to the system Data Bus. Control words and status information are transferred through the Data Bus Buffer.

READ/WRITE CONTROL LOGIC

The function of this block is to accept OUTput commands from the CPU. It contains the Initialization Command Word (ICW) registers and Operation Command Word (OCW) registers which store the various control formats for device operation. This function block also allows the status of the 8259A to be transferred onto the Data Bus.

$\overline{CS}$ (CHIP SELECT)

A LOW on this input enables the 8259A. No reading or writing of the chip will occur unless the device is selected.

$\overline{WR}$ (WRITE)

A LOW on this input enables the CPU to write control words (ICWs and OCWs) to the 8259A.

$\overline{RD}$ (READ)

A LOW on this input enables the 8259A to send the status of the Interrupt Request Register (IRR), In Service Register (ISR), the Interrupt Mask Register (IMR), or the Interrupt level onto the Data Bus.

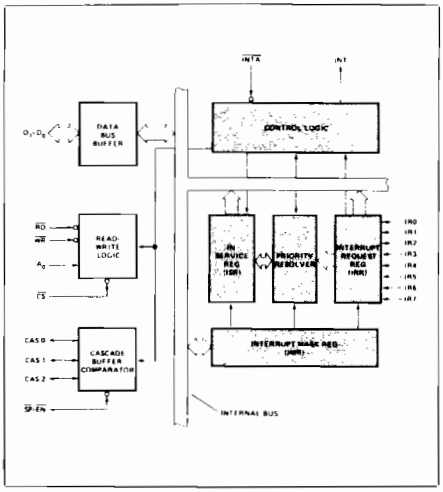


Figure 4a. 8259A Block Diagram

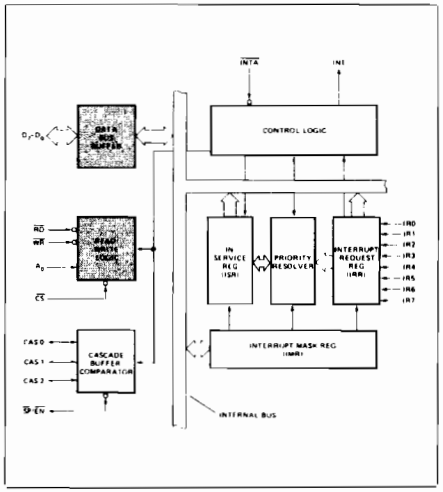


Figure 4b. 8259A Block Diagram

A_0

This input signal is used in conjunction with $\overline{WR}$ and $\overline{RD}$ signals to write commands into the various command registers, as well as reading the various status registers of the chip. This line can be tied directly to one of the address lines.

THE CASCADE BUFFER/COMPARATOR

This function block stores and compares the IDs of all 8259A's used in the system. The associated three I/O pins (CAS0-2) are outputs when the 8259A is used as a master and are inputs when the 8259A is used as a slave. As a master, the 8259A sends the ID of the interrupting slave device onto the CAS0-2 lines. The slave thus selected will send its preprogrammed subroutine address onto the Data Bus during the next one or two consecutive $\overline{INTA}$ pulses. (See section "Cascading the 8259A".)

INTERRUPT SEQUENCE

The powerful features of the 8259A in a microcomputer system are its programmability and the interrupt routine addressing capability. The latter allows direct or indirect jumping to the specific interrupt routine requested without any polling of the interrupting devices. The normal sequence of events during an interrupt depends on the type of CPU being used.

The events occur as follows in an MCS-80/85 system:

1. One or more of the INTERRUPT REQUEST lines (IR7-0) are raised high, setting the corresponding IRR bit(s).
2. The 8259A evaluates these requests, and sends an INT to the CPU, if appropriate.
3. The CPU acknowledges the INT and responds with an $\overline{INTA}$ pulse.
4. Upon receiving an $\overline{INTA}$ from the CPU group, the highest priority ISR bit is set, and the corresponding IRR bit is reset. The 8259A will also release a CALL instruction code (11001101) onto the 8-bit Data Bus through its D7-0 pins.
5. This CALL instruction will initiate two more $\overline{INTA}$ pulses to be sent to the 8259A from the CPU group.
6. These two $\overline{INTA}$ pulses allow the 8259A to release its preprogrammed subroutine address onto the Data Bus. The lower 8-bit address is released at the first $\overline{INTA}$ pulse and and the higher 8-bit address is released at the second $\overline{INTA}$ pulse.
7. This completes the 3-byte CALL instruction released by the 8259A. In the AEOI mode the ISR bit is reset at the end of the third $\overline{INTA}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt sequence.

The events occurring in an iAPX 86 system are the same until step 4.

4. Upon receiving an $\overline{INTA}$ from the CPU group, the highest priority ISR bit is set and the corresponding IRR bit is reset. The 8259A does not drive the Data Bus during this cycle.
5. The iAPX 86/10 will initiate a second $\overline{INTA}$ pulse. During this pulse, the 8259A releases an 8-bit pointer onto the Data Bus where it is read by the CPU.
6. This completes the interrupt cycle. In the AEOI mode the ISR bit is reset at the end of the second $\overline{INTA}$ pulse. Otherwise, the ISR bit remains set until an appropriate EOI command is issued at the end of the interrupt subroutine.

If no interrupt request is present at step 4 of either sequence (i.e., the request was too short in duration) the 8259A will issue an interrupt level 7. Both the vectoring bytes and the CAS lines will look like an interrupt level 7 was requested.

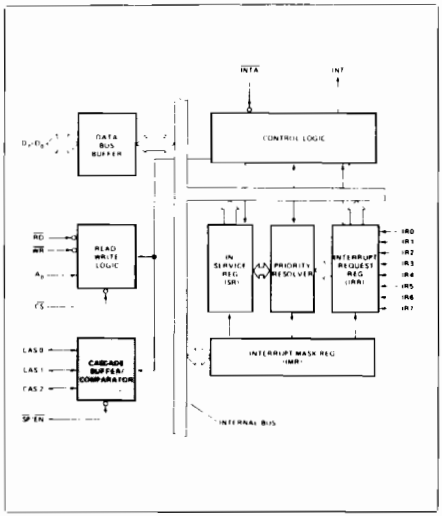


Figure 4c. 8259A Block Diagram

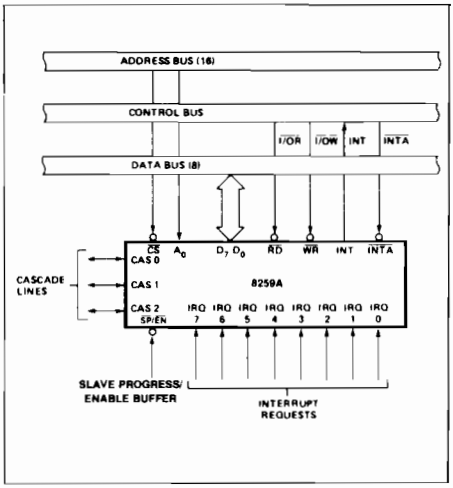


Figure 5. 8259A Interface to Standard System Bus

A

INTERRUPT SEQUENCE OUTPUTS

MCS-80®, MCS-85®

This sequence is timed by three $\overline{INTA}$ pulses. During the first $\overline{INTA}$ pulse the CALL opcode is enabled onto the data bus.

Content of First Interrupt Vector Byte

	D7	D6	D5	D4	D3	D2	D1	D0
CALL CODE	1	1	0	0	1	1	0	1

During the second $\overline{INTA}$ pulse the lower address of the appropriate service routine is enabled onto the data bus. When Interval = 4 bits A_5-A_7 are programmed, while A_0-A_4 are automatically inserted by the 8259A. When Interval = 8 only A_6 and A_7 are programmed, while A_0-A_5 are automatically inserted.

Content of Second Interrupt Vector Byte

IR	Interval = 4							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	A5	1	1	1	0	0
6	A7	A6	A5	1	1	0	0	0
5	A7	A6	A5	1	0	1	0	0
4	A7	A6	A5	1	0	0	0	0
3	A7	A6	A5	0	1	1	0	0
2	A7	A6	A5	0	1	0	0	0
1	A7	A6	A5	0	0	1	0	0
0	A7	A6	A5	0	0	0	0	0

IR	Interval = 8							
	D7	D6	D5	D4	D3	D2	D1	D0
7	A7	A6	1	1	1	0	0	0
6	A7	A6	1	1	0	0	0	0
5	A7	A6	1	0	1	0	0	0
4	A7	A6	1	0	0	0	0	0
3	A7	A6	0	1	1	0	0	0
2	A7	A6	0	1	0	0	0	0
1	A7	A6	0	0	1	0	0	0
0	A7	A6	0	0	0	0	0	0

During the third INTA pulse the higher address of the appropriate service routine, which was programmed as byte 2 of the initialization sequence (A_8-A_{15}), is enabled onto the bus.

Content of Third Interrupt Vector Byte

D7	D6	D5	D4	D3	D2	D1	D0
A15	A14	A13	A12	A11	A10	A9	A8

iAPX 86, iAPX 88

iAPX 86 mode is similar to MCS-80 mode except that only two Interrupt Acknowledge cycles are issued by the processor and no CALL opcode is sent to the processor. The first interrupt acknowledge cycle is similar to that of MCS-80, 85 systems in that the 8259A uses it to internally freeze the state of the interrupts for priority resolution and as a master it issues the interrupt code on the cascade lines at the end of the INTA pulse. On this first cycle it does not issue any data to the processor and leaves its data bus buffers disabled. On the second interrupt acknowledge cycle in iAPX 86 mode the master (or slave if so programmed) will send a byte of data to the processor with the acknowledged interrupt code composed as follows (note the state of the ADI mode control is ignored and A_5-A_{11} are unused in iAPX 86 mode):

Content of Interrupt Vector Byte for iAPX 86 System Mode

	D7	D6	D5	D4	D3	D2	D1	D0
IR7	T7	T6	T5	T4	T3	1	1	1
IR6	T7	T6	T5	T4	T3	1	1	0
IR5	T7	T6	T5	T4	T3	1	0	1
IR4	T7	T6	T5	T4	T3	1	0	0
IR3	T7	T6	T5	T4	T3	0	1	1
IR2	T7	T6	T5	T4	T3	0	1	0
IR1	T7	T6	T5	T4	T3	0	0	1
IR0	T7	T6	T5	T4	T3	0	0	0

PROGRAMMING THE 8259A

The 8259A accepts two types of command words generated by the CPU:

1. *Initialization Command Words (ICWs):* Before normal operation can begin, each 8259A in the system must be brought to a starting point — by a sequence of 2 to 4 bytes timed by $\overline{WR}$ pulses.
2. *Operation Command Words (OCWs):* These are the command words which command the 8259A to operate in various interrupt modes. These modes are:
   a. Fully nested mode
   b. Rotating priority mode
   c. Special mask mode
   d. Polled mode

The OCWs can be written into the 8259A anytime after initialization.

INITIALIZATION COMMAND WORDS (ICWS)

GENERAL

Whenever a command is issued with A0 = 0 and D4 = 1, this is interpreted as Initialization Command Word 1 (ICW1). ICW1 starts the initialization sequence during which the following automatically occur.

a. The edge sense circuit is reset, which means that following initialization, an interrupt request (IR) input must make a low-to-high transition to generate an interrupt.
b. The Interrupt Mask Register is cleared.
c. IR7 input is assigned priority 7.
d. The slave mode address is set to 7.
e. Special Mask Mode is cleared and Status Read is set to IRR.
f. If IC4 = 0, then all functions selected in ICW4 are set to zero. (Non-Buffered mode*, no Auto-EOI, MCS-80, 85 system).

***Note:** Master/Slave in ICW4 is only used in the buffered mode

INITIALIZATION COMMAND WORDS 1 AND 2 (ICW1, ICW2)

A_5-A_{15}: *Page starting address of service routines.* In an MCS 80/85 system, the 8 request levels will generate CALLs to 8 locations equally spaced in memory. These can be programmed to be spaced at intervals of 4 or 8 memory locations, thus the 8 routines will occupy a page of 32 or 64 bytes, respectively.

The address format is 2 bytes long (A_0-A_{15}). When the routine interval is 4, A_0-A_4 are automatically inserted by the 8259A, while A_5-A_{15} are programmed externally. When the routine interval is 8, A_0-A_5 are automatically inserted by the 8259A, while A_6-A_{15} are programmed externally.

The 8-byte interval will maintain compatibility with current software, while the 4-byte interval is best for a compact jump table.

In an iAPX 86 system A_{15}–A_{11} are inserted in the five most significant bits of the vectoring byte and the 8259A sets the three least significant bits according to the interrupt level. A_{10}–A_5 are ignored and ADI (Address interval) has no effect.

LTIM: If LTIM = 1, then the 8259A will operate in the level interrupt mode. Edge detect logic on the interrupt inputs will be disabled.

ADI: CALL address interval. ADI = 1 then interval = 4; ADI = 0 then interval = 8.

SNGL: Single. Means that this is the only 8259A in the system. If SNGL = 1 no ICW3 will be issued.

IC4: If this bit is set — ICW4 has to be read. If ICW4 is not needed, set IC4 = 0.

INITIALIZATION COMMAND WORD 3 (ICW3)

This word is read only when there is more than one 8259A in the system and cascading is used, in which case SNGL = 0. It will load the 8-bit slave register. The functions of this register are:

a. In the master mode (either when SP = 1, or in buffered mode when M/S = 1 in ICW4) a "1" is set for each slave in the system. The master then will release byte 1 of the call sequence (for MCS-80/85 system) and will enable the corresponding slave to release bytes 2 and 3 (for iAPX 86 only byte 2) through the cascade lines.

b. In the slave mode (either when $\overline{SP}$ = 0, or if BUF = 1 and M/S = 0 in ICW4) bits 2-0 identify the slave. The slave compares its cascade input with these bits and, if they are equal, bytes 2 and 3 of the call sequence (or just byte 2 for iAPX 86 are released by it on the Data Bus.

INITIALIZATION COMMAND WORD 4 (ICW4)

SFNM: If SFNM = 1 the special fully nested mode is programmed.

BUF: If BUF = 1 the buffered mode is programmed. In buffered mode $\overline{SP}/\overline{EN}$ becomes an enable output and the master/slave determination is by M/S.

M/S: If buffered mode is selected: M/S = 1 means the 8259A is programmed to be a master, M/S = 0 means the 8259A is programmed to be a slave. If BUF = 0, M/S has no function.

AEOI: If AEOI = 1 the automatic end of interrupt mode is programmed.

μPM: Microprocessor mode: μPM = 0 sets the 8259A for MCS-80, 85 system operation, μPM = 1 sets the 8259A for iAPX 86 system operation.

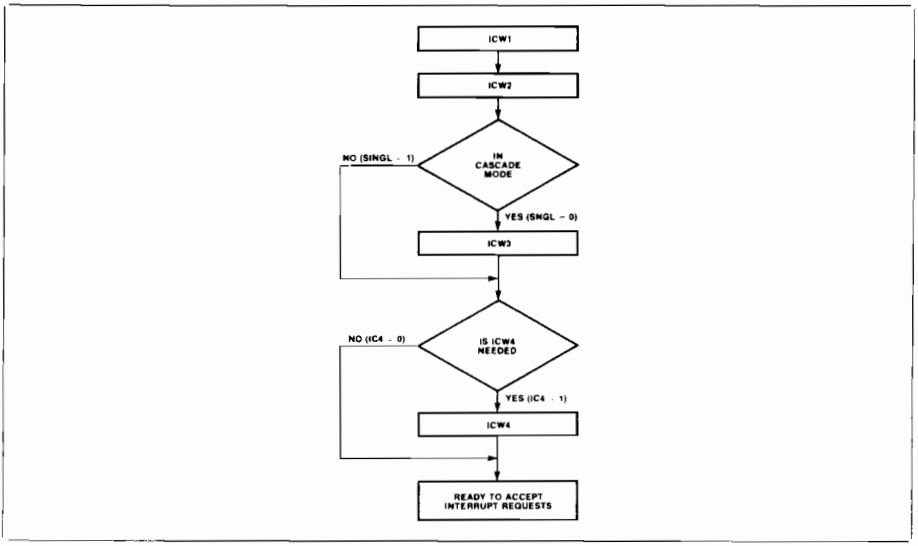
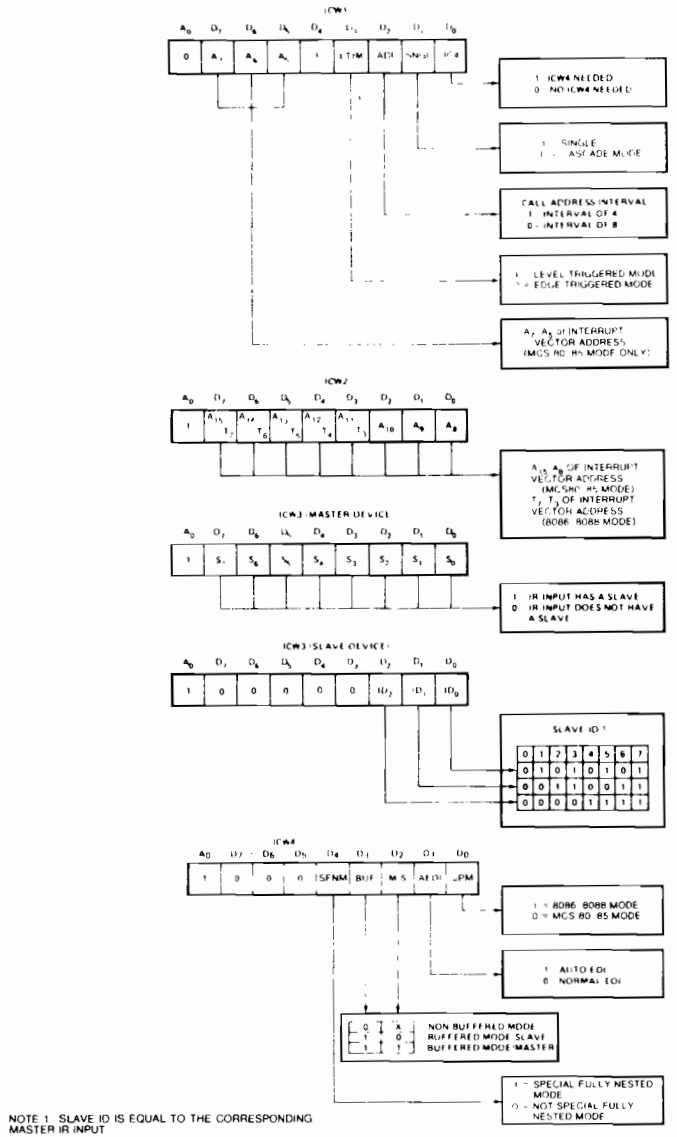


Figure 6. Initialization Sequence



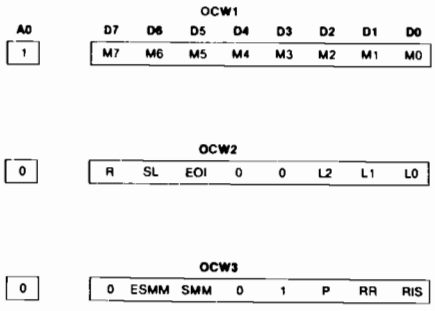
NOTE 1. SLAVE ID IS EQUAL TO THE CORRESPONDING MASTER IR INPUT

Figure 7. Initialization Command Word Format

OPERATION COMMAND WORDS (OCWs)

After the Initialization Command Words (ICWs) are programmed into the 8259A, the chip is ready to accept interrupt requests at its input lines. However, during the 8259A operation, a selection of algorithms can command the 8259A to operate in various modes through the Operation Command Words (OCWs)

OPERATION CONTROL WORDS (OCWs)



OPERATION CONTROL WORD 1 (OCW1)

OCW1 sets and clears the mask bits in the interrupt Mask Register (IMR). $M_7 - M_0$ represent the eight mask bits. M = 1 indicates the channel is masked (inhibited), M = 0 indicates the channel is enabled.

OPERATION CONTROL WORD 2 (OCW2)

R, SL, EOI — These three bits control the Rotate and End of Interrupt modes and combinations of the two. A chart of these combinations can be found on the Operation Command Word Format.

L_2, L_1, L_0—These bits determine the interrupt level acted upon when the SL bit is active.

OPERATION CONTROL WORD 3 (OCW3)

ESMM — Enable Special Mask Mode. When this bit is set to 1 it enables the SMM bit to set or reset the Special Mask Mode. When ESMM = 0 the SMM bit becomes a "don't care".

SMM — Special Mask Mode. If ESMM = 1 and SMM = 1 the 8259A will enter Special Mask Mode. If ESMM = 1 and SMM = 0 the 8259A will revert to normal mask mode. When ESMM = 0, SMM has no effect.

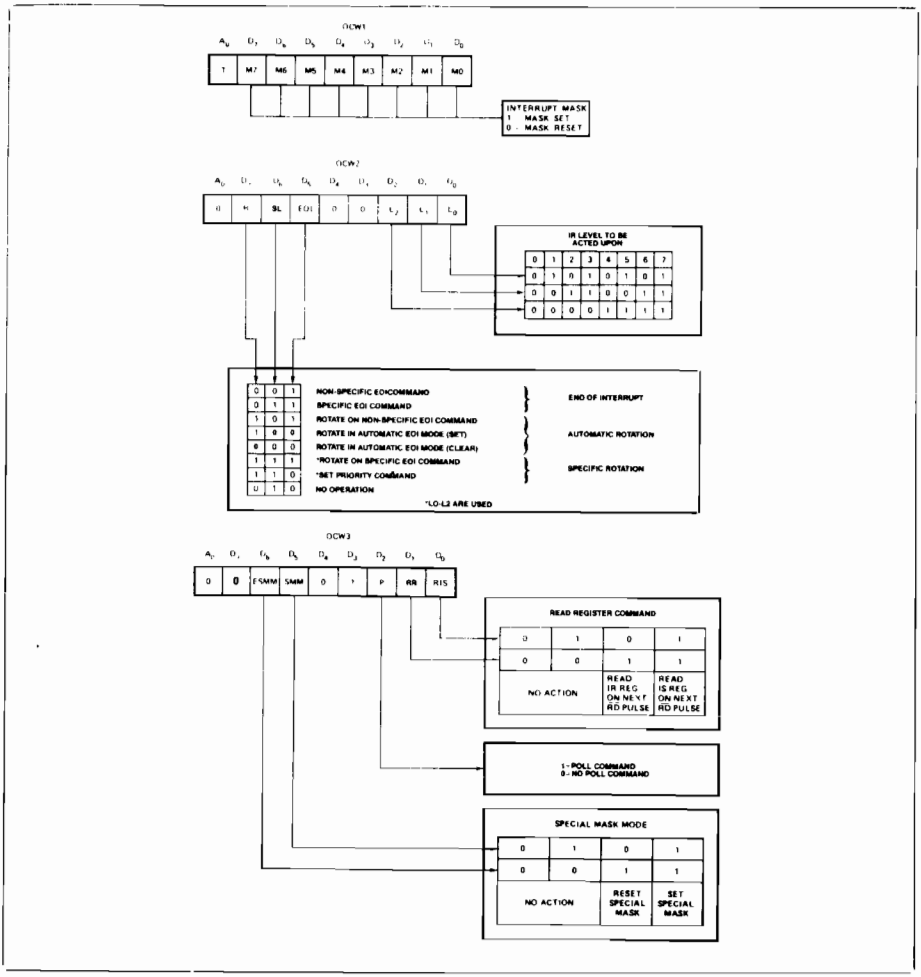


Figure 8. Operation Command Word Format

FULLY NESTED MODE

This mode is entered after initialization unless another mode is programmed. The interrupt requests are ordered in priority form 0 through 7 (0 highest). When an interrupt is acknowledged the highest priority request is determined and its vector placed on the bus. Additionally, a bit of the Interrupt Service register (ISO-7) is set. This bit remains set until the microprocessor issues an End of Interrupt (EOI) command immediately before returning from the service routine, or if AEOI (Automatic End of Interrupt) bit is set, until the trailing edge of the last INTA. While the IS bit is set, all further interrupts of the same or lower priority are inhibited, while higher levels will generate an interrupt (which will be acknowledged only if the microprocessor internal Interrupt enable flip-flop has been re-enabled through software).

After the initialization sequence, IR0 has the highest priority and IR7 the lowest. Priorities can be changed, as will be explained, in the rotating priority mode.

END OF INTERRUPT (EOI)

The In Service (IS) bit can be reset either automatically following the trailing edge of the last in sequence $\overline{\text{INTA}}$ pulse (when AEOI bit in ICW1 is set) or by a command word that must be issued to the 8259A before returning from a service routine (EOI command). An EOI command must be issued twice if in the Cascade mode, once for the master and once for the corresponding slave.

There are two forms of EOI command: Specific and Non-Specific. When the 8259A is operated in modes which preserve the fully nested structure, it can determine which IS bit to reset on EOI. When a Non-Specific EOI command is issued the 8259A will automatically reset the highest IS bit of those that are set, since in the fully nested mode the highest IS level was necessarily the last level acknowledged and serviced. A non-specific EOI can be issued with OCW2 (EOI = 1, SL = 0, R = 0).

When a mode is used which may disturb the fully nested structure, the 8259A may no longer be able to determine the last level acknowledged. In this case a Specific End of Interrupt must be issued which includes as part of the command the IS level to be reset. A specific EOI can be issued with OCW2 (EOI = 1, SL = 1, R = 0, and LO-L2 is the binary level of the IS bit to be reset).

It should be noted that an IS bit that is masked by an IMR bit will not be cleared by a non-specific EOI if the 8259A is in the Special Mask Mode.

AUTOMATIC END OF INTERRUPT (AEOI) MODE

If AEOI = 1 in ICW4, then the 8259A will operate in AEOI mode continuously until reprogrammed by ICW4. In this mode the 8259A will automatically perform a non-specific EOI operation at the trailing edge of the last interrupt acknowledge pulse (third pulse in MCS-80/85, second in iAPX 86). Note that from a system standpoint, this mode should be used only when a nested multilevel interrupt structure is not required within a single 8259A.

The AEOI mode can only be used in a master 8259A and not a slave.

AUTOMATIC ROTATION (Equal Priority Devices)

In some applications there are a number of interrupting devices of equal priority. In this mode a device, after being serviced, receives the lowest priority, so a device requesting an interrupt will have to wait, in the worst case until each of 7 other devices are serviced at most *once*. For example, if the priority and "in service" status is:

Before Rotate (IR4 the highest priority requiring service)

	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
"IS" Status	0	1	0	1	0	0	0	0
	Lowest Priority							Highest Priority
Priority Status	7	6	5	4	3	2	1	0

After Rotate (IR4 was serviced, all other priorities rotated correspondingly)

	IS7	IS6	IS5	IS4	IS3	IS2	IS1	IS0
"IS" Status	0	1	0	0	0	0	0	0
	Highest Priority							Lowest Priority
Priority Status	2	1	0	7	6	5	4	3

There are two ways to accomplish Automatic Rotation using OCW2, the Rotation on Non-Specific EOI Command (R = 1, SL = 0, EOI = 1) and the Rotate in Automatic EOI Mode which is set by (R = 1, SL = 0, EOI = 0) and cleared by (R = 0, SL = 0, EOI = 0).

SPECIFIC ROTATION (Specific Priority)

The programmer can change priorities by programming the bottom priority and thus fixing all other priorities; i.e., if IR5 is programmed as the bottom priority device, then IR6 will have the highest one.

The Set Priority command is issued in OCW2 where: R = 1, SL = 1; LO-L2 is the binary priority level code of the bottom priority device.

Observe that in this mode internal status is updated by software control during OCW2. However, it is independent of the End of Interrupt (EOI) command (also executed by OCW2). Priority changes can be executed during an EOI command by using the Rotate on Specific EOI command in OCW2 (R = 1, SL = 1, EOI = 1 and LO-L2 = IR level to receive bottom priority).

INTERRUPT MASKS

Each Interrupt Request input can be masked individually by the Interrupt Mask Register (IMR) programmed through OCW1. Each bit in the IMR masks one interrupt channel if it is set (1). Bit 0 masks IR0, Bit 1 masks IR1 and so forth. Masking an IR channel does not affect the other channels operation.

A

SPECIAL MASK MODE

Some applications may require an interrupt service routine to dynamically alter the system priority structure during its execution under software control. For example, the routine may wish to inhibit lower priority requests for a portion of its execution but enable some of them for another portion.

The difficulty here is that if an Interrupt Request is acknowledged and an End of Interrupt command did not reset its IS bit (i.e., while executing a service routine), the 8259A would have inhibited all lower priority requests with no easy way for the routine to enable them

That is where the Special Mask Mode comes in. In the special Mask Mode, when a mask bit is set in OCW1, it inhibits further interrupts at that level *and enables* interrupts from *all other* levels (lower as well as higher) that are not masked.

Thus, any interrupts may be selectively enabled by loading the mask register.

The special Mask Mode is set by OCW3 where: SSMM = 1, SMM = 1, and cleared where SSMM = 1, SMM = 0.

POLL COMMAND

In this mode the INT output is not used or the microprocessor internal Interrupt Enable flip-flop is reset, disabling its interrupt input. Service to devices is achieved by software using a Poll command.

The Poll command is issued by setting P = "1" in OCW3. The 8259A treats the next $\overline{RD}$ pulse to the 8259A (i.e., $\overline{RD} = 0$, $\overline{CS} = 0$) as an interrupt acknowledge, sets the appropriate IS bit if there is a request, and reads the priority level. Interrupt is frozen from $\overline{WR}$ to $\overline{RD}$.

The word enabled onto the data bus during $\overline{RD}$ is:

D7	D6	D5	D4	D3	D2	D1	D0
I	—	—	—	—	W2	W1	W0

W0-W2: Binary code of the highest priority level requesting service.

I: Equal to a "1" if there is an interrupt.

This mode is useful if there is a routine command common to several levels so that the $\overline{INTA}$ sequence is not needed (saves ROM space). Another application is to use the poll mode to expand the number of priority levels to more than 64.

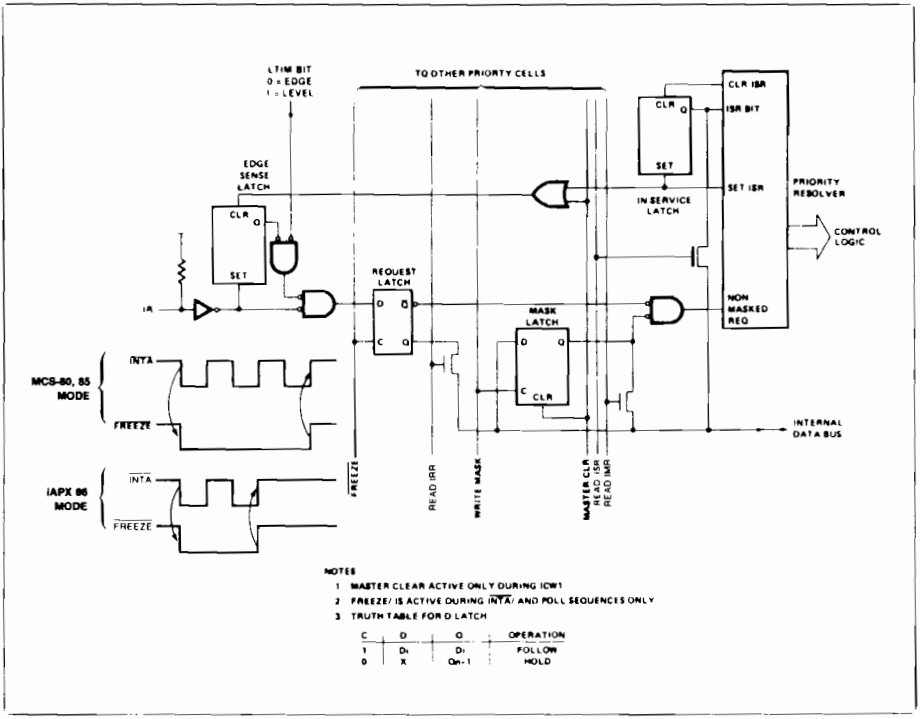


Figure 9. Priority Cell—Simplified Logic Diagram

READING THE 8259A STATUS

The input status of several internal registers can be read to update the user information on the system. The following registers can be read via OCW3 (IRR and ISR or OCW1 [IMR]).

Interrupt Request Register (IRR): 8-bit register which contains the levels requesting an interrupt to be acknowledged. The highest request level is reset from the IRR when an interrupt is acknowledged. (Not affected by IMR.)

In-Service Register (ISR): 8-bit register which contains the priority levels that are being serviced. The ISR is updated when an End of Interrupt Command is issued.

Interrupt Mask Register: 8-bit register which contains the interrupt request lines which are masked.

The IRR can be read when, prior to the RD pulse, a Read Register Command is issued with OCW3 (RR = 1, RIS = 0.)

The ISR can be read when, prior to the RD pulse, a Read Register Command is issued with OCW3 (RR = 1, RIS = 1).

There is no need to write an OCW3 before every status read operation, as long as the status read corresponds with the previous one; i.e., the 8259A "remembers" whether the IRR or ISR has been previously selected by the OCW3. This is not true when poll is used.

After initialization the 8259A is set to IRR.

For reading the IMR, no OCW3 is needed. The output data bus will contain the IMR whenever $\overline{RD}$ is active and A0 = 1 (OCW1).

Polling overrides status read when P = 1, RR = 1 in OCW3.

EDGE AND LEVEL TRIGGERED MODES

This mode is programmed using bit 3 in ICW1.

If LTIM = '0', an interrupt request will be recognized by a low to high transition on an IR input. The IR input can remain high without generating another interrupt.

If LTIM = '1', an interrupt request will be recognized by a 'high' level on IR input, and there is no need for an edge detection. The interrupt request must be removed before the EOI command is issued or the CPU interrupt is enabled to prevent a second interrupt from occurring.

The priority cell diagram shows a conceptual circuit of the level sensitive and edge sensitive input circuitry of the 8259A. Be sure to note that the request latch is a transparent D type latch.

In both the edge and level triggered modes the IR inputs must remain high until after the falling edge of the first INTA. If the IR input goes low before this time a DEFAULT IR7 will occur when the CPU acknowledges the interrupt. This can be a useful safeguard for detecting interrupts caused by spurious noise glitches on the IR inputs. To implement this feature the IR7 routine is used for "clean up" simply executing a return instruction, thus ignoring the interrupt. If IR7 is needed for other purposes a default IR7 can still be detected by reading the ISR. A normal IR7 interrupt will set the corresponding ISR bit, a default IR7 won't. If a default IR7 routine occurs during a normal IR7 routine, however, the ISR will remain set. In this case it is necessary to keep track of whether or not the IR7 routine was previously entered. If another IR7 occurs it is a default.

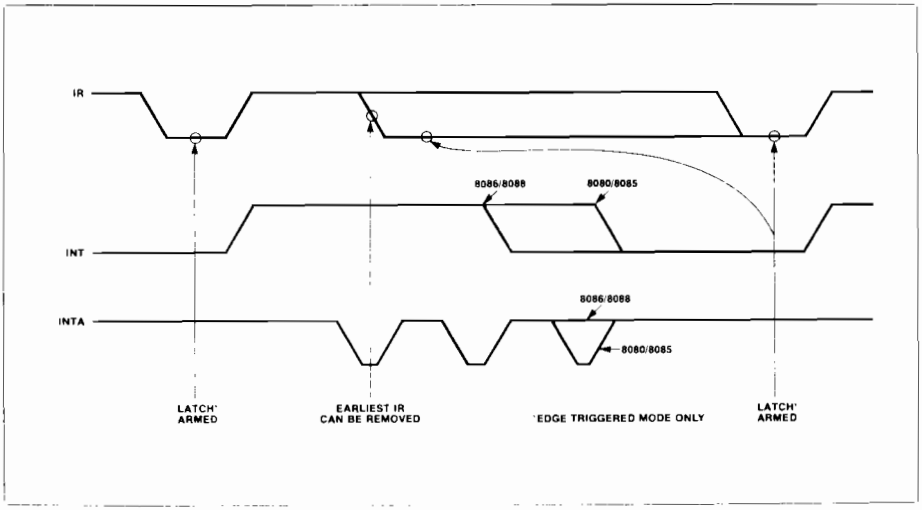


Figure 10. IR Triggering Timing Requirements

THE SPECIAL FULLY NESTED MODE

This mode will be used in the case of a big system where cascading is used, and the priority has to be conserved within each slave. In this case the fully nested mode will be programmed to the master (using ICW4). This mode is similar to the normal nested mode with the following exceptions:

a. When an interrupt request from a certain slave is in service this slave is not locked out from the master's priority logic and further interrupt requests from higher priority IR's within the slave will be recognized by the master and will initiate interrupts to the processor. (In the normal nested mode a slave is masked out when its request is in service and no higher requests from the same slave can be serviced.)

b. When exiting the Interrupt Service routine the software has to check whether the interrupt serviced was the only one from that slave. This is done by sending a non-specific End of Interrupt (EOI) command to the slave and then reading its In-Service register and checking for zero. If it is empty, a non-specific EOI can be sent to the master too. If not, no EOI should be sent.

BUFFERED MODE

When the 8259A is used in a large system where bus driving buffers are required on the data bus and the cascading mode is used, there exists the problem of enabling buffers.

The buffered mode will structure the 8259A to send an enable signal on $\overline{SP}/\overline{EN}$ to enable the buffers. In this mode, whenever the 8259A's data bus outputs are enabled, the $\overline{SP}/\overline{EN}$ output becomes active.

This modification forces the use of software programming to determine whether the 8259A is a master or a slave. Bit 3 in ICW4 programs the buffered mode, and bit 2 in ICW4 determines whether it is a master or a slave.

CASCADE MODE

The 8259A can be easily interconnected in a system of one master with up to eight slaves to handle up to 64 priority levels.

The master controls the slaves through the 3 line cascade bus. The cascade bus acts like chip selects to the slaves during the $\overline{INTA}$ sequence.

In a cascade configuration, the slave interrupt outputs are connected to the master interrupt request inputs. When a slave request line is activated and afterwards acknowledged, the master will enable the corresponding slave to release the device routine address during bytes 2 and 3 of INTA. (Byte 2 only for 8086/8088).

The cascade bus lines are normally low and will contain the slave address code from the trailing edge of the first INTA pulse to the trailing edge of the third pulse. Each 8259A in the system must follow a separate initialization sequence and can be programmed to work in a different mode. An EOI command must be issued twice: once for the master and once for the corresponding slave. An address decoder is required to activate the Chip Select (CS) input of each 8259A.

The cascade lines of the Master 8259A are activated only for slave inputs, non slave inputs leave the cascade line inactive (low).

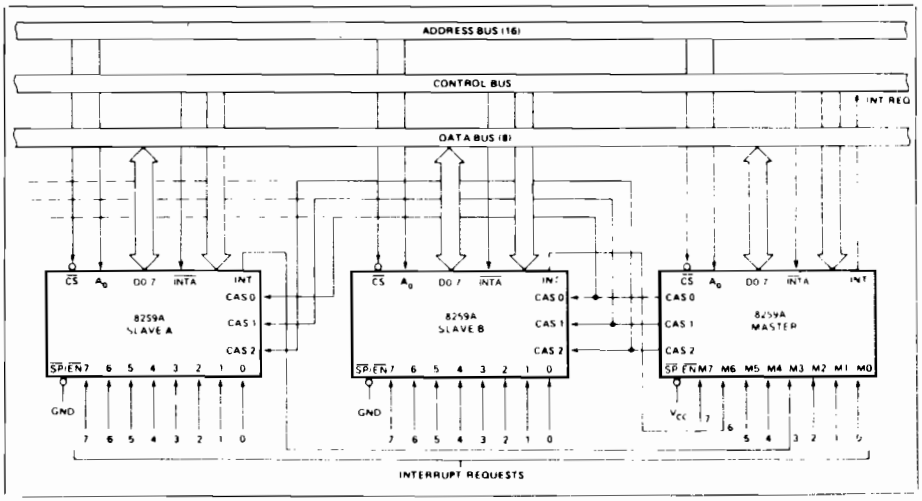


Figure 11. Cascading the 8259A

A.C. CHARACTERISTICS (Continued)

Symbol	Parameter	8259A-8		8259A		8259A-2		Units	Test Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
*TCHCL	End of Command to next Command (Not same command type)	500		500		500		ns	
	End of $\overline{INTA}$ sequence to next $\overline{INTA}$ sequence.								

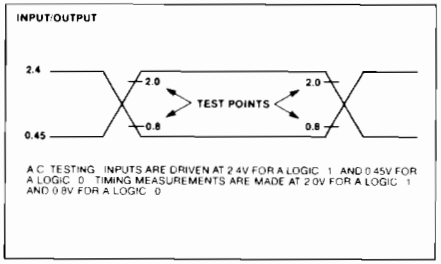
*Worst case timing for TCHCL in an actual microprocessor system is typically much greater than 500 ns (i.e. 8085A = 1.6μs, 8085A-2 = 1μs, 8086 = 1μs, 8086-2 = 625 ns)

NOTE: This is the low time required to clear the input latch in the edge triggered mode.

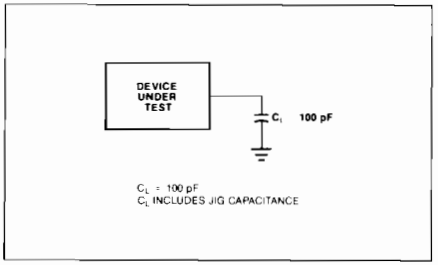
TIMING RESPONSES

Symbol	Parameter	8259A-8		8259A		8259A-2		Units	Test Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
TRLDV	Data Valid from $\overline{RD}$/$\overline{INTA}$↓		300		200		120	ns	C of Data Bus = 100 pF
TRHDZ	Data Float after $\overline{RD}$/$\overline{INTA}$↑	10	200	10	100	10	85	ns	C of Data Bus Max test C = 100 pF Min test C = 15 pF
TJHIH	Interrupt Output Delay		400		350		300	ns	
TIALCV	Cascade Valid from First $\overline{INTA}$↓ (Master Only)		565		565		360	ns	C_{INT} = 100 pF
TRLEL	Enable Active from $\overline{RD}$↓ or $\overline{INTA}$↓		160		125		100	ns	$C_{CASCADE}$ = 100 pF
TRHEH	Enable Inactive from $\overline{RD}$↑ or $\overline{INTA}$↑		325		150		150	ns	
TAHDV	Data Valid from Stable Address		350		200		200	ns	
TCVDV	Cascade Valid to Valid Data		300		300		200	ns	

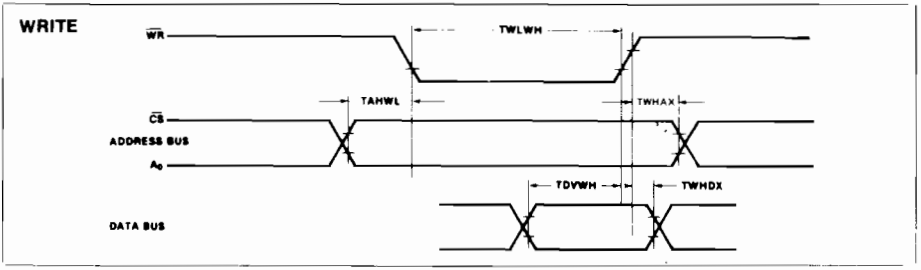
A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. TESTING LOAD CIRCUIT

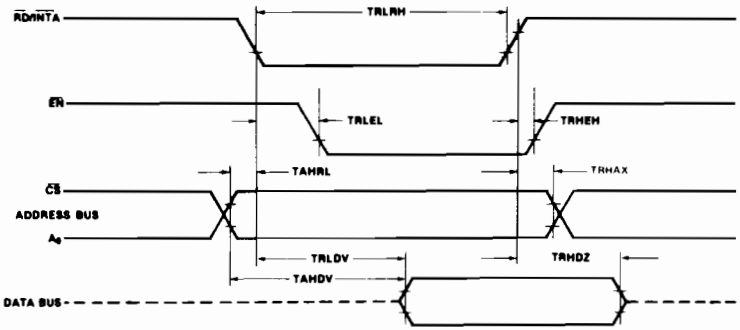


WAVEFORMS

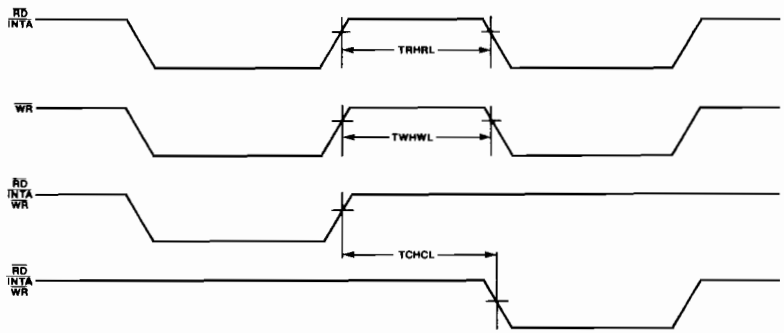


WAVEFORMS (Continued)

READ/INTA

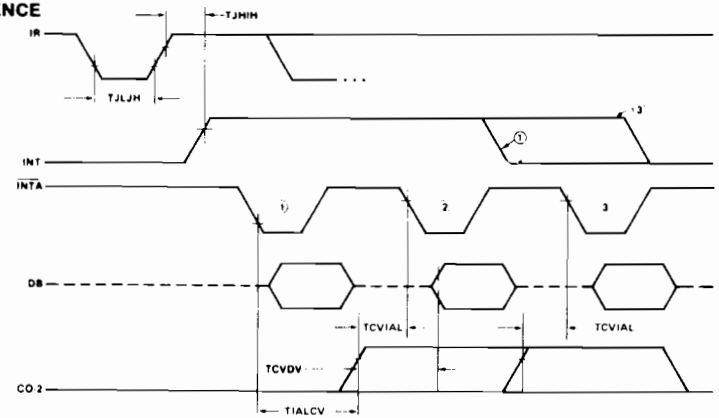


OTHER TIMING



WAVEFORMS (Continued)

INTA SEQUENCE



NOTES: Interrupt output must remain HIGH at least until leading edge of first INTA.
1. Cycle 1 in iAPX 86, iAPX 88 systems, the Data Bus is not active.

8251A
PROGRAMMABLE COMMUNICATION INTERFACE

- **Synchronous and Asynchronous Operation**
- **Synchronous 5-8 Bit Characters; Internal or External Character Synchronization; Automatic Sync Insertion**
- **Asynchronous 5-8 Bit Characters; Clock Rate—1, 16 or 64 Times Baud Rate; Break Character Generation; 1, 1½, or 2 Stop Bits; False Start Bit Detection; Automatic Break Detect and Handling**
- **Synchronous Baud Rate—DC to 64K Baud**
- **Asynchronous Baud Rate—DC to 19.2K Baud**
- **Full-Duplex, Double-Buffered Transmitter and Receiver**
- **Error Detection—Parity, Overrun and Framing**
- **Compatible with an Extended Range of Intel Microprocessors**
- **28-Pin DIP Package**
- **All Inputs and Outputs are TTL Compatible**
- **Available in EXPRESS**
  —Standard Temperature Range
  —Extended Temperature Range

The Intel® 8251A is the enhanced version of the industry standard, Intel 8251 Universal Synchronous/Asynchronous Receiver/Transmitter (USART), designed for data communications with Intel's microprocessor families such as MCS-48, 80, 85, and iAPX-86, 88. The 8251A is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique presently in use (including IBM "bi-sync"). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously, it can receive serial data streams and convert them into parallel data characters for the CPU. The USART will signal the CPU whenever it can accept a new character for transmission or whenever it has received a character for the CPU. The CPU can read the complete status of the USART at any time. These include data transmission errors and control signals such as SYNDET, TxEMPTY. The chip is fabricated using N-channel silicon gate technology.

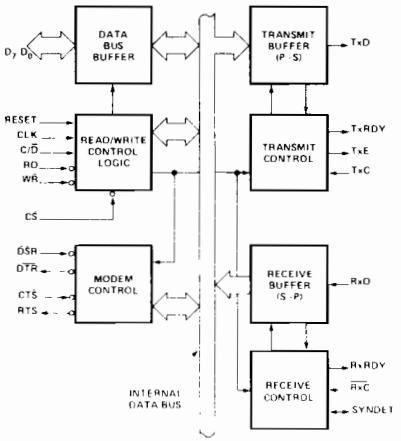


Figure 1. Block Diagram

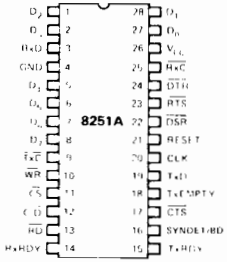
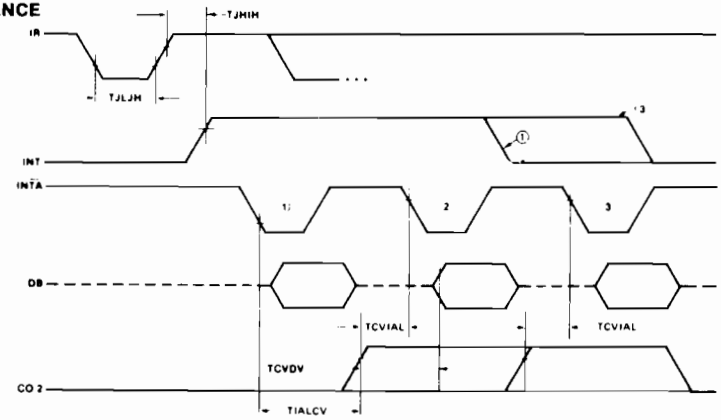


Figure 2. Pin Configuration

WAVEFORMS (Continued)

INTA SEQUENCE



NOTES: Interrupt output must remain HIGH at least until leading edge of first INTA.
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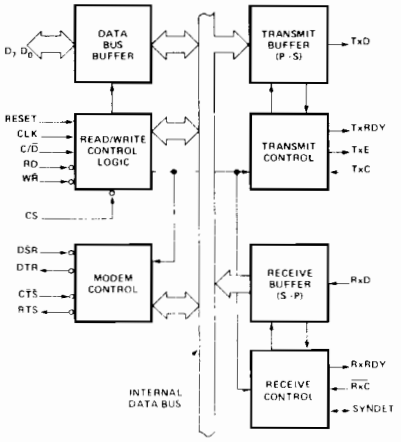


Figure 1. Block Diagram

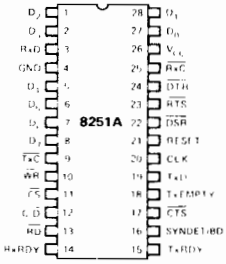


Figure 2. Pin Configuration

FEATURES AND ENHANCEMENTS

The 8251A is an advanced design of the industry standard USART, the Intel® 8251. The 8251A operates with an extended range of Intel microprocessors and maintains compatibility with the 8251. Familiarization time is minimal because of compatibility and involves only knowing the additional features and enhancements, and reviewing the AC and DC specifications of the 8251A.

The 8251A incorporates all the key features of the 8251 and has the following additional features and enhancements:

- 8251A has double-buffered data paths with separate I/O registers for control, status, Data In, and Data Out, which considerably simplifies control programming and minimizes CPU overhead.
- In asynchronous operations, the Receiver detects and handles "break" automatically, relieving the CPU of this task.
- A refined Rx initialization prevents the Receiver from starting when in "break" state, preventing unwanted interrupts from a disconnected USART.
- At the conclusion of a transmission, TxD line will always return to the marking state unless SBRK is programmed.
- Tx Enable logic enhancement prevents a Tx Disable command from halting transmission until all data previously written has been transmitted. The logic also prevents the transmitter from turning off in the middle of a word.
- When External Sync Detect is programmed, Internal Sync Detect is disabled, and an External Sync Detect status is provided via a flip-flop which clears itself upon a status read.
- Possibility of false sync detect is minimized by ensuring that if double character sync is programmed, the characters be contiguously detected and also by clearing the Rx register to all ones whenever Enter Hunt command is issued in Sync mode.
- As long as the 8251A is not selected, the $\overline{RD}$ and $\overline{WR}$ do not affect the internal operation of the device.
- The 8251A Status can be read at any time but the status update will be inhibited during status read.
- The 8251A is free from extraneous glitches and has enhanced AC and DC characteristics, providing higher speed and better operating margins.
- Synchronous Baud rate from DC to 64K.

FUNCTIONAL DESCRIPTION

General

The 8251A is a Universal Synchronous/Asynchronous Receiver/Transmitter designed for a wide range of Intel microcomputers such as 8048, 8080, 8085, 8086 and 8088. Like other I/O devices in a microcomputer system, its functional configuration is programmed by the system's software for maximum flexibility. The 8251A can support most serial data techniques in use, including IBM "bi-sync."

In a communication environment an interface device must convert parallel format system data into serial format for transmission and convert incoming serial format data into parallel system data for reception. The interface device must also delete or insert bits or characters that are functionally unique to the communication technique. In essence, the interface should appear "transparent" to the CPU, a simple input or output of byte-oriented system data.

Data Bus Buffer

This 3-state, bidirectional, 8-bit buffer is used to interface the 8251A to the system Data Bus. Data is transmitted or received by the buffer upon execution of INput or OUTput instructions of the CPU. Control words, Command words and Status information are also transferred through the Data Bus Buffer. The Command Status, Data-In and Data-Out registers are separate, 8-bit registers communicating with the system bus through the Data Bus Buffer.

This functional block accepts inputs from the system Control bus and generates control signals for overall device operation. It contains the Control Word Register and Command Word Register that store the various control formats for the device functional definition.

RESET (Reset)

A "high" on this input forces the 8251A into an "Idle" mode. The device will remain at "Idle" until a new set of control words is written into the 8251A to program its functional definition. Minimum RESET pulse width is 6 t_{CY} (clock must be running).

A command reset operation also puts the device into the "Idle" state.

CLK (Clock)

The CLK input is used to generate internal device timing and is normally connected to the Phase 2 (TTL) output of the Clock Generator. No external inputs or outputs are referenced to CLK but the frequency of CLK must be greater than 30 times the Receiver or Transmitter data bit rates.

$\overline{WR}$ (Write)

A "low" on this input informs the 8251A that the CPU is writing data or control words to the 8251A.

$\overline{RD}$ (Read)

A "low" on this input informs the 8251A that the CPU is reading data or status information from the 8251A.

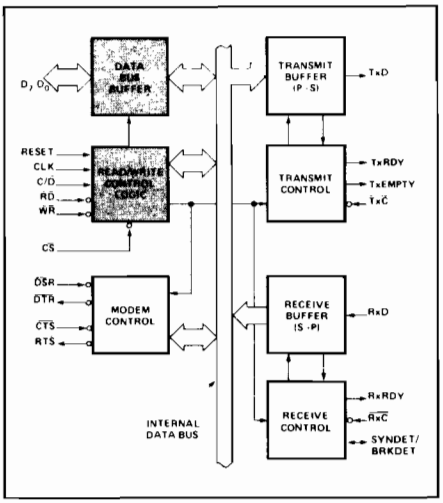


Figure 3. 8251A Block Diagram Showing Data Bus Buffer and Read/Write Logic Functions

C/$\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	8251A DATA → DATA BUS
0	1	0	0	DATA BUS → 8251A DATA
1	0	1	0	STATUS → DATA BUS
1	1	0	0	DATA BUS → CONTROL
X	1	1	0	DATA BUS → 3-STATE
X	X	X	1	DATA BUS → 3-STATE

C/$\overline{D}$ (Control/Data)

This input, in conjunction with the $\overline{WR}$ and $\overline{RD}$ inputs, informs the 8251A that the word on the Data Bus is either a data character, control word or status information.

1 = CONTROL/STATUS; 0 = DATA.

$\overline{CS}$ (Chip Select)

A "low" on this input selects the 8251A. No reading or writing will occur unless the device is selected. When $\overline{CS}$ is high, the Data Bus is in the float state and $\overline{RD}$ and $\overline{WR}$ have no effect on the chip.

Modem Control

The 8251A has a set of control inputs and outputs that can be used to simplify the interface to almost any modem. The modem control signals are general purpose in nature and can be used for functions other than modem control, if necessary.

$\overline{DSR}$ (Data Set Ready)

The $\overline{DSR}$ input signal is a general-purpose, 1-bit inverting input port. Its condition can be tested by the CPU using a Status Read operation. The $\overline{DSR}$ input is normally used to test modem conditions such as Data-Set Ready.

$\overline{DTR}$ (Data Terminal Ready)

The $\overline{DTR}$ output signal is a general-purpose, 1-bit inverting output port. It can be set "low" by programming the appropriate bit in the Command Instruction word. The $\overline{DTR}$ output signal is normally used for modem control such as Data Terminal Ready.

$\overline{RTS}$ (Request to Send)

The $\overline{RTS}$ output signal is a general-purpose, 1-bit inverting output port. It can be set "low" by programming the appropriate bit in the Command Instruction word. The $\overline{RTS}$ output signal is normally used for modem control such as Request to Send.

$\overline{CTS}$ (Clear to Send)

A "low" on this input enables the 8251A to transmit serial data if the Tx Enable bit in the Command byte is set to a "one." If either a Tx Enable off or $\overline{CTS}$ off condition occurs while the Tx is in operation, the Tx will transmit all the data in the USART, written prior to Tx Disable command before shutting down.

Transmitter Buffer

The Transmitter Buffer accepts parallel data from the Data Bus Buffer, converts it to a serial bit stream, inserts the appropriate characters or bits (based on the communication technique) and outputs a composite serial stream of data on the TxD output pin on the falling edge of $\overline{TxC}$. The transmitter will begin transmission upon being enabled if $\overline{CTS}$ = 0. The TxD line will be held in the marking state immediately upon a master Reset or when Tx Enable or $\overline{CTS}$ is off or the transmitter is empty.

Transmitter Control

The Transmitter Control manages all activities associated with the transmission of serial data. It accepts and issues signals both externally and internally to accomplish this function.

TxRDY (Transmitter Ready)

This output signals the CPU that the transmitter is ready to accept a data character. The TxRDY output pin can be used as an interrupt to the system, since it is masked by TxEnable; or, for Polled operation, the CPU can check TxRDY using a Status Read operation. TxRDY is automatically reset by the leading edge of $\overline{WR}$ when a data character is loaded from the CPU.

Note that when using the Polled operation, the TxRDY status bit is *not* masked by TxEnable, but will only indicate the Empty/Full Status of the Tx Data Input Register.

TxE (Transmitter Empty)

When the 8251A has no characters to send, the TxEMPTY output will go "high." It resets upon receiving a character from CPU if the transmitter is enabled. TxEMPTY remains high when the transmitter is disabled. TxEMPTY can be used to indicate the end of a transmission mode, so that the CPU "knows" when to "turn the line around" in the half-duplex operational mode.

In the Synchronous mode, a "high" on this output indicates that a character has not been loaded and the SYNC character or characters are about to be or are being transmitted automatically as "fillers." TxEMPTY does not go low when the SYNC characters are being shifted out.

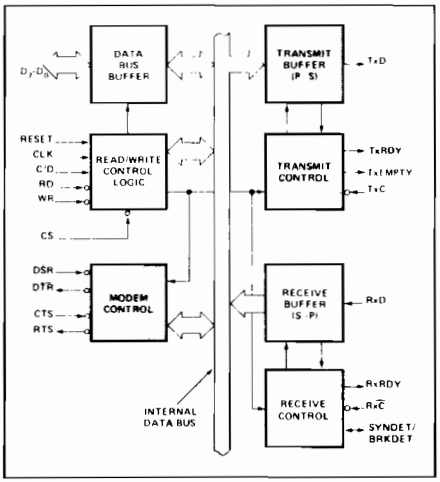


Figure 4. 8251A Block Diagram Showing Modem and Transmitter Buffer and Control Functions

$\overline{TxC}$ (Transmitter Clock)

The Transmitter Clock controls the rate at which the character is to be transmitted. In the Synchronous transmission mode, the Baud Rate (1x) is equal to the $\overline{TxC}$ frequency. In Asynchronous transmission mode, the baud rate is a fraction of the actual $\overline{TxC}$ frequency. A portion of the mode instruction selects this factor; it can be 1, 1/16 or 1/64 the $\overline{TxC}$.

For Example:

If Baud Rate equals 110 Baud,
$\overline{TxC}$ equals 110 Hz in the 1x mode.
$\overline{TxC}$ equals 1.72 kHz in the 16x mode.
$\overline{TxC}$ equals 7.04 kHz in the 64x mode.

The falling edge of $\overline{TxC}$ shifts the serial data out of the 8251A.

Receiver Buffer

The Receiver accepts serial data, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and sends an "assembled" character to the CPU. Serial data is input to RxD pin, and is clocked in on the rising edge of $\overline{RxC}$.

Receiver Control

This functional block manages all receiver-related activities which consists of the following features.

The RxD initialization circuit prevents the 8251A from mistaking an unused input line for an active low data line in the "break condition." Before starting to receive serial characters on the RxD line, a valid "1" must first be detected after a chip master Reset. Once this has been determined, a search for a valid low (Start bit) is enabled. This feature is only active in the asynchronous mode, and is only done once for each master Reset.

The False Start bit detection circuit prevents false starts due to a transient noise spike by first detecting the falling edge and then strobing the nominal center of the Start bit (RxD = low).

Parity error detection sets the corresponding status bit.

The Framing Error status bit is set if the Stop bit is absent at the end of the data byte (asynchronous mode).

RxRDY (Receiver Ready)

This output indicates that the 8251A contains a character that is ready to be input to the CPU. RxRDY can be connected to the interrupt structure of the CPU or, for polled operation, the CPU can check the condition of RxRDY using a Status Read operation.

RxEnable, when off, holds RxRDY in the Reset Condition. For Asynchronous mode, to set RxRDY, the Receiver must be enabled to sense a Start Bit and a complete character must be assembled and transferred to the Data Output Register. For Synchronous mode, to set RxRDY, the Receiver must be enabled and a character must finish assembly and be transferred to the Data Output Register.

Failure to read the received character from the Rx Data Output Register prior to the assembly of the next Rx Data character will set overrun condition error and the previous character will be written over and lost. If the Rx Data is being read by the CPU when the internal transfer is occurring, overrun error will be set and the old character will be lost.

$\overline{RxC}$ (Receiver Clock)

The Receiver Clock controls the rate at which the character is to be received. In Synchronous Mode, the Baud Rate (1x) is equal to the actual frequency of $\overline{RxC}$. In Asynchronous Mode, the Baud Rate is a fraction of the actual $\overline{RxC}$ frequency. A portion of the mode instruction selects this factor: 1, 1/16 or 1/64 the $\overline{RxC}$.

For example:

Baud Rate equals 300 Baud, if
$\overline{RxC}$ equals 300 Hz in the 1x mode;
$\overline{RxC}$ equals 4800 Hz in the 16x mode;
$\overline{RxC}$ equals 19.2 kHz in the 64x mode.

Baud Rate equals 2400 Baud, if
$\overline{RxC}$ equals 2400 Hz in the 1x mode;
$\overline{RxC}$ equals 38.4 kHz in the 16x mode;
$\overline{RxC}$ equals 153.6 kHz in the 64x mode.

Data is sampled into the 8251A on the rising edge of $\overline{RxC}$.

NOTE: In most communications systems, the 8251A will be handling both the transmission and reception operations of a single link. Consequently, the Receive and Transmit Baud Rates will be the same. Both $\overline{TxC}$ and $\overline{RxC}$ will require identical frequencies for this operation and can be tied together and connected to a single frequency source (Baud Rate Generator) to simplify the interface.

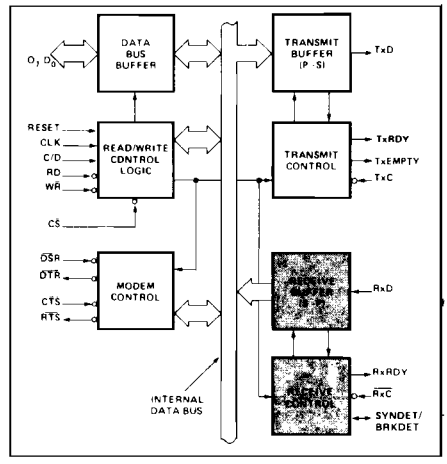


Figure 5. 8251A Block Diagram Showing Receiver Buffer and Control Functions

SYNDET (SYNC Detect/ BRKDET Break Detect)

This pin is used in Synchronous Mode for SYNDET and may be used as either input or output, programmable through the Control Word. It is reset to output mode low upon RESET. When used as an output (internal Sync mode), the SYNDET pin will go "high" to indicate that the 8251A has located the SYNC character in the Receive mode. If the 8251A is programmed to use double Sync characters (bisync), then SYNDET will go "high" in the middle of the last bit of the second Sync character. SYNDET is automatically reset upon a Status Read operation.

When used as an input (external SYNC detect mode), a positive going signal will cause the 8251A to start assembling data characters on the rising edge of the next $\overline{RxC}$. Once in SYNC, the "high" input signal can be removed. When External SYNC Detect is programmed, Internal SYNC Detect is disabled.

BREAK (Async Mode Only)

This output will go high whenever the receiver remains low through two consecutive stop bit sequences (including the start bits, data bits, and parity bits). Break Detect may also be read as a Status bit. It is reset only upon a master chip Reset or Rx Data returning to a "one" state.

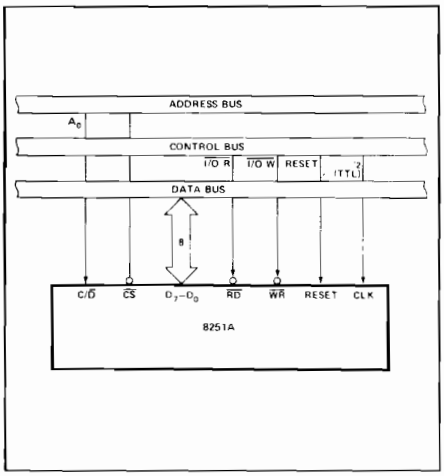


Figure 6. 8251A Interface to 8080 Standard System Bus

DETAILED OPERATION DESCRIPTION

General

The complete functional definition of the 8251A is programmed by the system's software. A set of control words must be sent out by the CPU to initialize the 8251A to support the desired communications format. These control words will program the: BAUD RATE, CHARACTER LENGTH, NUMBER OF STOP BITS, SYNCHRONOUS or ASYNCHRONOUS OPERATION, EVEN/ODD/OFF PARITY, etc. In the Synchronous Mode, options are also provided to select either internal or external character synchronization.

Once programmed, the 8251A is ready to perform its communication functions. The TxRDY output is raised "high" to signal the CPU that the 8251A is ready to receive a data character from the CPU. This output (TxRDY) is reset automatically when the CPU writes a character into the 8251A. On the other hand, the 8251A receives serial data from the MODEM or I/O device. Upon receiving an entire character, the RxRDY output is raised "high" to signal the CPU that the 8251A has a complete character ready for the CPU to fetch. RxRDY is reset automatically upon the CPU data read operation.

The 8251A cannot begin transmission until the Tx Enable (Transmitter Enable) bit is set in the Command Instruction and it has received a Clear To Send ($\overline{CTS}$) input. The TxD output will be held in the marking state upon Reset.

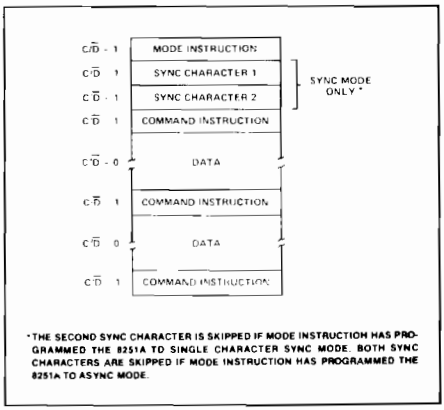


Figure 7. Typical Data Block

Programming the 8251A

Prior to starting data transmission or reception, the 8251A must be loaded with a set of control words generated by the CPU. These control signals define the complete functional definition of the 8251A and must immediately follow a Reset operation (internal or external).

The control words are split into two formats:

1. Mode Instruction
2. Command Instruction

Mode Instruction

This instruction defines the general operational characteristics of the 8251A. It must follow a Reset operation (internal or external). Once the Mode Instruction has been written into the 8251A by the CPU, SYNC characters or Command Instructions may be written.

Command Instruction

This instruction defines a word that is used to control the actual operation of the 8251A.

Both the Mode and Command Instructions must conform to a specified sequence for proper device operation (see Figure 7). The Mode Instruction must be written immediately following a Reset operation, prior to using the 8251A for data communication.

All control words written into the 8251A after the Mode Instruction will load the Command Instruction. Command Instructions can be written into the 8251A at any time in the data block during the operation of the 8251A. To return to the Mode Instruction format, the master Reset bit in the Command Instruction word can be set to initiate an internal Reset operation which automatically places the 8251A back into the Mode Instruction format. Command Instructions must follow the Mode Instructions or Sync characters.

Mode Instruction Definition

The 8251A can be used for either Asynchronous or Synchronous data communication. To understand how the Mode Instruction defines the functional operation of the 8251A, the designer can best view the device as two separate components, one Asynchronous and the other Synchronous, sharing the same package. The format definition can be changed only after a master chip Reset. For explanation purposes the two formats will be isolated.

NOTE: When parity is enabled it is not considered as one of the data bits for the purpose of programming the word length. The actual parity bit received on the Rx Data line cannot be read on the Data Bus. In the case of a programmed character length of less than 8 bits, the least significant Data Bus bits will hold the data; unused bits are "don't care" when writing data to the 8251A, and will be "zeros" when reading the data from the 8251A.

Asynchronous Mode (Transmission)

Whenever a data character is sent by the CPU the 8251A automatically adds a Start bit (low level) followed by the data bits (least significant bit first), and the programmed number of Stop bits to each character. Also, an even or odd Parity bit is inserted prior to the Stop bit(s), as defined by the Mode Instruction. The character is then transmitted as a serial data stream on the TxD output. The serial data is shifted out on the falling edge of $\overline{TxC}$ at a rate equal to 1, 1/16, or 1/64 that of the $\overline{TxC}$, as defined by the Mode Instruction. BREAK characters can be continuously sent to the TxD if commanded to do so.

When no data characters have been loaded into the 8251A the TxD output reamins "high" (marking) unless a Break (continuously low) has been programmed.

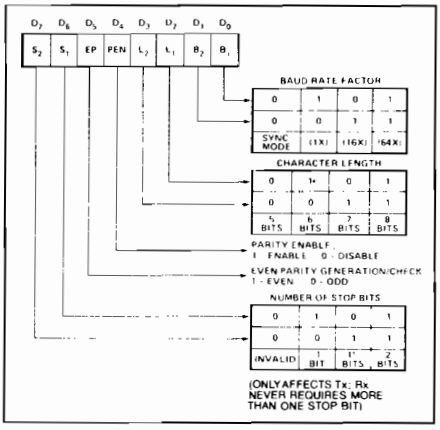


Figure 8. Mode Instruction Format, Asynchronous Mode

Asynchronous Mode (Receive)

The RxD line is normally high. A falling edge on this line triggers the beginning of a START bit. The validity of this START bit is checked by again strobing this bit at its nominal center (16X or 64X mode only). If a low is detected again, it is a valid START bit, and the bit counter will start counting. The bit counter thus locates the center of the data bits, the parity bit (if it exists) and the stop bits. If parity error occurs, the parity error flag is set. Data and parity bits are sampled on the RxD pin with the rising edge of $\overline{RxC}$. If a low level is detected as the STOP bit, the Framing Error flag will be set. The STOP bit signals the end of a character. Note that the *receiver* requires only *one* stop bit, regardless of the number of stop bits programmed. This character is then loaded into the parallel I/O buffer of the 8251A. The RxRDY pin is raised to signal the CPU that a character is ready to be fetched. If a previous character has not been fetched by the CPU, the present character replaces it in the I/O buffer, and the OVERRUN Error flag is raised (thus the previous character is lost). All of the error flags can be reset by an Error Reset Instruction. The occurrence of any of these errors will not affect the operation of the 8251A.

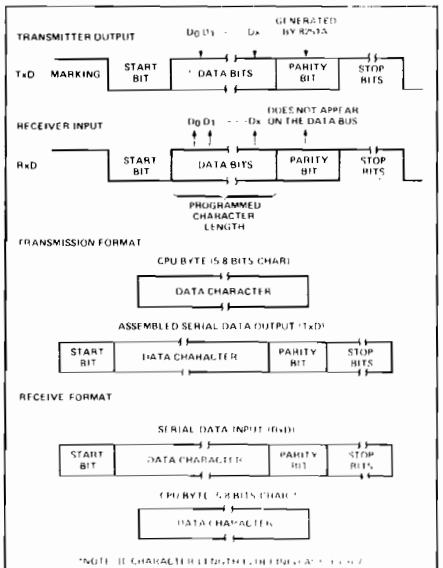
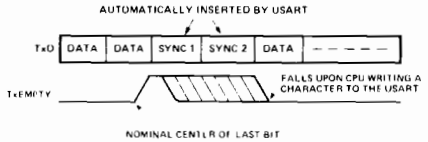


Figure 9. Asynchronous Mode

Synchronous Mode (Transmission)

The TxD output is continuously high until the CPU sends its first character to the 8251A which usually is a SYNC character. When the $\overline{CTS}$ line goes low, the first character is serially transmitted out. All characters are shifted out on the falling edge of $\overline{TxC}$. Data is shifted out at the same rate as the $\overline{TxC}$.

Once transmission has started, the data stream at the TxD output must continue at the $\overline{TxC}$ rate. If the CPU does not provide the 8251A with a data character before the 8251A Transmitter Buffers become empty, the SYNC characters (or character if in single SYNC character mode) will be automatically inserted in the TxD data stream. In this case, the TxEMPTY pin is raised high to signal that the 8251A is empty and SYNC characters are being sent out. TxEMPTY does not go low when the SYNC is being shifted out (see figure below). The TxEMPTY pin is internally reset by a data character being written into the 8251A.



Synchronous Mode (Receive)

In this mode, character synchronization can be internally or externally achieved. If the SYNC mode has been programmed, ENTER HUNT command should be included in the first command instruction word written. Data on the RxD pin is then sampled on the rising edge of $\overline{RxC}$. The content of the Rx buffer is compared at every bit boundary with the first SYNC character until a match occurs. If the 8251A has been programmed for two SYNC characters, the subsequent received character is also compared; when both SYNC characters have been detected, the USART ends the HUNT mode and is in character synchronization. The SYNDET pin is then set high, and is reset automatically by a STATUS READ. If parity is programmed, SYNDET will not be set until the middle of the parity bit instead of the middle of the last data bit.

In the external SYNC mode, synchronization is achieved by applying a high level on the SYNDET pin, thus forcing the 8251A out of the HUNT mode. The high level can be removed after one $\overline{RxC}$ cycle. An ENTER HUNT command has no effect in the asynchronous mode of operation.

Parity error and overrun error are both checked in the same way as in the Asynchronous Rx mode. Parity is checked when not in Hunt, regardless of whether the Receiver is enabled or not.

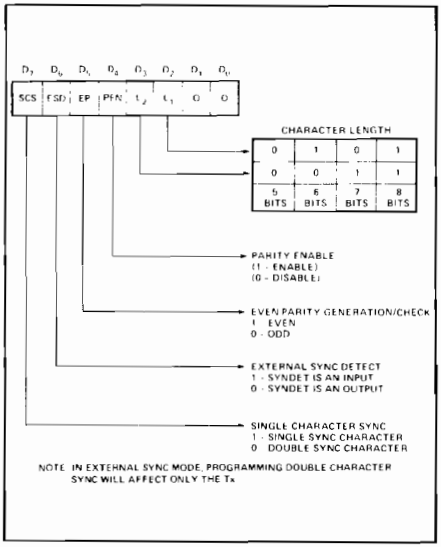


Figure 10. Mode Instruction Format, Synchronous Mode

The CPU can command the receiver to enter the HUNT mode if synchronization is lost. This will also set all the used character bits in the buffer to a "one," thus preventing a possible false SYNDET caused by data that happens to be in the Rx Buffer at ENTER HUNT time. Note that the SYNDET F/F is reset at each Status Read, regardless of whether internal or external SYNC has been programmed. This does not cause the 8251A to return to the HUNT mode. When in SYNC mode, but not in HUNT, Sync Detection is still functional, but only occurs at the "known" word boundaries. Thus, if one Status Read indicates SYNDET and a second Status Read also indicates SYNDET, then the programmed SYNDET characters have been received since the previous Status Read. (If double character sync has been programmed, then both sync characters have been contiguously received to gate a SYNDET indication.) When external SYNDET mode is selected, internal Sync Detect is disabled, and the SYNDET F/F may be set at any bit boundary.

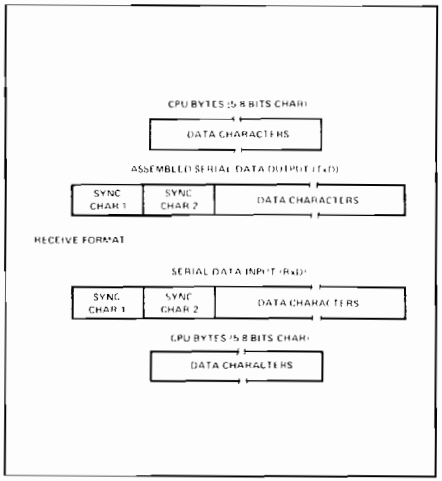


Figure 11. Data Format, Synchronous Mode

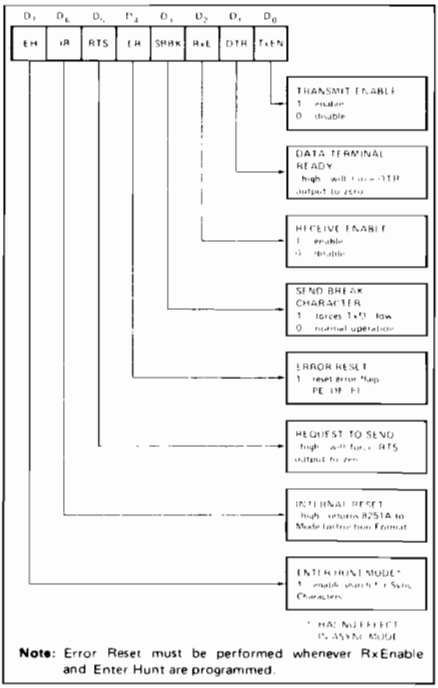
COMMAND INSTRUCTION DEFINITION

Once the functional definition of the 8251A has been programmed by the Mode Instruction and the sync characters are loaded (if in Sync Mode) then the device is ready to be used for data communication. The Command Instruction controls the actual operation of the selected format. Functions such as: Enable Transmit/Receive, Error Reset and Modem Controls are provided by the Command Instruction.

Once the Mode Instruction has been written into the 8251A and Sync characters inserted, if necessary, then all further "control writes" (C/D = 1) will load a Command Instruction. A Reset Operation (internal or external) will return the 8251A to the Mode Instruction format.

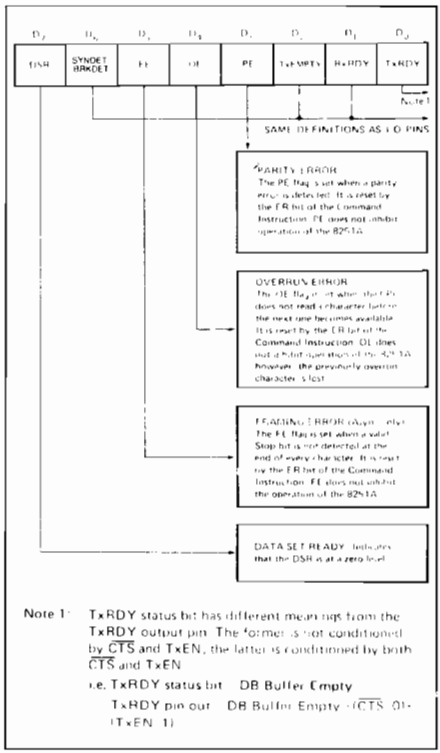
Note: Internal Reset on Power-up

When power is first applied, the 8251A may come up in the Mode, Sync character or Command format. To guarantee that the device is in the Command Instruction format before the Reset command is issued, it is safest to execute the worst-case initialization sequence (sync mode with two sync characters). Loading three 00Hs consecutively into the device with C/$\overline{D}$ = 1 configures sync operation and writes two dummy 00H sync characters. An Internal Reset command (40H) may then be issued to return the device to the "Idle" state.



Note: Error Reset must be performed whenever RxEnable and Enter Hunt are programmed.

Figure 12. Command Instruction Format



Note 1: TxRDY status bit has different meanings from the TxRDY output pin. The former is not conditioned by $\overline{CTS}$ and TxEN, the latter is conditioned by both $\overline{CTS}$ and TxEN.

i.e. TxRDY status bit — DB Buffer Empty

TxRDY pin out — DB Buffer Empty · ($\overline{CTS}$ · (TxEN · 1))

Figure 13. Status Read Format

STATUS READ DEFINITION

In data communication systems it is often necessary to examine the "status" of the active device to ascertain if errors have occurred or other conditions that require the processor's attention. The 8251A has facilities that allow the programmer to "read" the status of the device at any time during the functional operation. (Status update is inhibited during status read.)

A normal "read" command is issued by the CPU with C/$\overline{D}$ = 1 to accomplish this function.

Some of the bits in the Status Read Format have identical meanings to external output pins so that the 8251A can be used in a completely polled or interrupt-driven environment. TxRDY is an exception.

Note that status update can have a maximum delay of 28 clock periods from the actual event affecting the status.

APPLICATIONS OF THE 8251A

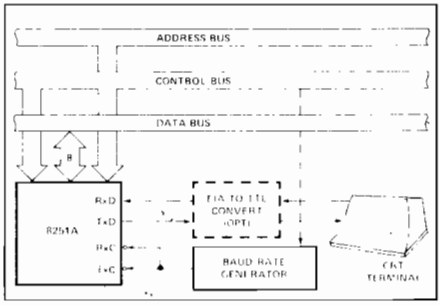


Figure 14. Asynchronous Serial Interface to CRT Terminal, DC—9600 Baud

AFN-01573D

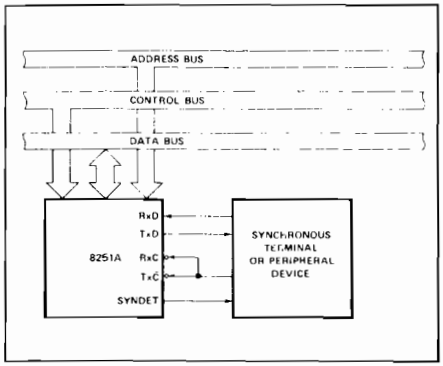


Figure 15. Synchronous Interface to Terminal or Peripheral Device

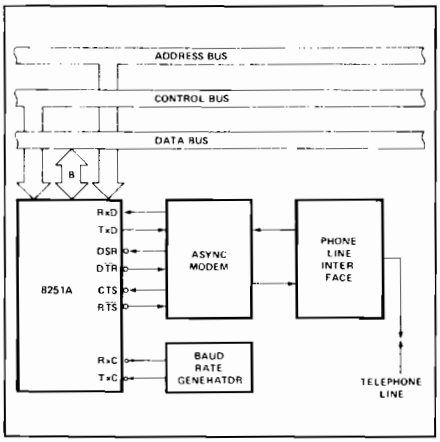


Figure 16. Asynchronous Interface to Telephone Lines

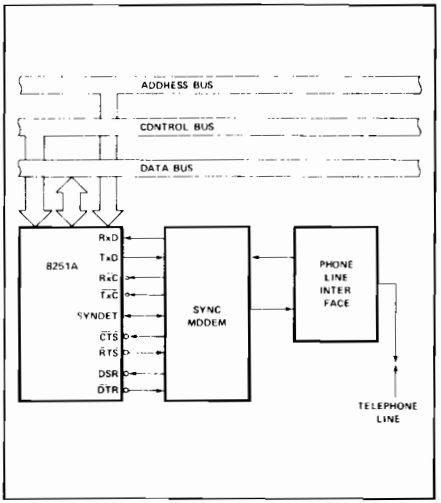


Figure 17. Synchronous Interface to Telephone Lines

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... −65°C to +150°C
Voltage On Any Pin
With Respect To Ground ..... −0.5V to +7V
Power Dissipation ..... 1 Watt

NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5.0V ±10%, GND = 0V)*

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OL} = −400 μA
I_{OFL}	Output Float Leakage		±10	μA	V_{OUT} = V_{CC} TO 0.45V
I_{IL}	Input Leakage		±10	μA	V_{IN} = V_{CC} TO 0.45V
I_{CC}	Power Supply Current		100	mA	All Outputs = High

CAPACITANCE (T_A = 25°C, V_{CC} = GND = 0V)

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance		10	pF	fc = 1MHz
$C_{I/O}$	I/O Capacitance		20	pF	Unmeasured pins returned to GND

A.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5.0V ±10%, GND = 0V)*

Bus Parameters (Note 1)

READ CYCLE

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{AR}	Address Stable Before $\overline{READ}$ ($\overline{CS}$, C/$\overline{D}$)	0		ns	Note 2
t_{RA}	Address Hold Time for $\overline{READ}$ ($\overline{CS}$, C/$\overline{D}$)	0		ns	Note 2
t_{RR}	$\overline{READ}$ Pulse Width	250		ns	
t_{RD}	Data Delay from $\overline{READ}$		200	ns	3, C_L = 150 pF
t_{DF}	$\overline{READ}$ to Data Floating	10	100	ns	

WRITE CYCLE

Symbol	Parameter	Min.	Max.	Unit	Test Condtions
t_{AW}	Address Stable Before $\overline{WRITE}$	0		ns	
t_{WA}	Address Hold Time for $\overline{WRITE}$	0		ns	
t_{WW}	$\overline{WRITE}$ Pulse Width	250		ns	
t_{DW}	Data Set-Up Time for $\overline{WRITE}$	150		ns	
t_{WD}	Data Hold Time for $\overline{WRITE}$	20		ns	
t_{RV}	Recovery Time Between WRITES	6		t_{CY}	Note 4

A.C. CHARACTERISTICS (Continued)

OTHER TIMINGS

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
t_{CY}	Clock Period	320	1350	ns	Notes 5, 6
t_{ϕ}	Clock High Pulse Width	120	t_{CY} 90	ns	
$t_{\bar{\phi}}$	Clock Low Pulse Width	90		ns	
t_R, t_F	Clock Rise and Fall Time		20	ns	
t_{DTx}	TxD Delay from Falling Edge of $\overline{TxC}$		1	μs	
f_{Tx}	Transmitter Input Clock Frequency 1x Baud Rate 16x Baud Rate 64x Baud Rate	 DC DC DC	 64 310 615	 kHz kHz kHz	
t_{TPW}	Transmitter Input Clock Pulse Width 1x Baud Rate 16x and 64x Baud Rate	 12 1		 t_{CY} t_{CY}	
t_{TPD}	Transmitter Input Clock Pulse Delay 1x Baud Rate 16x and 64x Baud Rate	 15 3		 t_{CY} t_{CY}	
f_{Rx}	Receiver Input Clock Frequency 1x Baud Rate 16x Baud Rate 64x Baud Rate	 DC DC DC	 64 310 615	 kHz kHz kHz	
t_{RPW}	Receiver Input Clock Pulse Width 1x Baud Rate 16x and 64x Baud Rate	 12 1		 t_{CY} t_{CY}	
t_{RPD}	Receiver Input Clock Pulse Delay 1x Baud Rate 16x and 64x Baud Rate	 15 3		 t_{CY} t_{CY}	
t_{TxRDY}	TxRDY Pin Delay from Center of Last Bit		8	t_{CY}	Note 7
$t_{TxRDY\ CLEAR}$	TxRDY ↓ from Leading Edge of $\overline{WR}$		400	ns	Note 7
t_{RxRDY}	RxRDY Pin Delay from Center of Last Bit		26	t_{CY}	Note 7
$t_{RxRDY\ CLEAR}$	RxRDY ↓ from Leading Edge of $\overline{RD}$		400	ns	Note 7
t_{IS}	Internal SYNDET Delay from Rising Edge of $\overline{RxC}$		26	t_{CY}	Note 7
t_{ES}	External SYNDET Set-Up Time After Rising Edge of $\overline{RxC}$	18		t_{CY}	Note 7
$t_{TxEMPTY}$	TxEMPTY Delay from Center of Last Bit	20		t_{CY}	Note 7
t_{WC}	Control Delay from Rising Edge of WRITE (TxEn, $\overline{DTR}$, $\overline{RTS}$)	8		t_{CY}	Note 7
t_{CR}	Control to READ Set-Up Time ($\overline{DSR}$, $\overline{CTS}$)	20		t_{CY}	Note 7

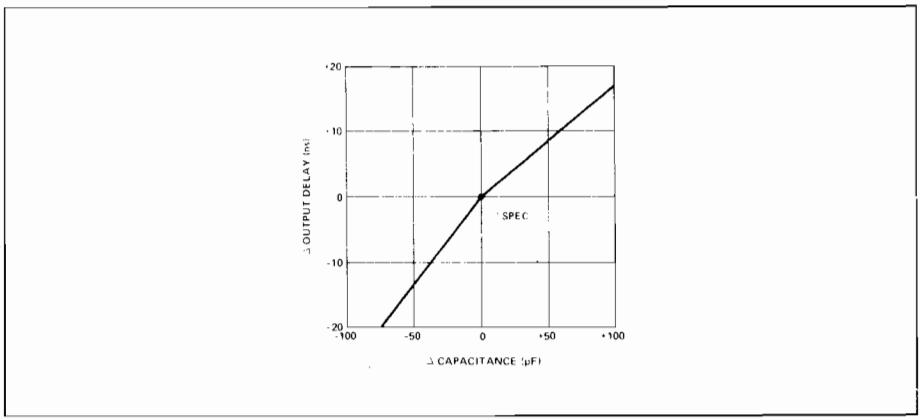
***NOTE:**
1. For Extended Temperature EXPRESS, use M8251A electrical parameters

A

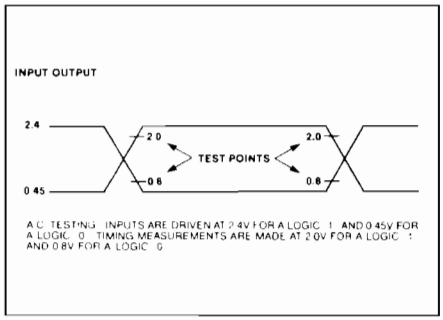
A.C. CHARACTERISTICS (Continued)

NOTES:
1. AC timings measured V_{OH} = 2.0 V_{OL} = 2.0, V_{OL} = 0.8, and with load circuit of Figure 1
2. Chip Select (CS) and Command/Data (C/D) are considered as Addresses.
3. Assumes that Address is valid before $R_D\downarrow$.
4. This recovery time is for Mode Initialization only. Write Data is allowed only when TxRDY = 1. Recovery Time between Writes for Asynchronous Mode is 8 t_{CY} and for Synchronous Mode is 16 t_{CY}.
5. The TxC and RxC frequencies have the following limitations with respect to CLK: For 1x Baud Rate, f_{Tx} or f_{Rx} = 1/(30 t_{CY}).
   For 16x and 64x Baud Rate, f_{Tx} or f_{Rx} = 1/(4.5 t_{CY}).
6. Reset Pulse Width = 6 t_{CY} minimum; System Clock must be running during Reset.
7. Status update can have a maximum delay of 28 clock periods from the event affecting the status.

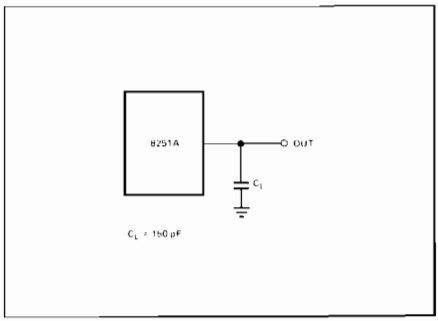
TYPICAL Δ OUTPUT DELAY VS. Δ CAPACITANCE (pF)



A.C. TESTING INPUT, OUTPUT WAVEFORM

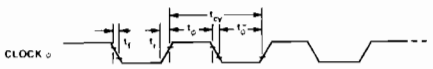


A.C. TESTING LOAD CIRCUIT

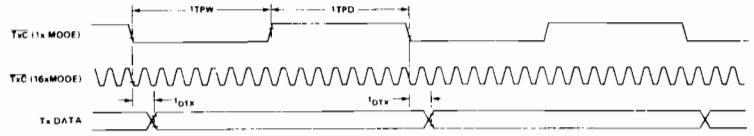


WAVEFORMS

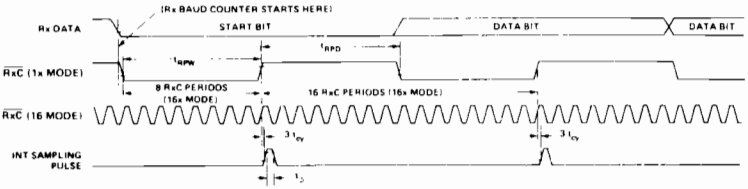
SYSTEM CLOCK INPUT



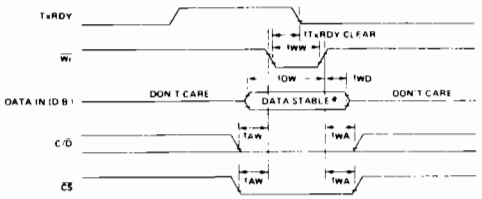
TRANSMITTER CLOCK AND DATA



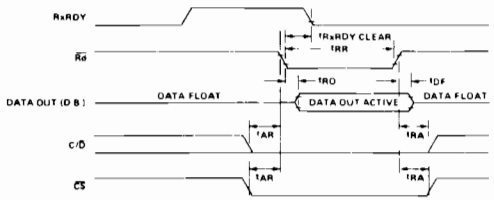
RECEIVER CLOCK AND DATA



WRITE DATA CYCLE (CPU → USART)



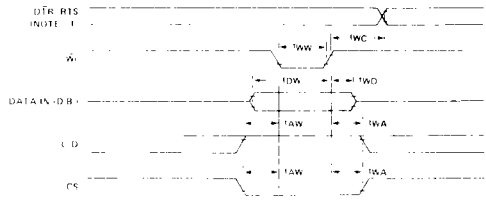
READ DATA CYCLE (CPU ← USART)



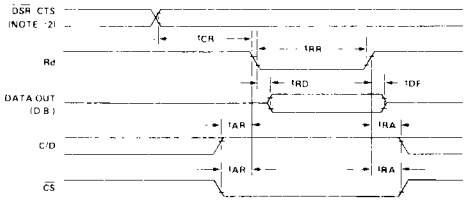
A

WAVEFORMS (Continued)

WRITE CONTROL OR OUTPUT PORT CYCLE (CPU → USART)

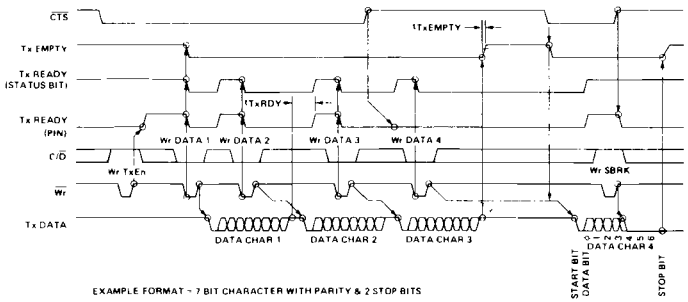


READ CONTROL OR INPUT PORT (CPU ← USART)



NOTE #1 T_{WC} INCLUDES THE RESPONSE TIMING OF A CONTROL BYTE
NOTE #2 T_{CR} INCLUDES THE EFFECT OF CTS ON THE TxENBL CIRCUITRY

TRANSMITTER CONTROL AND FLAG TIMING (ASYNC MODE)

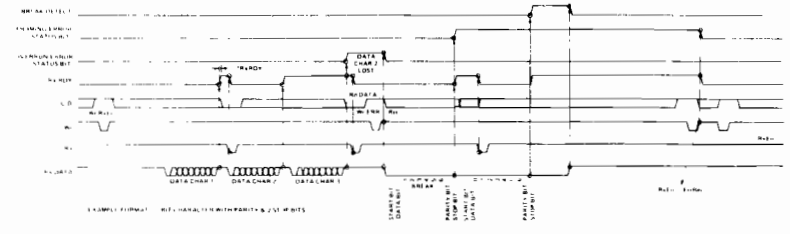


EXAMPLE FORMAT – 7 BIT CHARACTER WITH PARITY & 2 STOP BITS

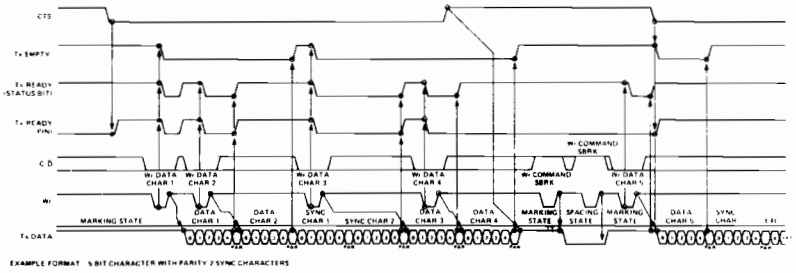
AFN-01573D

WAVEFORMS (Continued)

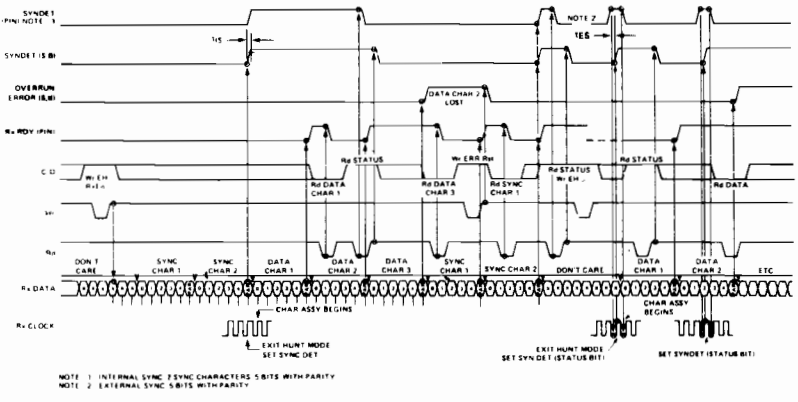
RECEIVER CONTROL AND FLAG TIMING (ASYNC MODE)



TRANSMITTER CONTROL AND FLAG TIMING (SYNC MODE)



RECEIVER CONTROL AND FLAG TIMING (SYNC MODE)



8253/8253-5
PROGRAMMABLE INTERVAL TIMER

A

- MCS-85™ Compatible 8253-5
- 3 Independent 16-Bit Counters
- DC to 2 MHz
- Programmable Counter Modes
- Count Binary or BCD
- Single +5V Supply
- Available in EXPRESS
  - —Standard Temperature Range
  - —Extended Temperature Range

The Intel® 8253 is a programmable counter/timer chip designed for use as an Intel microcomputer peripheral. It uses nMOS technology with a single +5V supply and is packaged in a 24-pin plastic DIP.

It is organized as 3 independent 16-bit counters, each with a count rate of up to 2 MHz. All modes of operation are software programmable.

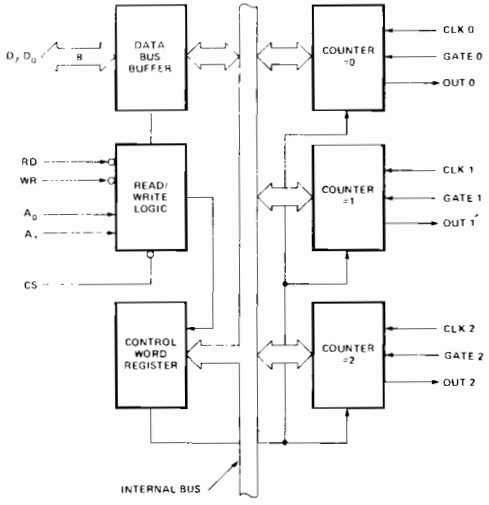


Figure 1. Block Diagram

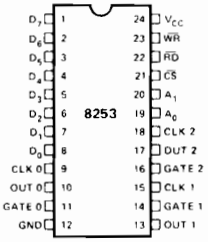


Figure 2. Pin Configuration

AFN-00745C

FUNCTIONAL DESCRIPTION

General

The 8253 is a programmable interval timer/counter specifically designed for use with the Intel™ Microcomputer systems. Its function is that of a general purpose, multi-timing element that can be treated as an array of I/O ports in the system software.

The 8253 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in systems software, the programmer configures the 8253 to match his requirements, initializes one of the counters of the 8253 with the desired quantity, then upon command the 8253 will count out the delay and interrupt the CPU when it has completed its tasks. It is easy to see that the software overhead is minimal and that multiple delays can easily be maintained by assignment of priority levels.

Other counter/timer functions that are non-delay in nature but also common to most microcomputers can be implemented with the 8253.

- Programmable Rate Generator
- Event Counter
- Binary Rate Multiplier
- Real Time Clock
- Digital One-Shot
- Complex Motor Controller

Data Bus Buffer

This 3-state, bi-directional, 8-bit buffer is used to interface the 8253 to the system data bus. Data is transmitted or received by the buffer upon execution of INput or OUTput CPU instructions. The Data Bus Buffer has three basic functions.

1. Programming the MODES of the 8253.
2. Loading the count registers.
3. Reading the count values.

Read/Write Logic

The Read/Write Logic accepts inputs from the system bus and in turn generates control signals for overall device operation. It is enabled or disabled by CS so that no operation can occur to change the function unless the device has been selected by the system logic.

$\overline{RD}$ (Read)

A "low" on this input informs the 8253 that the CPU is inputting data in the form of a counters value.

$\overline{WR}$ (Write)

A "low" on this input informs the 8253 that the CPU is outputting data in the form of mode information or loading counters.

A0, A1

These inputs are normally connected to the address bus. Their function is to select one of the three counters to be operated on and to address the control word register for mode selection.

$\overline{CS}$ (Chip Select)

A "low" on this input enables the 8253. No reading or writing will occur unless the device is selected. The $\overline{CS}$ input has no effect upon the actual operation of the counters.

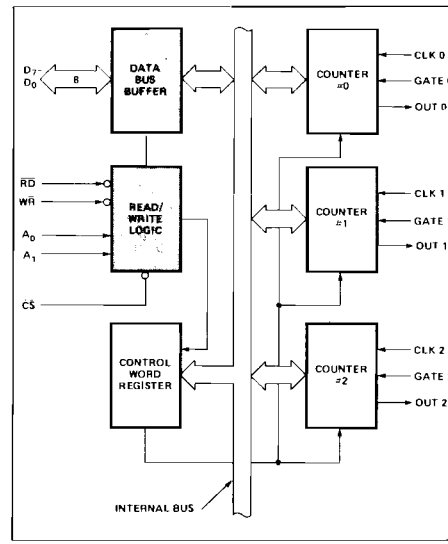


Figure 3. Block Diagram Showing Data Bus Buffer and Read/Write Logic Functions

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	
0	1	0	0	0	Load Counter No. 0
0	1	0	0	1	Load Counter No. 1
0	1	0	1	0	Load Counter No. 2
0	1	0	1	1	Write Mode Word
0	0	1	0	0	Read Counter No. 0
0	0	1	0	1	Read Counter No. 1
0	0	1	1	0	Read Counter No. 2
0	0	1	1	1	No-Operation 3-State
1	X	X	X	X	Disable 3-State
0	1	1	X	X	No-Operation 3-State

Control Word Register

The Control Word Register is selected when A0, A1 are 11. It then accepts information from the data bus buffer and stores it in a register. The information stored in this register controls the operational MODE of each counter, selection of binary or BCD counting and the loading of each count register.

The Control Word Register can only be written into; no read operation of its contents is available.

Counter #0, Counter #1, Counter #2

These three functional blocks are identical in operation so only a single Counter will be described. Each Counter consists of a single, 16-bit, pre-settable, DOWN counter. The counter can operate in either binary or BCD and its input, gate and output are configured by the selection of MODES stored in the Control Word Register.

The counters are fully independent and each can have separate Mode configuration and counting operation, binary or BCD. Also, there are special features in the control word that handle the loading of the count value so that software overhead can be minimized for these functions.

The reading of the contents of each counter is available to the programmer with simple READ operations for event counting applications and special commands and logic are included in the 8253 so that the contents of each counter can be read "on the fly" without having to inhibit the clock input.

8253 SYSTEM INTERFACE

The 8253 is a component of the Intel™ Microcomputer Systems and interfaces in the same manner as all other peripherals of the family. It is treated by the systems software as an array of peripheral I/O ports; three are counters and the fourth is a control register for MODE programming.

Basically, the select inputs A0, A1 connect to the A0, A1 address bus signals of the CPU. The $\overline{CS}$ can be derived directly from the address bus using a linear select method Or it can be connected to the output of a decoder, such as an Intel® 8205 for larger systems.

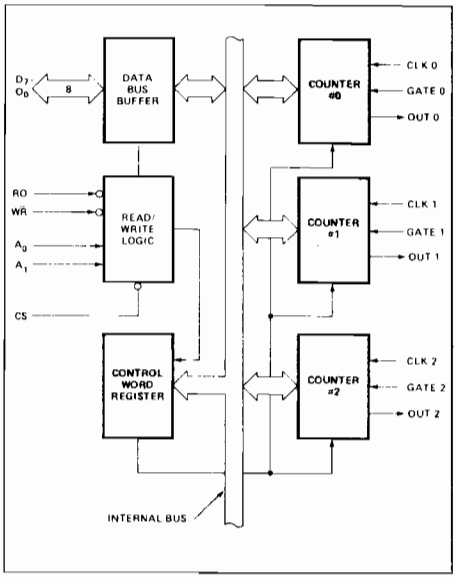


Figure 4. Block Diagram Showing Control Word Register and Counter Functions

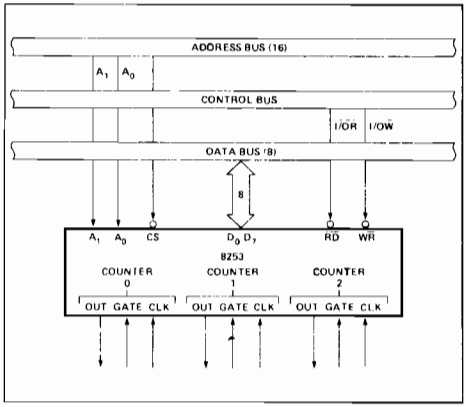


Figure 5. 8253 System Interface

OPERATIONAL DESCRIPTION

General

The complete functional definition of the 8253 is programmed by the systems software. A set of control words must be sent out by the CPU to initialize each counter of the 8253 with the desired MODE and quantity information. Prior to initialization, the MODE, count, and output of all counters is undefined. These control words program the MODE, Loading sequence and selection of binary or BCD counting.

Once programmed, the 8253 is ready to perform whatever timing tasks it is assigned to accomplish.

The actual counting operation of each counter is completely independent and additional logic is provided on-chip so that the usual problems associated with efficient monitoring and management of external, asynchronous events or rates to the microcomputer system have been eliminated.

Programming the 8253

All of the MODES for each counter are programmed by the systems software by simple I/O operations.

Each counter of the 8253 is individually programmed by writing a control word into the Control Word Register (A0, A1 = 11)

Control Word Format

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

Definition of Control

SC — Select Counter:

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Illegal

RL — Read/Load:

RL1	RL0	
0	0	Counter Latching operation (see READ/WRITE Procedure Section)
1	0	Read/Load most significant byte only.
0	1	Read/Load least significant byte only.
1	1	Read/Load least significant byte first, then most significant byte.

M — MODE:

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

BCD:

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

Counter Loading

The count register is not loaded until the count value is written (one or two bytes, depending on the mode selected by the RL bits), followed by a rising edge and a falling edge of the clock. Any read of the counter prior to that falling clock edge may yield invalid data.

MODE Definition

MODE 0: Interrupt on Terminal Count. The output will be initially low after the mode set operation. After the count is loaded into the selected count register, the output will remain low and the counter will count. When terminal count is reached the output will go high and remain high until the selected count register is reloaded with the mode or a new count is loaded. The counter continues to decrement after terminal count has been reached.

Rewriting a counter register during counting results in the following:

(1) Write 1st byte stops the current counting.
(2) Write 2nd byte starts the new count.

MODE 1: Programmable One-Shot. The output will go low on the count following the rising edge of the gate input.

The output will go high on the terminal count. If a new count value is loaded while the output is low it will not affect the duration of the one-shot pulse until the succeeding trigger. The current count can be read at any time without affecting the one-shot pulse.

The one-shot is retriggerable, hence the output will remain low for the full count after any rising edge of the gate input.

MODE 2: Rate Generator. Divide by N counter. The output will be low for one period of the input clock. The period from one output pulse to the next equals the number of input counts in the count register. If the count register is reloaded between output pulses the present period will not be affected, but the subsequent period will reflect the new value.

The gate input, when low, will force the output high. When the gate input goes high, the counter will start from the initial count. Thus, the gate input can be used to synchronize the counter.

When this mode is set, the output will remain high until after the count register is loaded. The output then can also be synchronized by software.

MODE 3: Square Wave Rate Generator. Similar to MODE 2 except that the output will remain high until one half the count has been completed (for even numbers) and go low for the other half of the count. This is accomplished by decrementing the counter by two on the falling edge of each clock pulse. When the counter reaches terminal count, the state of the output is changed and the counter is reloaded with the full count and the whole process is repeated.

If the count is odd and the output is high, the first clock pulse (after the count is loaded) decrements the count by 1. Subsequent clock pulses decrement the clock by 2. After timeout, the output goes low and the full count is reloaded. The first clock pulse (following the reload) decrements the counter by 3. Subsequent clock pulses decrement the count by 2 until timeout. Then the whole process is repeated. In this way, if the count is odd, the output will be high for $(N+1)/2$ counts and low for $(N-1)/2$ counts.

MODE 4: Software Triggered Strobe. After the mode is set, the output will be high. When the count is loaded, the counter will begin counting. On terminal count, the output will go low for one input clock period, then will go high again.

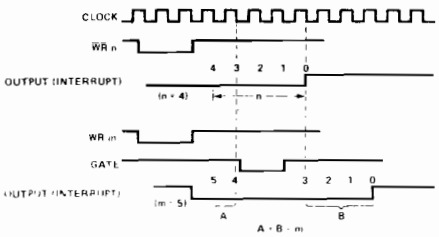
If the count register is reloaded during counting, the new count will be loaded on the next CLK pulse. The count will be inhibited while the GATE input is low.

MODE 5: Hardware Triggered Strobe. The counter will start counting after the rising edge of the trigger input and will go low for one clock period when the terminal count is reached. The counter is retriggerable. The output will not go low until the full count after the rising edge of any trigger.

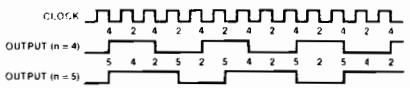
Modes \ Signal Status	Low Or Going Low	Rising	High
0	Disables counting	— —	Enables counting
1	— —	1) Initiates counting 2) Resets output after next clock	— —
2	1) Disables counting 2) Sets output immediately high	**1) Reloads counter** **2) Initiates counting**	Enables counting
3	1) Disables counting 2) Sets output immediately high	Initiates counting	Enables counting
4	Disables counting	— —	Enables counting
5	— —	Initiates counting	— —

Figure 6. Gate Pin Operations Summary

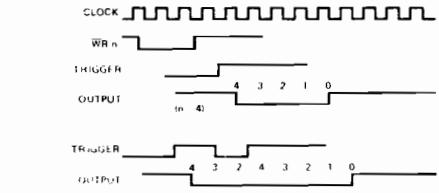
MODE 0: Interrupt on Terminal Count



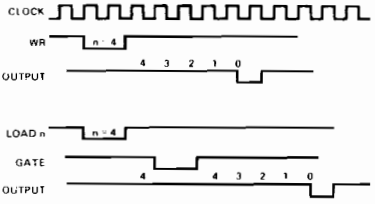
MODE 3: Square Wave Generator



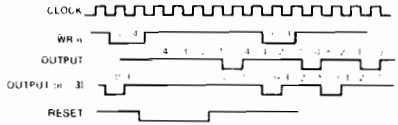
MODE 1: Programmable One-Shot



MODE 4: Software Triggered Strobe



MODE 2: Rate Generator



MODE 5: Hardware Triggered Strobe

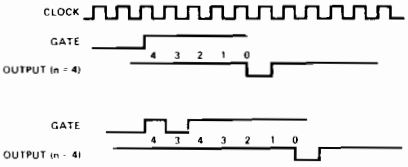


Figure 7. 8253 Timing Diagrams

8253 READ/WRITE PROCEDURE

Write Operations

The systems software must program each counter of the 8253 with the mode and quantity desired. The programmer must write out to the 8253 a MODE control word and the programmed number of count register bytes (1 or 2) prior to actually using the selected counter.

The actual order of the programming is quite flexible. Writing out of the MODE control word can be in any sequence of counter selection, e.g., counter #0 does not have to be first or counter #2 last. Each counter's MODE control word register has a separate address so that its loading is completely sequence independent. (SC0, SC1)

The loading of the Count Register with the actual count value, however, must be done in exactly the sequence programmed in the MODE control word (RL0, RL1). This loading of the counter's count register is still sequence independent like the MODE control word loading, but when a selected count register is to be loaded it must be loaded with the number of bytes programmed in the MODE control word (RL0, RL1). The one or two bytes to be loaded in the count register do not have to follow the associated MODE control word. They can be programmed at any time following the MODE control word loading as long as the correct number of bytes is loaded in order.

All counters are down counters. Thus, the value loaded into the count register will actually be decremented. Loading all zeroes into a count register will result in the maximum count (2^{16} for Binary or 10^4 for BCD). In MODE 0 the new count will not restart until the load has been completed. It will accept one of two bytes depending on how the MODE control words (RL0, RL1) are programmed. Then proceed with the restart operation.

	MODE Control Word Counter n
LSB	Count Register byte Counter n
MSB	Count Register byte Counter n

Note: Format shown is a simple example of loading the 8253 and does not imply that it is the only format that can be used.

Figure 8. Programming Format

			A1	A0
No. 1		MODE Control Word Counter 0	1	1
No. 2		MODE Control Word Counter 1	1	1
No. 3		MODE Control Word Counter 2	1	1
No. 4	LSB	Count Register Byte Counter 1	0	1
No. 5	MSB	Count Register Byte Counter 1	0	1
No. 6	LSB	Count Register Byte Counter 2	1	0
No. 7	MSB	Count Register Byte Counter 2	1	0
No. 8	LSB	Count Register Byte Counter 0	0	0
No. 9	MSB	Count Register Byte Counter 0	0	0

Note: The exclusive addresses of each counter's count register make the task of programming the 8253 a very simple matter, and maximum effective use of the device will result if this feature is fully utilized.

Figure 9. Alternate Programming Formats

Read Operations

In most counter applications it becomes necessary to read the value of the count in progress and make a computational decision based on this quantity. Event counters are probably the most common application that uses this function. The 8253 contains logic that will allow the programmer to easily read the contents of any of the three counters without disturbing the actual count in progress.

There are two methods that the programmer can use to read the value of the counters. The first method involves the use of simple I/O read operations of the selected counter. By controlling the A0, A1 inputs to the 8253 the programmer can select the counter to be read (remember that no read operation of the mode register is allowed A0, A1=11). The only requirement with this method is that in order to assure a stable count reading the actual operation of the selected counter must be inhibited either by controlling the Gate input or by external logic that inhibits the clock input. The contents of the counter selected will be available as follows.

first I/O Read contains the least significant byte (LSB)

second I/O Read contains the most significant byte (MSB).

Due to the internal logic of the 8253 it is absolutely necessary to complete the entire reading procedure. If two bytes are programmed to be read then two bytes must be read before any loading WR command can be sent to the same counter.

Read Operation Chart

A1	A0	RD	
0	0	0	Read Counter No. 0
0	1	0	Read Counter No. 1
1	0	0	Read Counter No. 2
1	1	0	Illegal

Reading While Counting

In order for the programmer to read the contents of any counter without effecting or disturbing the counting operation the 8253 has special internal logic that can be accessed using simple WR commands to the MODE register. Basically, when the programmer wishes to read the contents of a selected counter "on the fly" he loads the MODE register with a special code which latches the present count value into a storage register so that its contents contain an accurate, stable quantity. The programmer then issues a normal read command to the selected counter and the contents of the latched register is available.

MODE Register for Latching Count

A0, A1 = 11

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	0	0	X	X	X	X

SC1,SC0 — specify counter to be latched.

D5,D4 — 00 designates counter latching operation.

X — don't care

The same limitation applies to this mode of reading the counter as the previous method. That is, it is mandatory to complete the entire read operation as programmed. This command has no effect on the counter's mode.

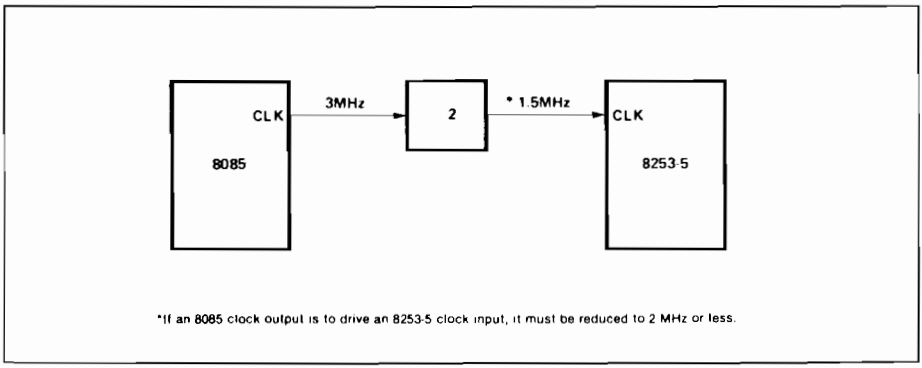


Figure 10. MCS-85™ Clock Interface*

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	−65°C to +150°C
Voltage On Any Pin With Respect to Ground	−0.5V to +7V
Power Dissipation	1 Watt

NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5V ±10%) *

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.2	V_{CC}+.5V	V	
V_{OL}	Output Low Voltage		0.45	V	Note 1
V_{OH}	Output High Voltage	2.4		V	Note 2
I_{IL}	Input Load Current		±10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Float Leakage		±10	μA	V_{OUT} = V_{CC} to .45V
I_{CC}	V_{CC} Supply Current		140	mA	

CAPACITANCE (T_A = 25°C, V_{CC} = GND = 0V)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	fc = 1 MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to V_{SS}

A.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5.0V ± 10%, GND = 0V) *

Bus Parameters (Note 3)

READ CYCLE

Symbol	Parameter	8253 Min.	8253 Max.	8253-5 Min.	8253-5 Max.	Unit
t_{AR}	Address Stable Before $\overline{READ}$	50		30		ns
t_{RA}	Address Hold Time for $\overline{READ}$	5		5		ns
t_{RR}	$\overline{READ}$ Pulse Width	400		300		ns
t_{RD}	Data Delay From $\overline{READ}$ [4]		300		200	ns
t_{DF}	$\overline{READ}$ to Data Floating	25	125	25	100	ns
t_{RV}	Recovery Time Between READ and Any Other Control Signal	1		1		μs

A.C. CHARACTERISTICS (Continued)

WRITE CYCLE

Symbol	Parameter	8253		8253-5		Unit
		Min.	Max.	Min.	Max.	
t_{AW}	Address Stable Before $\overline{WRITE}$	50		30		ns
t_{WA}	Address Hold Time for $\overline{WRITE}$	30		30		ns
t_{WW}	$\overline{WRITE}$ Pulse Width	400		300		ns
t_{DW}	Data Set Up Time for $\overline{WRITE}$	300		250		ns
t_{WD}	Data Hold Time for $\overline{WRITE}$	40		30		ns
t_{RV}	Recovery Time Between $\overline{WRITE}$ and Any Other Control Signal	1		1		μs

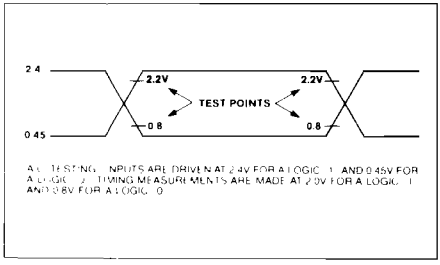
CLOCK AND GATE TIMING

Symbol	Parameter	8253		8253-5		Unit
		Min.	Max.	Min.	Max.	
t_{CLK}	Clock Period	380	dc	380	dc	ns
t_{PWH}	High Pulse Width	230		230		ns
t_{PWL}	Low Pulse Width	150		150		ns
t_{GW}	Gate Width High	150		150		ns
t_{GL}	Gate Width Low	100		100		ns
t_{GS}	Gate Set Up Time to CLK↑	100		100		ns
t_{GH}	Gate Hold Time After CLK↑	50		50		ns
t_{OD}	Output Delay From CLK↓[4]		400		400	ns
t_{ODG}	Output Delay From Gate↓[4]		300		300	ns
t_{WC}	Write to CLK Set Up	450		350		

NOTES:
1. I_{OL} = 2.2 mA.
2. I_{OH} = −400 μA.
3. AC timings measured at V_{OH} 2.2, V_{OL} = 0.8.
4. C_L = 150pF.

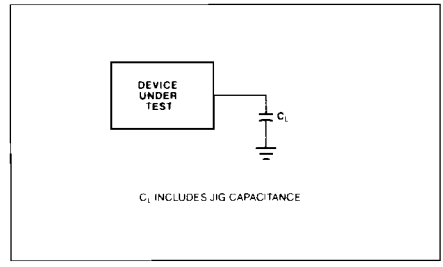
* For Extended Temperature EXPRESS, use M8253 electrical parameters.

A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0".

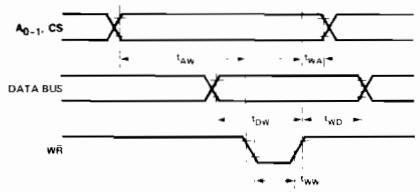
A.C. TESTING LOAD CIRCUIT



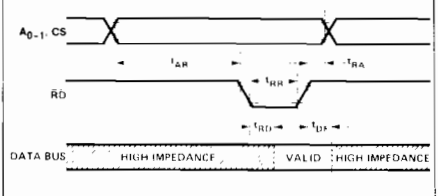
C_L INCLUDES JIG CAPACITANCE

WAVEFORMS

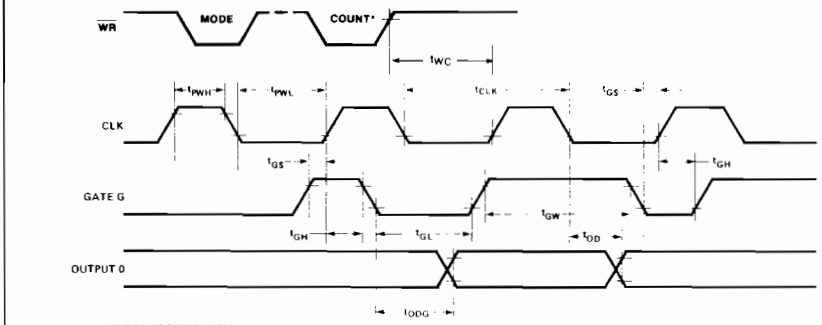
WRITE TIMING



READ TIMING



CLOCK AND GATE TIMING



*LAST BYTE OF COUNT BEING WRITTEN

A

8255A FUNCTIONAL DESCRIPTION

General

The 8255A is a programmable peripheral interface (PPI) device designed for use in Intel® microcomputer systems. Its function is that of a general purpose I/O component to interface peripheral equipment to the microcomputer system bus. The functional configuration of the 8255A is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to interface the 8255A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

($\overline{CS}$)

Chip Select. A "low" on this input pin enables the communiction between the 8255A and the CPU.

($\overline{RD}$)

Read. A "low" on this input pin enables the 8255A to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the 8255A.

($\overline{WR}$)

Write. A "low" on this input pin enables the CPU to write data or control words into the 8255A.

(A_0 and A_1)

Port Select 0 and Port Select 1. These input signals, in conjunction with the RD and WR inputs, control the selection of one of the three ports or the control word registers. They are normally connected to the least significant bits of the address bus (A_0 and A_1).

8255A BASIC OPERATION

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	INPUT OPERATION (READ)
0	0	0	1	0	PORT A → DATA BUS
0	1	0	1	0	PORT B → DATA BUS
1	0	0	1	0	PORT C → DATA BUS
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	DATA BUS → PORT A
0	1	1	0	0	DATA BUS → PORT B
1	0	1	0	0	DATA BUS → PORT C
1	1	1	0	0	DATA BUS → CONTROL
					DISABLE FUNCTION
X	X	X	X	1	DATA BUS → 3-STATE
1	1	0	1	0	ILLEGAL CONDITION
X	X	1	1	0	DATA BUS → 3-STATE

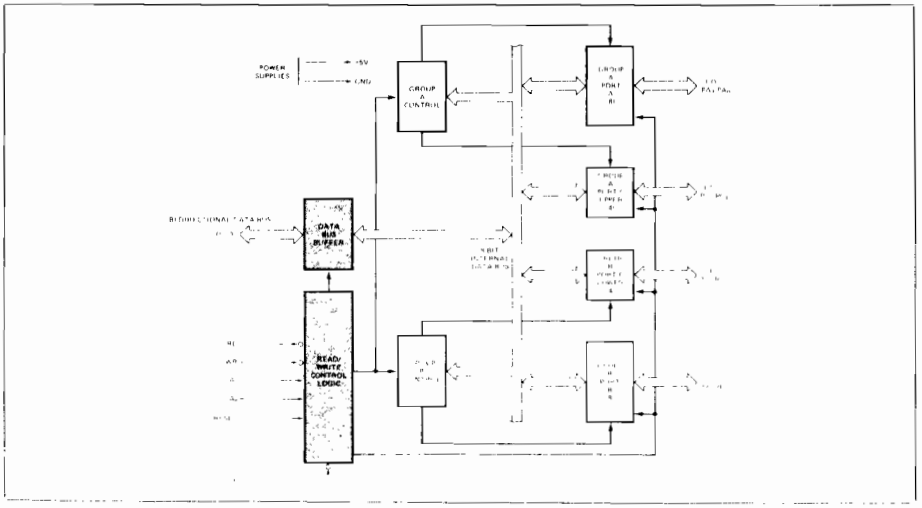


Figure 3. 8255A Block Diagram Showing Data Bus Buffer and Read/Write Control Logic Functions

8255A/8255A-5
PROGRAMMABLE PERIPHERAL INTERFACE

- MCS-85™ Compatible 8255A-5
- 24 Programmable I/O Pins
- Completely TTL Compatible
- Fully Compatible with Intel® Microprocessor Families
- Improved Timing Characteristics
- Direct Bit Set/Reset Capability Easing Control Application Interface
- Reduces System Package Count
- Improved DC Driving Capability
- Available in EXPRESS
  - —Standard Temperature Range
  - —Extended Temperature Range

The Intel® 8255A is a general purpose programmable I/O device designed for use with Intel® microprocessors. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the first mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In MODE 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (MODE 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group, for handshaking.

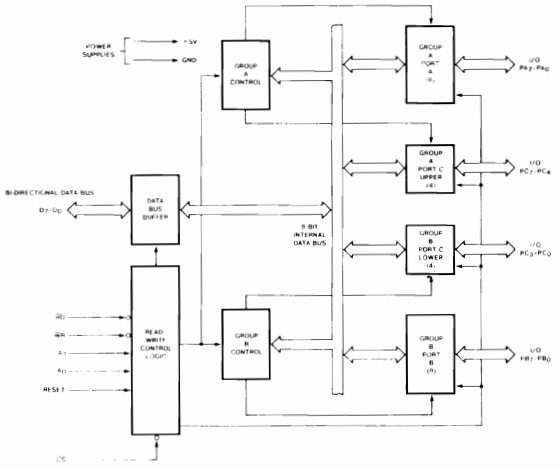


Figure 1. 8255A Block Diagram

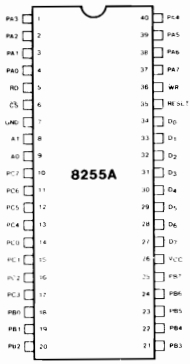


Figure 2. Pin Configuration

AFN-00744C

(RESET)

Reset. A "high" on this input clears the control register and all ports (A, B, C) are set to the input mode.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the 8255A. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the 8255A.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A – Port A and Port C upper (C7-C4)
Control Group B – Port B and Port C lower (C3-C0)

The Control Word Register can Only be written into. No Read operation of the Control Word Register is allowed.

Ports A, B, and C

The 8255A contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 8255A.

Port A. One 8-bit data output latch/buffer and one 8-bit data input latch.

Port B. One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

Port C. One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.

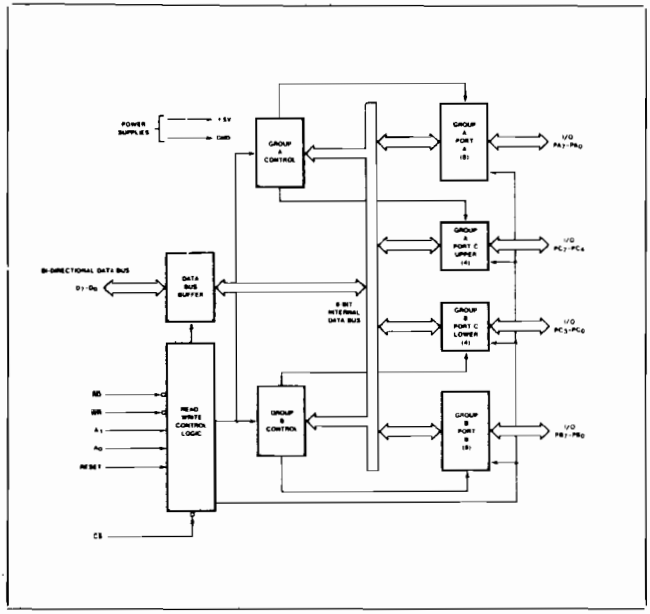
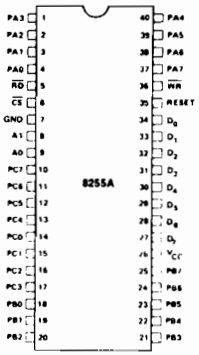


Figure 4. 8225A Block Diagram Showing Group A and Group B Control Functions

PIN CONFIGURATION



PIN NAMES

D_7–D_0	DATA BUS (BI-DIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V_{CC}	+5 VOLTS
GND	0 VOLTS

A

8255A OPERATIONAL DESCRIPTION

Mode Selection

There are three basic modes of operation that can be selected by the system software:

Mode 0 – Basic Input/Output
Mode 1 – Strobed Input/Output
Mode 2 – Bi-Directional Bus

When the reset input goes "high" all ports will be set to the input mode (i.e., all 24 lines will be in the high impedance state). After the reset is removed the 8255A can remain in the input mode with no additional initialization required. During the execution of the system program any of the other modes may be selected using a single output instruction. This allows a single 8255A to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be "tailored" to almost any I/O structure. For instance; Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

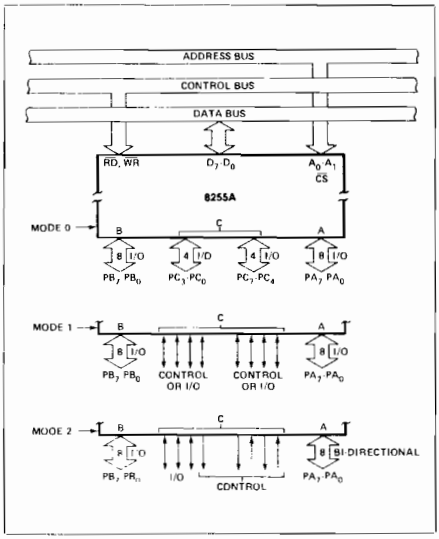


Figure 5. Basic Mode Definitions and Bus Interface

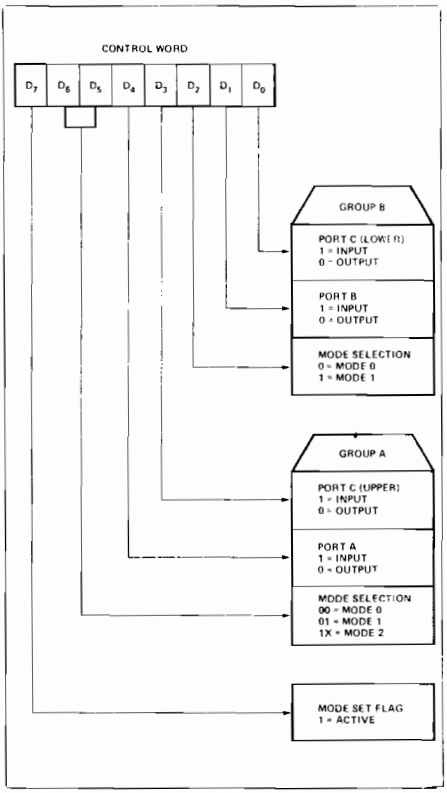


Figure 6. Mode Definition Format

The mode definitions and possible mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 8255A has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUTput instruction. This feature reduces software requirements in Control-based applications.

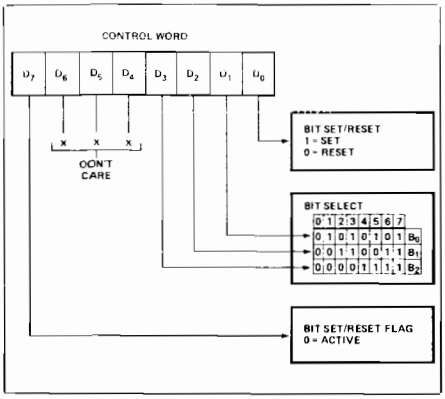


Figure 7. Bit Set/Reset Format

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

Interrupt Control Functions

When the 8255A is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the bit set/reset function of port C.

This function allows the Programmer to disallow or allow a specific I/O device to interrupt the CPU without affecting any other device in the interrupt structure.

INTE flip-flop definition:

(BIT-SET) — INTE is SET — Interrupt enable
(BIT-RESET) — INTE is RESET — Interrupt disable

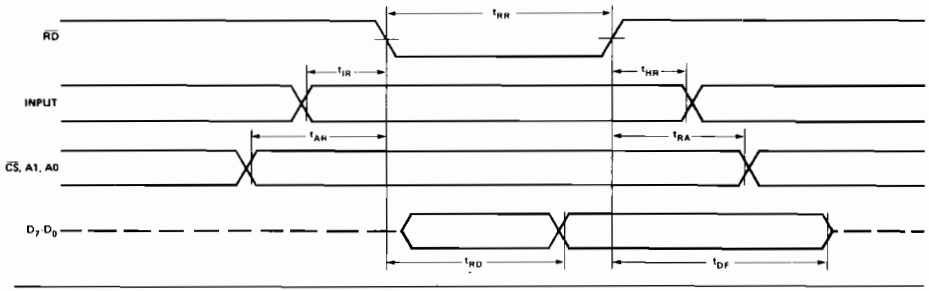
Note: All Mask flip-flops are automatically reset during mode selection and device Reset.

Operating Modes

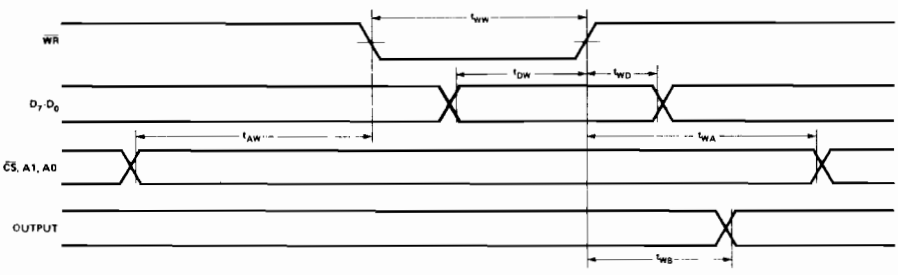
MODE 0 (Basic Input/Output). This functional configuration provides simple input and output operations for each of the three ports. No "handshaking" is required, data is simply written to or read from a specified port.

Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports.
- Any port can be input or output.
- Outputs are latched.
- Inputs are not latched.
- 16 different Input/Output configurations are possible in this Mode.



MODE 0 (Basic Input)

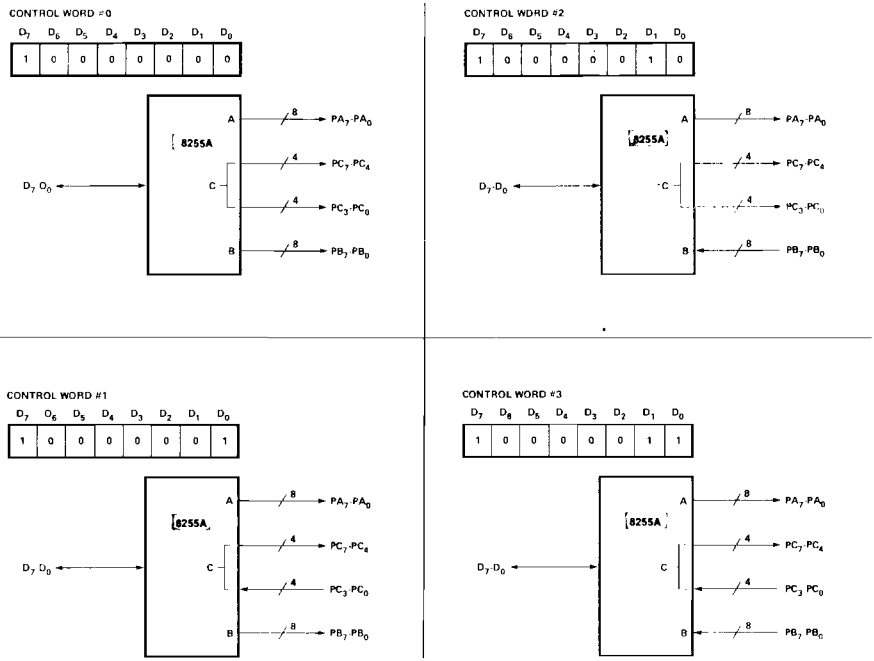


MODE 0 (Basic Output)

MODE 0 Port Definition

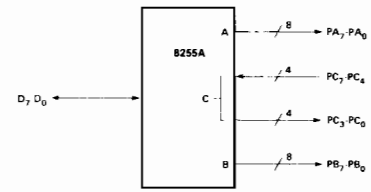
A		B		GROUP A			GROUP B	
D_4	D_3	D_1	D_0	PORT A	PORT C (UPPER)	#	PORT B	PORT C (LOWER)
0	0	0	0	OUTPUT	OUTPUT	0	OUTPUT	OUTPUT
0	0	0	1	OUTPUT	OUTPUT	1	OUTPUT	INPUT
0	0	1	0	OUTPUT	OUTPUT	2	INPUT	OUTPUT
0	0	1	1	OUTPUT	OUTPUT	3	INPUT	INPUT
0	1	0	0	OUTPUT	INPUT	4	OUTPUT	OUTPUT
0	1	0	1	OUTPUT	INPUT	5	OUTPUT	INPUT
0	1	1	0	OUTPUT	INPUT	6	INPUT	OUTPUT
0	1	1	1	OUTPUT	INPUT	7	INPUT	INPUT
1	0	0	0	INPUT	OUTPUT	8	OUTPUT	OUTPUT
1	0	0	1	INPUT	OUTPUT	9	OUTPUT	INPUT
1	0	1	0	INPUT	OUTPUT	10	INPUT	OUTPUT
1	0	1	1	INPUT	OUTPUT	11	INPUT	INPUT
1	1	0	0	INPUT	INPUT	12	OUTPUT	OUTPUT
1	1	0	1	INPUT	INPUT	13	OUTPUT	INPUT
1	1	1	0	INPUT	INPUT	14	INPUT	OUTPUT
1	1	1	1	INPUT	INPUT	15	INPUT	INPUT

MODE 0 Configurations



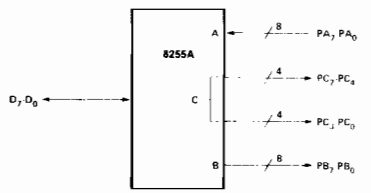
CONTROL WORD #4

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	0	0



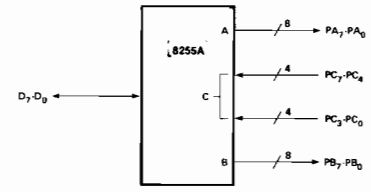
CONTROL WORD #8

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	0	0



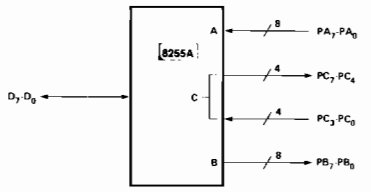
CONTROL WORD #5

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	0	1



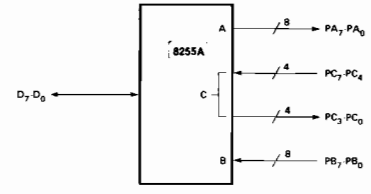
CONTROL WORD #9

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	0	1



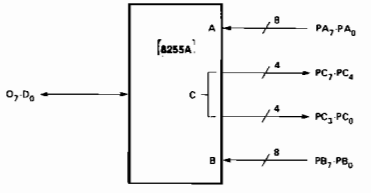
CONTROL WORD #6

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	1	0



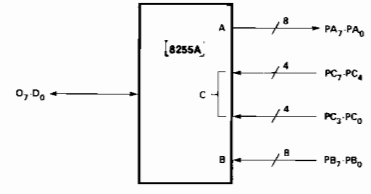
CONTROL WORD #10

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	1	0



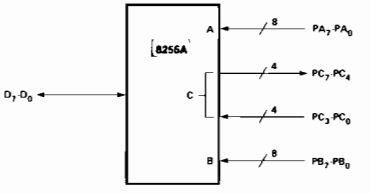
CONTROL WORD #7

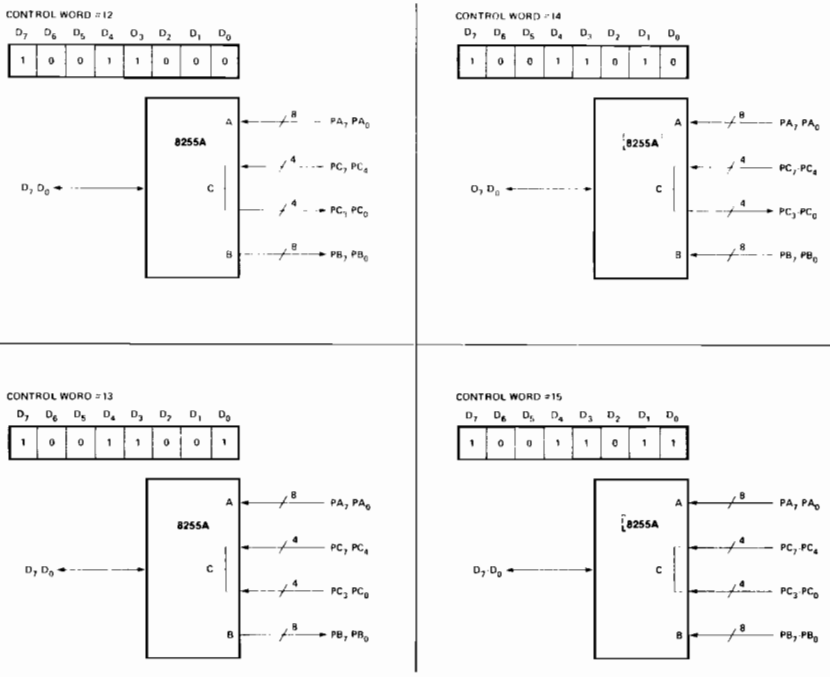
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	1	0	1	1



CONTROL WORD #11

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	1	1





Operating Modes

MODE 1 (Strobed Input/Output). This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In mode 1, port A and Port B use the lines on port C to generate or accept these "handshaking" signals.

Mode 1 Basic Functional Definitions:

- Two Groups (Group A and Group B)
- Each group contains one 8-bit data port and one 4-bit control/data port.
- The 8-bit data port can be either input or output. Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the 8-bit data port.

Input Control Signal Definition

STB (Strobe Input). A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement. IBF is set by STB input being low and is reset by the rising edge of the RD input.

INTR (Interrupt Request)

A "high" on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the $\overline{STB}$ is a "one", IBF is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{RD}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A

Controlled by bit set/reset of PC_4.

INTE B

Controlled by bit set/reset of PC_2.

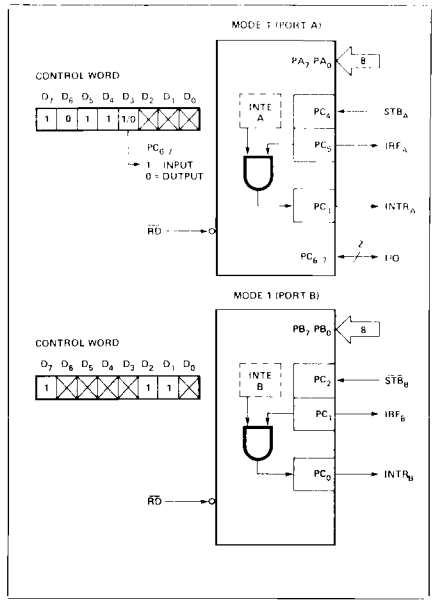


Figure 8. MODE 1 Input

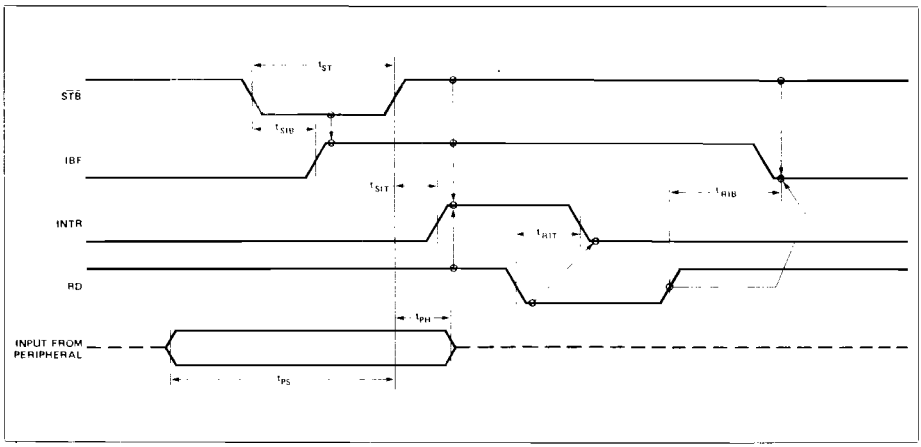


Figure 9. MODE 1 (Strobed Input)

Output Control Signal Definition

$\overline{OBF}$ (Output Buffer Full F/F). The OBF output will go "low" to indicate that the CPU has written data out to the specified port. The OBF F/F will be set by the rising edge of the WR input and reset by ACK Input being low.

$\overline{ACK}$ (Acknowledge Input). A "low" on this input informs the 8255A that the data from port A or port B has been accepted. In essence, a response from the peripheral device indicating that it has received the data output by the CPU.

INTR (Interrupt Request). A "high" on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when ACK is a "one", OBF is a "one" and INTE is a "one". It is reset by the falling edge of WR.

INTE A

Controlled by bit set/reset of PC_6.

INTE B

Controlled by bit set/reset of PC_2.

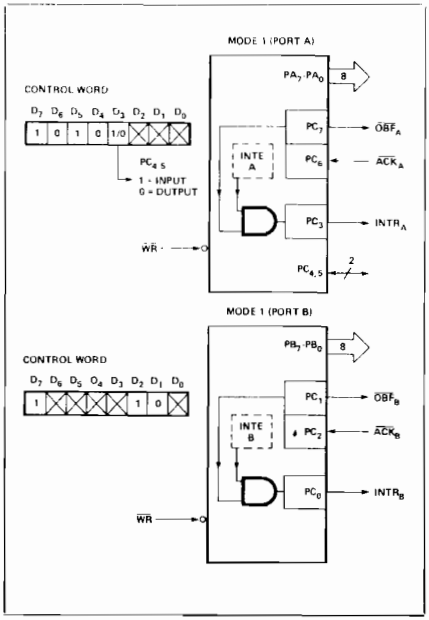


Figure 10. MODE 1 Output

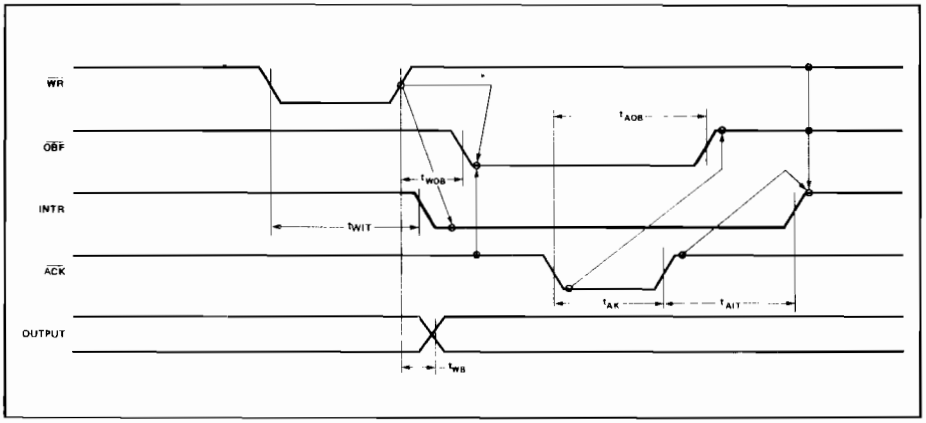


Figure 11. Mode 1 (Strobed Output)

Combinations of MODE 1

Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications.

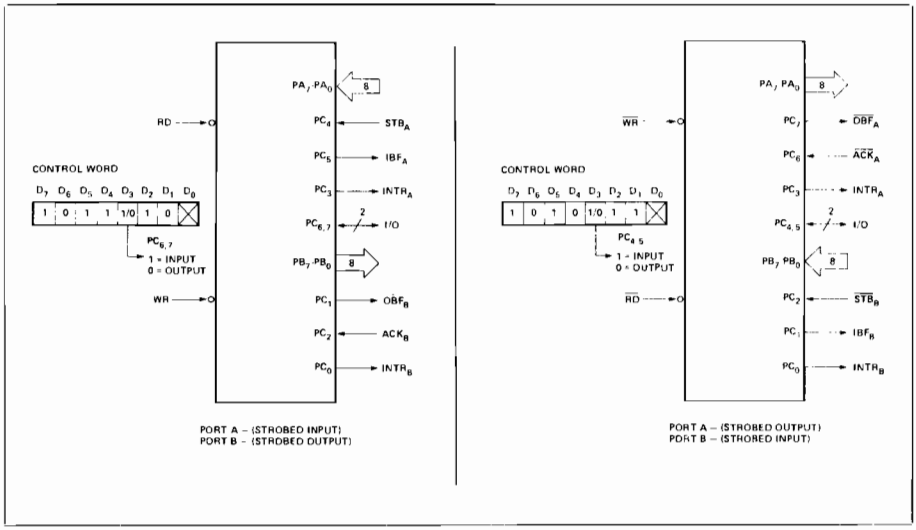


Figure 12. Combinations of MODE 1

Operating Modes

MODE 2 (Strobed Bidirectional Bus I/O). This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus I/O). "Handshaking" signals are provided to maintain proper bus flow discipline in a similar manner to MODE 1. Interrupt generation and enable/disable functions are also available.

MODE 2 Basic Functional Definitions:

- Used in Group A only.
- One 8-bit, bi-directional bus Port (Port A) and a 5-bit control Port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A).

Bidirectional Bus I/O Control Signal Definition

INTR (Interrupt Request). A high on this output can be used to interrupt the CPU for both input or output operations.

Output Operations

$\overline{OBF}$ (Output Buffer Ful). The OBF output will go "low" to indicate that the CPU has written data out to port A.

$\overline{ACK}$ (Acknowledge). A "low" on this input enables the tri-state output buffer of port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

INTE 1 (The INTE Flip-Flop Associated with OBF). Controlled by bit set/reset of PC_6.

Input Operations

$\overline{STB}$ (Strobe Input)

STB (Strobe Input). A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F). A "high" on this output indicates that data has been loaded into the input latch.

INTE 2 (The INTE Flip-Flop Associated with IBF). Controlled by bit set/reset of PC_4.

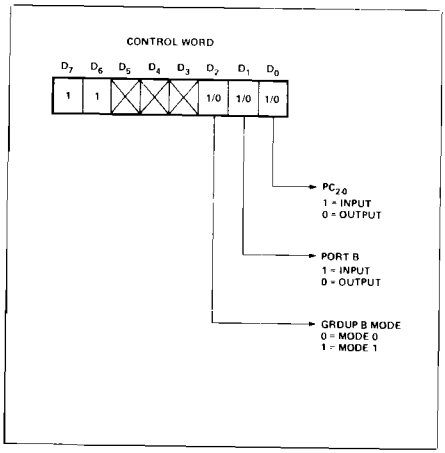


Figure 13. MODE Control Word

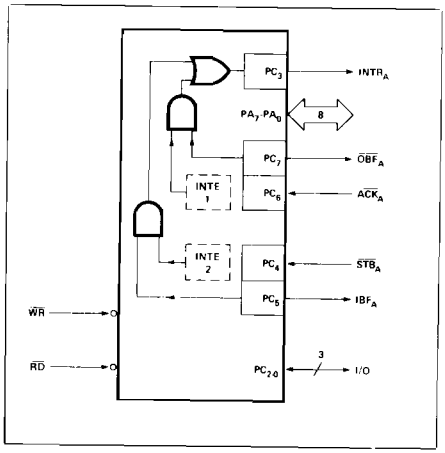


Figure 14. MODE 2

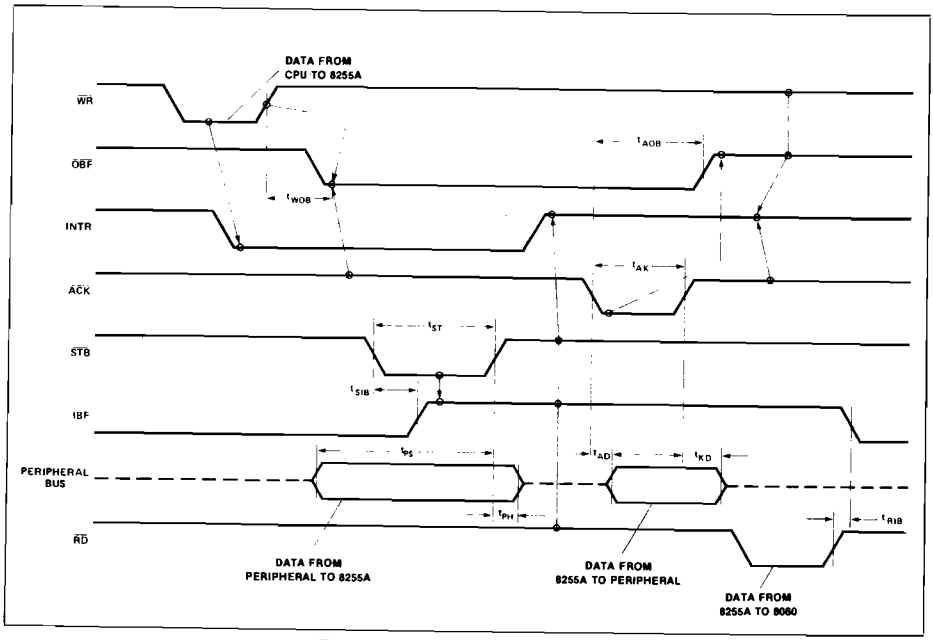


Figure 15. MODE 2 (Bidirectional)

NOTE: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
($INTR = IBF \cdot \overline{MASK} \cdot \overline{STB} \cdot \overline{RD} + \overline{OBF} \cdot \overline{MASK} \cdot \overline{ACK} \cdot \overline{WR}$)

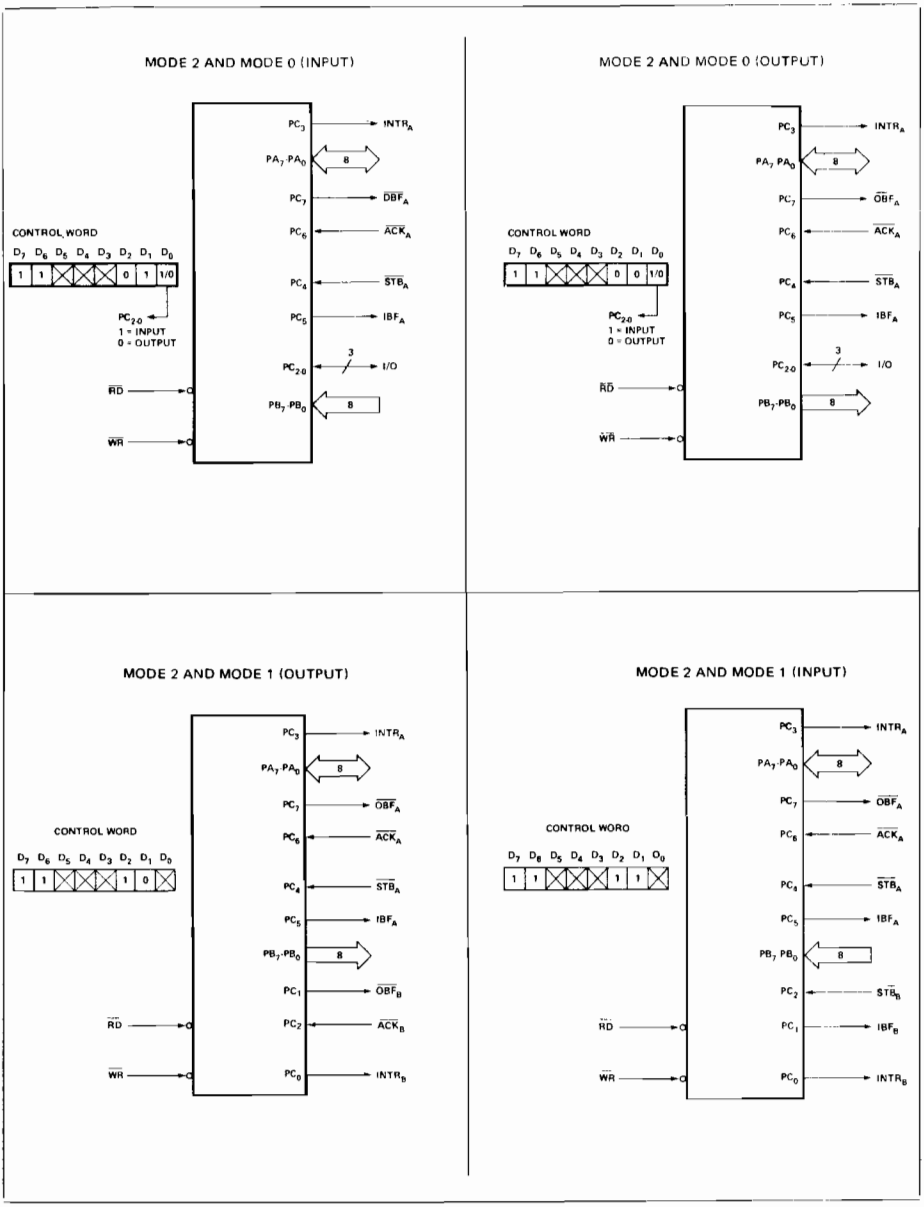


Figure 16. MODE ¼ Combinations

Mode Definition Summary

	MODE 0		MODE 1		MODE 2	
	IN	OUT	IN	OUT	GROUP A ONLY	
PA_0	IN	OUT	IN	OUT	←→	
PA_1	IN	OUT	IN	OUT	←→	
PA_2	IN	OUT	IN	OUT	←→	
PA_3	IN	OUT	IN	OUT	←→	
PA_4	IN	OUT	IN	OUT	←→	
PA_5	IN	OUT	IN	OUT	←→	
PA_6	IN	OUT	IN	OUT	←→	
PA_7	IN	OUT	IN	OUT	←→	
PB_0	IN	OUT	IN	OUT	—	MODE 0 OR MODE 1 ONLY
PB_1	IN	OUT	IN	OUT	—	
PB_2	IN	OUT	IN	OUT	—	
PB_3	IN	OUT	IN	OUT	—	
PB_4	IN	OUT	IN	OUT	—	
PB_5	IN	OUT	IN	OUT	—	
PB_6	IN	OUT	IN	OUT	—	
PB_7	IN	OUT	IN	OUT	—	
PC_0	IN	OUT	$INTR_B$	$INTR_B$	I/O	
PC_1	IN	OUT	IBF_B	$\overline{OBF}_B$	I/O	
PC_2	IN	OUT	$\overline{STB}_B$	$\overline{ACK}_B$	I/O	
PC_3	IN	OUT	$INTR_A$	$INTR_A$	$INTR_A$	
PC_4	IN	OUT	$\overline{STB}_A$	I/O	$\overline{STB}_A$	
PC_5	IN	OUT	IBF_A	I/O	IBF_A	
PC_6	IN	OUT	I/O	$\overline{ACK}_A$	$\overline{ACK}_A$	
PC_7	IN	OUT	I/O	$\overline{OBF}_A$	$\overline{OBF}_A$	

Special Mode Combination Considerations

There are several combinations of modes when not all of the bits in Port C are used for control or status. The remaining bits can be used as follows:

If Programmed as Inputs –
All input lines can be accessed during a normal Port C read.

If Programmed as Outputs –
Bits in C upper (PC_7-PC_4) must be individually accessed using the bit set/reset function.

Bits in C lower (PC_3-PC_0) can be accessed using the bit set/reset function or accessed as a threesome by writing into Port C.

Source Current Capability on Port B and Port C

Any set of eight output buffers, selected randomly from Ports B and C can source 1mA at 1.5 volts. This feature allows the 8255 to directly drive Darlington type drivers and high-voltage displays that require such source current.

Reading Port C Status

In Mode 0, Port C transfers data to or from the peripheral device. When the 8255 is programmed to function in Modes 1 or 2, Port C generates or accepts "hand-shaking" signals with the peripheral device. Reading the contents of Port C allows the programmer to test or verify the "status" of each peripheral device and change the program flow accordingly.

There is no special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.

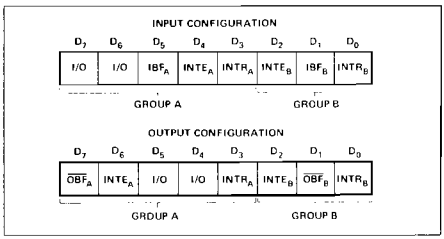


Figure 17. MODE 1 Status Word Format

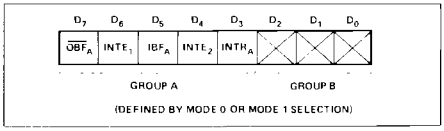


Figure 18. MODE 2 Status Word Format

APPLICATIONS OF THE 8255A

The 8255A is a very powerful tool for interfacing peripheral equipment to the microcomputer system. It represents the optimum use of available pins and is flexible enough to interface almost any I/O device without the need for additional external logic.

Each peripheral device in a microcomputer system usually has a "service routine" associated with it. The routine manages the software interface between the device and the CPU. The functional definition of the 8255A is programmed by the I/O service routine and becomes an extension of the system software. By examining the I/O devices interface characteristics for both data transfer and timing, and matching this information to the examples and tables in the detailed operational description, a control word can easily be developed to initialize the 8255A to exactly "fit" the application. Figures 19 through 25 present a few examples of typical applications of the 8255A.

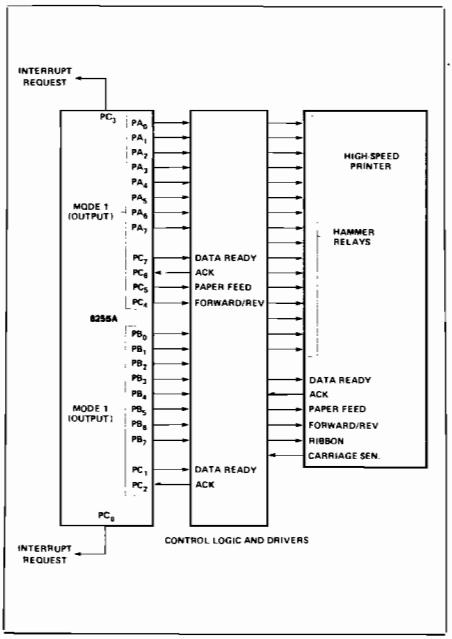


Figure 19. Printer Interface

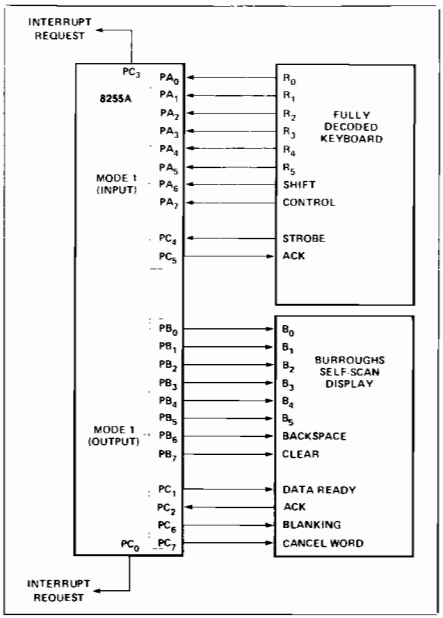


Figure 20. Keyboard and Display Interface

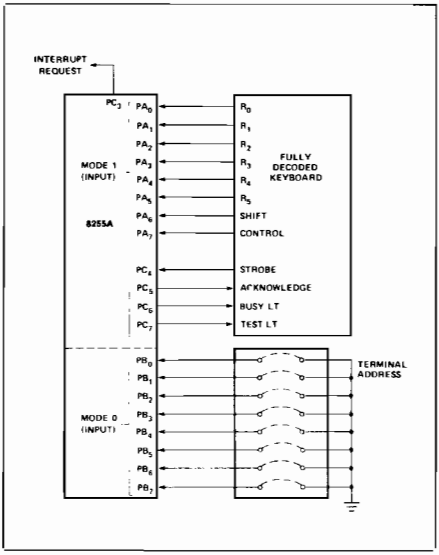


Figure 21. Keyboard and Terminal Address Interface

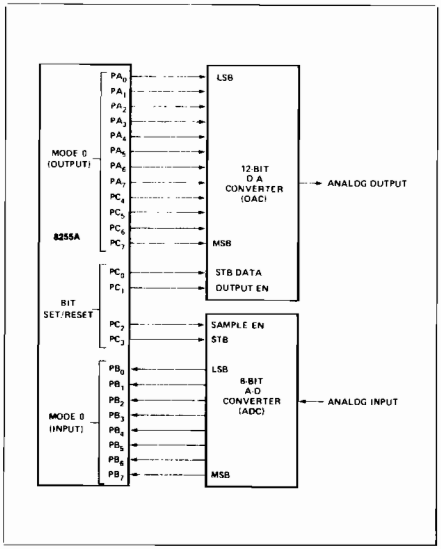


Figure 22. Digital to Analog, Analog to Digital

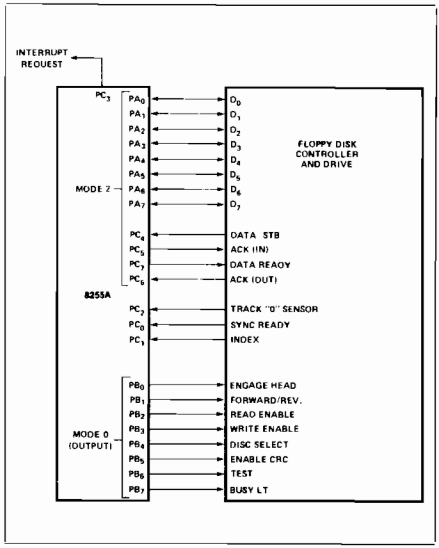


Figure 23. Basic CRT Controller Interface

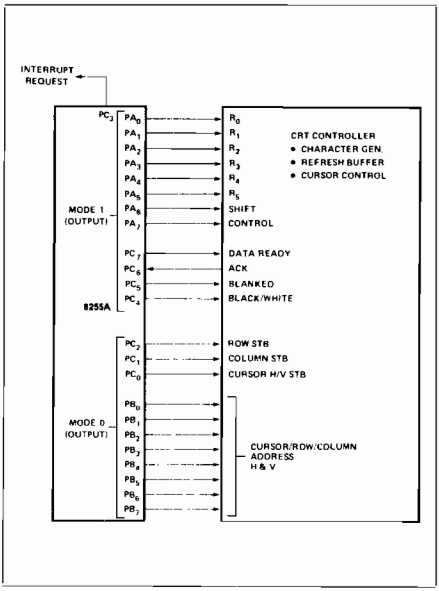


Figure 24. Basic Floppy Disc Interface

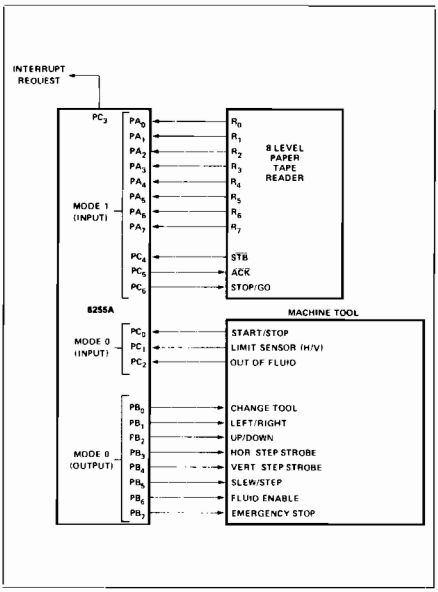


Figure 25. Machine Tool Controller Interface

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias	0°C to 70°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin With Respect to Ground	-0.5V to +7V
Power Dissipation	1 Watt

*NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ±10%, GND = 0V)*

Symbol	Parameter	Min.	Max.	Unit	Test Conditions
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
V_{OL} (DB)	Output Low Voltage (Data Bus)		0.45*	V	I_{OL} = 2.5mA
V_{OL} (PER)	Output Low Voltage (Peripheral Port)		0.45*	V	I_{OL} = 1.7mA
V_{OH} (DB)	Output High Voltage (Data Bus)	2.4		V	I_{OH} = -400μA
V_{OH} (PER)	Output High Voltage (Peripheral Port)	2.4		V	I_{OH} = -200μA
I_{DAR}[1]	Darlington Drive Current	-1.0	-4.0	mA	R_{EXT} = 750Ω; V_{EXT} = 1.5V
I_{CC}	Power Supply Current		120	mA	
I_{IL}	Input Load Current		±10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Float Leakage		±10	μA	V_{OUT} = V_{CC} to .45V

NOTE:
1. Available on any 8 pins from Port B and C.

CAPACITANCE (T_A = 25°C, V_{CC} = GND = 0V)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{IN}	Input Capacitance			10	pF	fc = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND

A.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ±10%, GND = 0V)*

Bus Parameters

READ

Symbol	Parameter	8255A		8255A-5		Unit
		Min.	Max.	Min.	Max.	
t_{AR}	Address Stable Before READ	0		0		ns
t_{RA}	Address Stable After READ	0		0		ns
t_{RR}	READ Pulse Width	300		300		ns
t_{RD}	Data Valid From READ[1]		250		200	ns
t_{DF}	Data Float After READ	10	150	10	100	ns
t_{RV}	Time Between READs and/or WRITEs	850		850		ns

A

A.C. CHARACTERISTICS (Continued)

WRITE

Symbol	Parameter	8255A		8255A-5		Unit
		Min.	Max.	Min.	Max.	
t_{AW}	Address Stable Before WRITE	0		0		ns
t_{WA}	Address Stable After WRITE	20		20		ns
t_{WW}	WRITE Pulse Width	400		300		ns
t_{DW}	Data Valid to WRITE (T.E.)	100		100		ns
t_{WD}	Data Valid After WRITE	30		30		ns

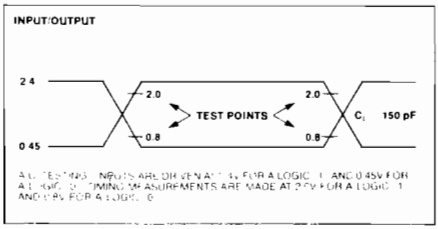
OTHER TIMINGS

Symbol	Parameter	8255A		8255A-5		Unit
		Min.	Max.	Min.	Max.	
t_{WB}	WR = 1 to Output[1]		350		350	ns
t_{IR}	Peripheral Data Before RD	0		0		ns
t_{HR}	Peripheral Data After RD	0		0		ns
t_{AK}	ACK Pulse Width	300		300		ns
t_{ST}	STB Pulse Width	500		500		ns
t_{PS}	Per. Data Before T.E. of STB	0		0		ns
t_{PH}	Per. Data After T.E. of STB	180		180		ns
t_{AD}	ACK = 0 to Output[1]		300		300	ns
t_{KD}	ACK = 1 to Output Float	20	250	20	250	ns
t_{WOB}	WR = 1 to OBF = 0[1]		650		650	ns
t_{AOB}	ACK = 0 to OBF = 1[1]		350		350	ns
t_{SIB}	STB = 0 to IBF = 1[1]		300		300	ns
t_{RIB}	RD = 1 to IBF = 0[1]		300		300	ns
t_{RIT}	RD = 0 to INTR = 0[1]		400		400	ns
t_{SIT}	STB = 1 to INTR = 1[1]		300		300	ns
t_{AIT}	ACK = 1 to INTR = 1[1]		350		350	ns
t_{WIT}	WR = 0 to INTR = 0[1,3]		450		450	ns

NOTES:
1. Test Conditions: C_L = 150 pF.
2. Period of Reset pulse must be at least 50μs during or after power on. Subsequent Reset pulse can be 500 ns min.
3. INTR↑ may occur as early as $\overline{WR}$↓.

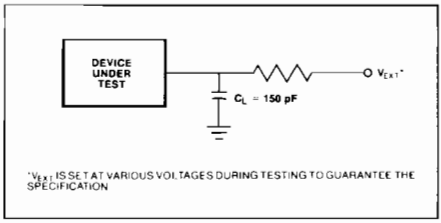
* For Extended Temperature EXPRESS, use M8255A electrical parameters.

A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0". TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0".

A.C. TESTING LOAD CIRCUIT

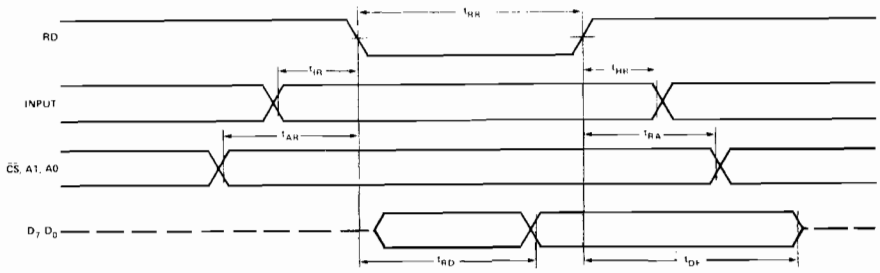


*V_{EXT} IS SET AT VARIOUS VOLTAGES DURING TESTING TO GUARANTEE THE SPECIFICATION

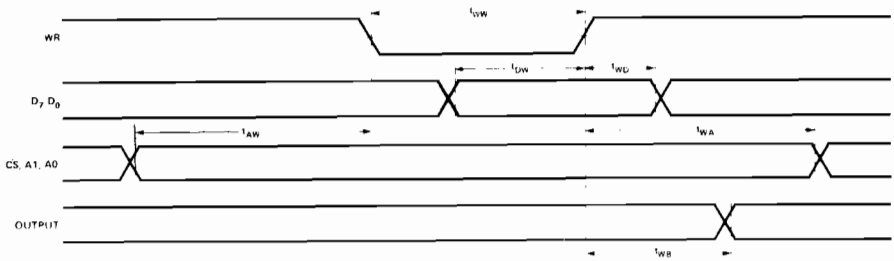
AFN-00744C

WAVEFORMS

MODE 0 (BASIC INPUT)



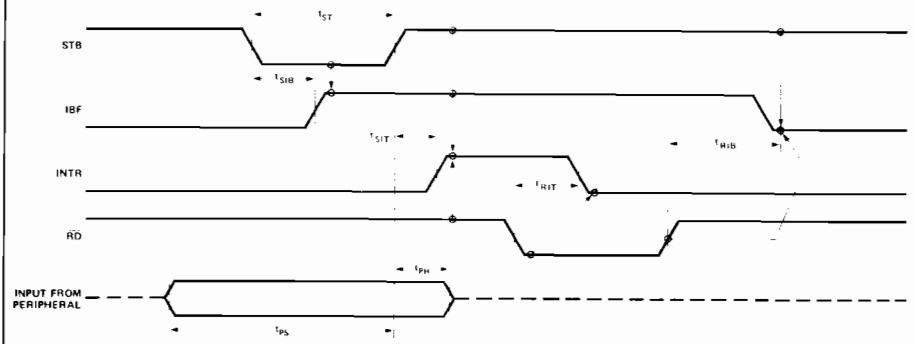
MODE 0 (BASIC OUTPUT)



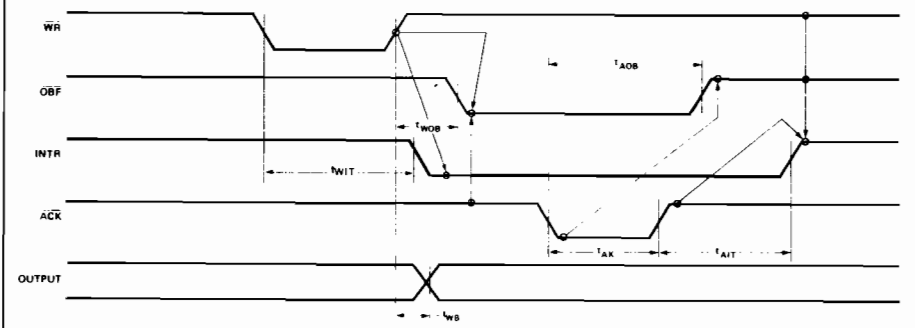
A

WAVEFORMS (Continued)

MODE 1 (STROBED INPUT)

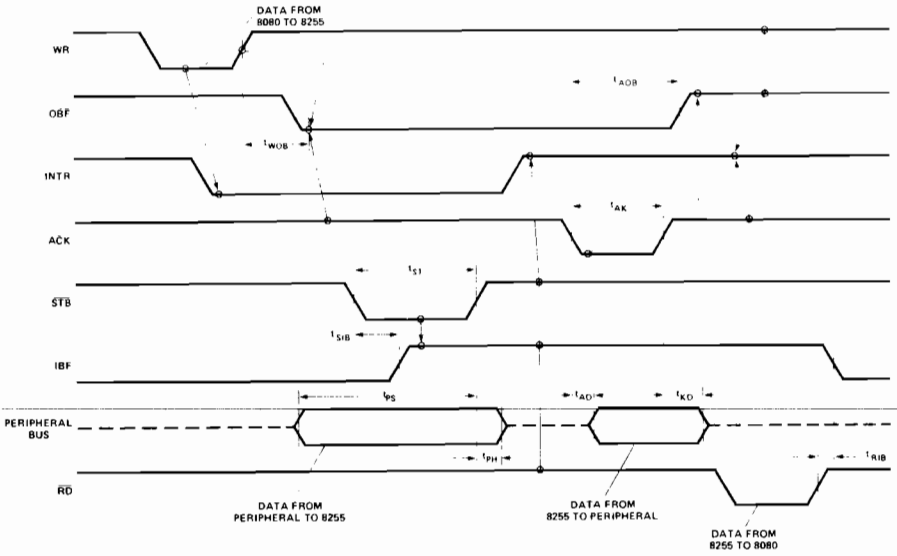


MODE 1 (STROBED OUTPUT)



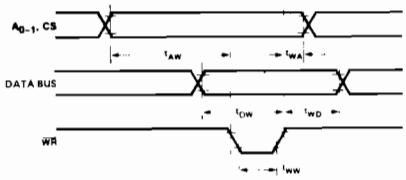
WAVEFORMS (Continued)

MODE 2 (BIDIRECTIONAL)

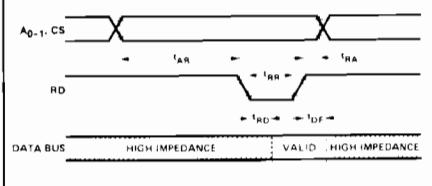


NOTE: Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
(INTR = IBF • $\overline{MASK}$ • $\overline{STB}$ • $\overline{RD}$ + $\overline{OBF}$ • $\overline{MASK}$ • $\overline{ACK}$ • $\overline{WR}$)

WRITE TIMING



READ TIMING



A

PRELIMINARY

8272A
SINGLE/DOUBLE DENSITY FLOPPY DISK CONTROLLER

- **IBM Compatible in Both Single and Double Density Recording Formats**
- **Programmable Data Record Lengths: 128, 256, 512, or 1024 Bytes/Sector**
- **Multi-Sector and Multi-Track Transfer Capability**
- **Drives Up to 4 Floppy or Mini-Floppy Disks**
- **Data Transfers in DMA or Non-DMA Mode**
- **Parallel Seek Operations on Up to Four Drives**
- **Compatible with all Intel and Most Other Microprocessors**
- **Single-Phase 8 MHz Clock**
- **Single +5 Volt Power Supply (±10%)**

The 8272A is an LSI Floppy Disk Controller (FDC) Chip, which contains the circuitry and control functions for interfacing a processor to 4 Floppy Disk Drives. It is capable of supporting either IBM 3740 single density format (FM), or IBM System 34 Double Density format (MFM) including double sided recording. The 8272A provides control signals which simplify the design of an external phase locked loop and write precompensation circuitry. The FDC simplifies and handles most of the burdens associated with implementing a Floppy Disk Drive Interface. The 8272A is a pin-compatible upgrade to the 8272.

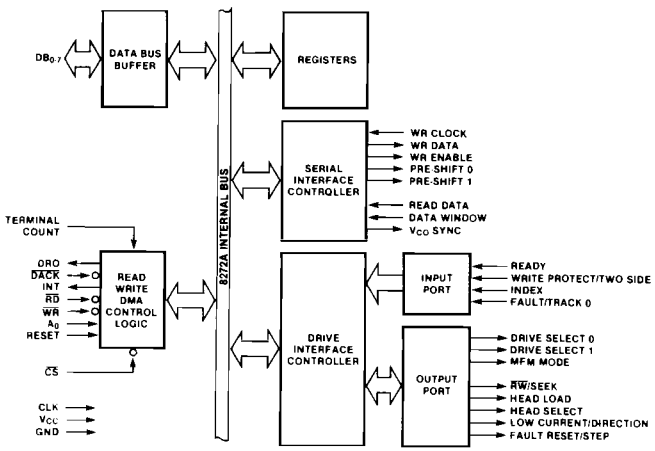


Figure 1. 8272A Internal Block Diagram

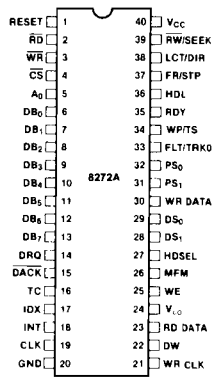


Figure 2. Pin Configuration

ORDER NUMBER 210606-001

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Table 1. Pin Description

Symbol	Pin No.	Type	Connection To	Name and Function
$\overline{RESET}$	1	I	μP	**Reset:** Places FDC in idle state. Resets output lines to FDD to "0" (low). Does not clear the last specify command.
$\overline{RD}$	2	I[1]	μP	**Read:** Control signal for transfer of data from FDC to Data Bus, when "0" (low).
$\overline{WR}$	3	I[1]	μP	**Write:** Control signal for transfer of data to FDC via Data Bus, when "0" (low).
$\overline{CS}$	4	I	μP	**Chip Select:** IC selected when "0" (low), allowing $\overline{RD}$ and $\overline{WR}$ to be enabled.
A_0	5	I[1]	μP	**Data/Status Register Select:** Selects Data Reg (A_0 = 1) or Status Reg (A_0 = 0) contents to be sent to Data Bus.
DB_0-DB_7	6-13	I/O[1]	μP	**Data Bus:** Bidirectional 8-Bit Data Bus.
DRQ	14	O	DMA	**Data DMA Request:** DMA Request is being made by FDC when DRQ "1."
$\overline{DACK}$	15	I	DMA	**DMA Acknowledge:** DMA cycle is active when "0" (low) and Controller is performing DMA transfer.
TC	16	I	DMA	**Terminal Count:** Indicates the termination of a DMA transfer when "1" (high)[2].
IDX	17	I	FDD	**Index:** Indicates the beginning of a disk track.
INT	18	O	μP	**Interrupt:** Interrupt Request Generated by FDC.
CLK	19	I		**Clock:** Single Phase 8 MHz (4 MHz for mini floppies) Squarewave Clock.
GND	20			**Ground:** D C Power Return

Note 1: Disabled when $\overline{CS}$ = 1.
Note 2: TC must be activated to terminate the Execution Phase of any command.

Symbol	Pin No.	Type	Connection To	Name and Function
V_{CC}	40			**D.C. Power:** +5V
$\overline{RW}$/SEEK	39	O	FDD	**Read Write / SEEK:** When "1" (high) Seek mode selected and when "0" (low) Read/Write mode selected.
LCT/DIR	38	O	FDD	**Low Current/Direction:** Lowers Write current on inner tracks in Read/Write mode, determines direction head will step in Seek mode.
FR/STP	37	O	FDD	**Fault Reset/Step:** Resets fault FF in FDD in Read/Write mode, provides step pulses to move head to another cylinder in Seek mode.
HDL	36	O	FDD	**Head Load:** Command which causes read/write head in FDD to contact diskette.
RDY	35	I	FDD	**Ready:** Indicates FDD is ready to send or receive data. Must be tied high (gated by the index pulse) for mini floppies which do not normally have a Ready line.
WP/TS	34	I	FDD	**Write Protect / Two-Side:** Senses Write Protect status in Read/Write mode, and Two Side Media in Seek mode.
FLT/TRK0	33	I	FDD	**Fault/Track 0:** Senses FDD fault condition in Read/Write mode and Track 0 condition in Seek mode.
PS_1,PS_0	31,32	O	FDD	**Precompensation (preshift):** Write precompensation status during MFM mode. Determines early, late, and normal times.
WR DATA	30	O	FDD	**Write Data:** Serial clock and data bits to FDD
DS_1,DS_0	28,29	O	FDD	**Drive Select:** Selects FDD unit
HDSEL	27	O	FDD	**Head Select:** Head 1 selected when "1" (high) Head 0 selected when "0" (low).

Table 1. Pin Description (Continued)

Symbol	Pin No.	Type	Connection To	Name and Function
MFM	26	O	PLL	**MFM Mode:** MFM mode when "1," FM mode when "0."
WE	25	O	FDD	**Write Enable:** Enables write data into FDD.
VCO	24	O	PLL	**VCO Sync:** Inhibits VCO in PLL when "0" (low), enables VCO when "1."
RD DATA	23	I	FDD	**Read Data:** Read data from FDD, containing clock and data bits.
DW	22	I	PLL	**Data Window:** Generated by PLL, and used to sample data from FDD.
WR CLK	21	I		**Write Clock:** Write data rate to FDD FM = 500 kHz, MFM = 1 MHz, with a pulse width of 250 ns for both FM and MFM. Must be enabled for all operations, both Read and Write.

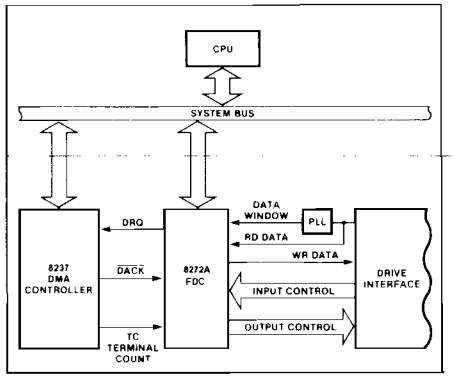


Figure 3. 8272A System Block Diagram

DESCRIPTION

Hand-shaking signals are provided in the 8272A which make DMA operation easy to incorporate with the aid of an external DMA Controller chip, such as the 8237A. The FDC will operate in either DMA or Non-DMA mode. In the Non-DMA mode, the FDC generates interrupts to the processor for every transfer of a data byte between the CPU and the 8272A. In the DMA mode, the processor need only load a command into the FDC and all data transfers occur under control of the 8272A and DMA controller.

There are 15 separate commands which the 8272A will execute. Each of these commands require multiple 8-bit bytes to fully specify the operation which the processor wishes the FDC to perform. The following commands are available.

Read Data	Write Data
Read ID	Format a Track
Read Deleted Data	Write Deleted Data
Read a Track	Seek
Scan Equal	Recalibrate (Restore to Track 0)
Scan High or Equal	Sense Interrupt Status
Scan Low or Equal	Sense Drive Status
Specify	

For more information see the Intel Application Notes AP-116 and AP-121.

FEATURES

Address mark detection circuitry is internal to the FDC which simplifies the phase locked loop and read electronics. The track stepping rate, head load time, and head unload time may be programmed by the user. The 8272A offers many additional features such as multiple sector transfers in both read and write modes with a single command, and full IBM compatibility in both single (FM) and double density (MFM) modes.

8272A ENHANCEMENTS

On the 8272A, after detecting the Index Pulse, the VCO Sync output stays low for a shorter period of time. See Figure 4A.

On the 8272 there can be a problem reading data when Gap 4A is 00 and there is no IAM. This occurs on some older floppy formats. The 8272A cures this problem by adjusting the VCO Sync timing so that it is not low during the data field. See Figure 4B.

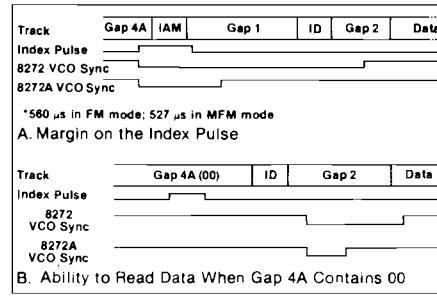


Figure 4. 8272A Enhancements over the 8272

8272A REGISTERS — CPU INTERFACE

The 8272A contains two registers which may be accessed by the main system processor; a Status Register and a Data Register. The 8-bit Main Status Register contains the status information of the FDC, and may be accessed at any time. The 8-bit Data Register (actually consists of several registers in a stack with only one register presented to the data bus at a time), stores data, commands, parameters, and FDD status information. Data bytes are read out of, or written into, the Data Register in order to program or obtain the results after execution of a command. The Status Register may only be read and is used to facilitate the transfer of data between the processor and 8272A.

The relationship between the Status/Data registers and the signals $\overline{RD}$, $\overline{WR}$, and A_0 is shown in Table 2.

Table 2. A_0, $\overline{RD}$, $\overline{WR}$ decoding for the selection of Status/Data register functions.

A_0	$\overline{RD}$	$\overline{WR}$	FUNCTION
0	0	1	Read Main Status Register
0	1	0	Illegal (see note)
0	0	0	Illegal (see note)
1	0	0	Illegal (see note)
1	0	1	Read from Data Register
1	1	1	Write into Data Register

Note: Design must guarantee that the 8272A is not subjected to illegal inputs.

The Main Status Register bits are defined in Table 3.

Table 3. Main Status Register bit description.

BIT NUMBER	NAME	SYMBOL	DESCRIPTION
D_0	FDD 0 Busy	D_0B	FDD number 0 is in the Seek mode.
D_1	FDD 1 Busy	D_1B	FDD number 1 is in the Seek mode.
D_2	FDD 2 Busy	D_2B	FDD number 2 is in the Seek mode.
D_3	FDD 3 Busy	D_3B	FDD number 3 is in the Seek mode.
D_4	FDC Busy	CB	A read or write command is in process.
D_5	Non-DMA mode	NDM	The FDC is in the non-DMA mode. This bit is set only during the execution phase in non-DMA mode. Transition to "0" state indicates execution phase has ended.
D_6	Data Input/Output	DIO	Indicates direction of data transfer between FDC and Data Register. If DIO = "1" then transfer is from Data Register to the Processor. If DIO = "0", then transfer is from the Processor to Data Register.
D_7	Request for Master	RQM	Indicates Data Register is ready to send or receive data to or from the Processor. Both bits DIO and RQM should be used to perform the hand-shaking functions of "ready" and "direction" to the processor.

The DIO and RQM bits in the Status Register indicate when Data is ready and in which direction data will be transferred on the Data Bus.

Note: There is a 12μS or 24μS RQM flag delay when using an 8 or 4 MHz clock respectively.

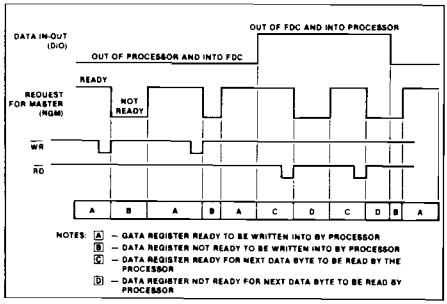


Figure 5. Status Register Timing

The 8272A is capable of executing 15 different commands. Each command is initiated by a multi-byte transfer from the processor, and the result after execution of the command may also be a multi-byte transfer back to the processor. Because of this multi-byte interchange of information between the 8272A and the processor, it is convenient to consider each command as consisting of three phases:

Command Phase: The FDC receives all information required to perform a particular operation from the processor.

Execution Phase: The FDC performs the operation it was instructed to do.

Result Phase: After completion of the operation, status and other housekeeping information are made available to the processor.

During Command or Result Phases the Main Status Register (described in Table 3) must be read by the processor before each byte of information is written into or read from the Data Register. Bits D6 and D7 in the Main Status Register must be in a 0 and 1 state, respectively, before each byte of the command word may be written into the 8272A. Many of the commands require multiple bytes, and as a result the Main Status Register must be read prior to each byte transfer to the 8272A. On the other hand, during the Result Phase, D6 and D7 in the Main Status Register must both be 1's (D6 = 1 and D7 = 1) before reading each byte from the Data Register. Note, this reading of the Main Status Register before each byte transfer to the 8272A is required in only the Command and Result Phases, and NOT during the Execution Phase.

During the Execution Phase, the Main Status Register need not be read. If the 8272A is in the non-DMA Mode, then the receipt of each data byte (if 8272A is reading data from FDD) is indicated by an Interrupt signal on pin 18 (INT = 1). The generation of a Read signal (RD = 0) will reset the Interrupt as well as output the Data onto

the Data Bus. For example, if the processor cannot handle Interrupts fast enough (every 13 μs for MFM mode) then it may poll the Main Status Register and then bit D7 (RQM) functions just like the Interrupt signal. If a Write Command is in process, then the WR signal performs the reset to the Interrupt signal.

The 8272A always operates in a multi-sector transfer mode. It continues to transfer data until the TC input is active. In Non-DMA Mode, the system must supply the TC input.

If the 8272A is in the DMA Mode, no Interrupts are generated during the Execution Phase. The 8272A generates DRQ's (DMA Requests) when each byte of data is available. The DMA Controller responds to this request with both a $\overline{DACK} = 0$ (DMA Acknowledge) and a $\overline{RD} = 0$ (Read signal). When the DMA Acknowledge signal goes low ($\overline{DACK} = 0$) then the DMA Request is reset (DRQ = 0). If a Write Command has been programmed then a $\overline{WR}$ signal will appear instead of $\overline{RD}$. After the Execution Phase has been completed (Terminal Count has occurred) then an Interrupt will occur (INT = 1). This signifies the beginning of the Result Phase. When the first byte of data is read during the Result Phase, the Interrupt is automatically reset (INT = 0).

It is important to note that during the Result Phase all bytes shown in the Command Table must be read. The Read Data Command, for example, has seven bytes of data in the Result Phase. All seven bytes must be read in order to successfully complete the Read Data Command. The 8272A will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the Result Phase.

The 8272A contains five Status Registers. The Main Status Register mentioned above may be read by the processor at any time. The other four Status Registers (ST0, ST1, ST2, and ST3) are only available during the Result Phase, and may be read only after successfully completing a command. The particular command which has been executed determines how many of the Status Registers will be read.

The bytes of data which are sent to the 8272A to form the Command Phase, and are read out of the 8272A in the Result Phase, must occur in the order shown in the Table 4. That is, the Command Code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the Command or Result Phases are allowed. After the last byte of data in the Command Phase is sent to the 8272A, the Execution Phase

Table 4. 8272A Command Set

PHASE	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
READ DATA										
Command	W	MT	MFM	SK	0	0	1	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W				C					Sector ID information prior to Command execution
	W				H					
	W				R					
	W				N					
	W				EOT					
	W				GPL					
	W				DTL					
Execution										Data transfer between the FDD and main-system
Result	R				ST 0					Status information after Command execution
	R				ST 1					
	R				ST 2					
	R				C					Sector ID information after command execution
	R				H					
	R				R					
	R				N					
READ DELETED DATA										
Command	W	MT	MFM	SK	0	1	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W				C					Sector ID information prior to Command execution
	W				H					
	W				R					
	W				N					
	W				EOT					
	W				GPL					
	W				DTL					
Execution										Data transfer between the FDD and main-system
Result	R				ST 0					Status information after Command execution
	R				ST 1					
	R				ST 2					
	R				C					Sector ID information after Command execution
	R				H					
	R				R					
	R				N					

PHASE	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
WRITE DATA										
Command	W	MT	MFM	0	0	0	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W				C					Sector ID information prior to Command execution
	W				H					
	W				R					
	W				N					
	W				EOT					
	W				GPL					
	W				DTL					
Execution										Data transfer between the main-system and FDD
Result	R				ST 0					Status information after Command execution
	R				ST 1					
	R				ST 2					
	R				C					Sector ID information after Command execution
	R				H					
	R				R					
	R				N					
WRITE DELETED DATA										
Command	W	MT	MFM	0	0	1	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W				C					Sector ID information prior to Command execution
	W				H					
	W				R					
	W				N					
	W				EOT					
	W				GPL					
	W				DTL					
Execution										Data transfer between the FDD and main-system
Result	R				ST 0					Status information after Command execution
	R				ST 1					
	R				ST 2					
	R				C					Sector ID information after Command execution
	R				H					
	R				R					
	R				N					

Note 1. Symbols used in this table are described at the end of this section

2. $A_0 = 1$ for all operations.

3. X = Don't care, usually made to equal binary 0.

Table 4. 8272A Command Set (Continued)

PHASE	R/W	DATA BUS D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	REMARKS
READ A TRACK			
Command	W	0 MFM SK 0 0 0 1 0	Command Codes
	W	0 0 0 0 0 HDS DS1 DS0	
	W	C	Sector ID information prior to Command execution
	W	H	
	W	R	
	W	N	
	W	EOT	
	W	GPL	
	W	DTL	
Execution			Data transfer between the FDD and main-system. FDC reads all of cylinders contents from index hole to EOT
Result	R	ST 0	Status information after Command execution
	R	ST 1	
	R	ST 2	
	R	C	Sector ID information after Command execution
	R	H	
	R	R	
	R	N	
READ ID			
Command	W	0 MFM 0 0 1 0 1 0	Commands
	W	0 0 0 0 0 HDS DS1 DS0	
Execution			The first correct ID information on the Cylinder is stored in Data Register
Result	R	ST 0	Status information after Command execution
	R	ST 1	
	R	ST 2	
	R	C	Sector ID information during Execution Phase
	R	H	
	R	R	
	R	N	
FORMAT A TRACK			
Command	W	0 MFM 0 0 1 1 0 1	Command Codes
	W	0 0 0 0 0 HDS DS1 DS0	
	W	N	Bytes/Sector
	W	SC	Sectors/Cylinder
	W	GPL	Gap 3
	W	D	Filler Byte
Execution			FDC formats an entire cylinder
Result	R	ST 0	Status information after Command execution
	R	ST 1	
	R	ST 2	
	R	C	In this case, the ID information has no meaning
	R	H	
	R	R	
	R	N	
SCAN EQUAL			
Command	W	MT MFM SK 1 0 0 0 1	Command Codes
	W	0 0 0 0 0 HDS DS1 DS0	
	W	C	Sector ID information prior to Command execution
	W	H	
	W	R	
	W	N	
	W	EOT	
	W	GPL	
	W	STP	
Execution			Data compared between the FDD and main-system
Result	R	ST 0	Status information after Command execution
	R	ST 1	
	R	ST 2	
	R	C	Sector ID information after Command execution
	R	H	
	R	R	
	R	N	

PHASE	R/W	DATA BUS D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	REMARKS
SCAN LOW OR EQUAL			
Command	W	MT MFM SK 1 1 0 0 1	Command Codes
	W	0 0 0 0 0 HDS DS1 DS0	
	W	C	Sector ID information prior Command execution
	W	H	
	W	R	
	W	N	
	W	EOT	
	W	GPL	
	W	STP	
Execution			Data compared between the FDD and main-system
Result	R	ST 0	Status information after Command execution
	R	ST 1	
	R	ST 2	
	R	C	Sector ID information after Command execution
	R	H	
	R	R	
	R	N	
SCAN HIGH OR EQUAL			
Command	W	MT MFM SK 1 1 1 0 1	Command Codes
	W	0 0 0 0 0 HDS DS1 DS0	
	W	C	Sector ID information prior Command execution
	W	H	
	W	R	
	W	N	
	W	EOT	
	W	GPL	
	W	STP	
Execution			Data compared between the FDD and main-system
Result	R	ST 0	Status information after Command execution
	R	ST 1	
	R	ST 2	
	R	C	Sector ID information after Command execution
	R	H	
	R	R	
	R	N	
RECALIBRATE			
Command	W	0 0 0 0 0 1 1 1	Command Codes
	W	0 0 0 0 0 0 DS1 DS0	
Execution			Head retracted to Track 0
SENSE INTERRUPT STATUS			
Command	W	0 0 0 0 1 0 0 0	Command Codes
Result	R	ST 0	Status information at the end of each seek operation about the FDC
	R	PCN	
SPECIFY			
Command	W	0 0 0 0 0 0 1 1	Command Codes
	W	SRT HUT	
	W	HLT ND	
SENSE DRIVE STATUS			
Command	W	0 0 0 0 0 1 0 0	Command Codes
	W	0 0 0 0 0 HDS DS1 DS0	
Result	R	ST 3	Status information about FDD
SEEK			
Command	W	0 0 0 0 1 1 1 1	Command Codes
	W	0 0 0 0 0 HDS DS1 DS0	
	W	NCN	
Execution			Head is positioned over proper Cylinder on Diskette
INVALID			
Command	W	Invalid Codes	Invalid Command Codes (NoOp — FDC goes into Standby State)
Result	R	ST 0	ST 0 = 80 (16)

Table 5. Command Mneumonics

SYMBOL	NAME	DESCRIPTION
A_0	Address Line 0	A_0 controls selection of Main Status Register (A_0 = 0) or Data Register (A_0 = 1).
C	Cylinder Number	C stands for the current selected Cylinder track number 0 through 76 of the medium.
D	Data	D stands for the data pattern which is going to be written into a Sector.
D_7-D_0	Data Bus	8-bit Data Bus where D_7 is the most significant bit, and D_0 is the least significant bit.
DS0, DS1	Drive Select	DS stands for a selected drive number 0 or 1.
DTL	Data Length	When N is defined as 00, DTL stands for the data length which users are going to read out or write into the Sector.
EOT	End of Track	EOT stands for the final Sector number of a Cylinder.
GPL	Gap Length	GPL stands for the length of Gap 3 (spacing between Sectors excluding VCO Sync Field).
H	Head Address	H stands for head number 0 or 1, as specified in ID field.
HDS	Head Select	HDS stands for a selected head number 0 or 1 (H = HDS in all command words).
HLT	Head Load Time	HLT stands for the head load time in the FDD (2 to 254 ms in 2 ms increments).
HUT	Head Unload Time	HUT stands for the head unload time after a read or write operation has occurred (16 to 240 ms in 16 ms increments).
MFM	FM or MFM Mode	If MF is low, FM mode is selected and if it is high, MFM mode is selected.
MT	Multi-Track	If MT is high, a multi-track operation is to be performed (a cylinder under both HD0 and HD1 will be read or written).
N	Number	N stands for the number of data bytes written in a Sector.
NCN	New Cylinder Number	NCN stands for a new Cylinder number, which is going to be reached as a result of the Seek operation. Desired position of Head.
ND	Non-DMA Mode	ND stands for operation in the Non-DMA Mode.
PCN	Present Cylinder Number	PCN stands for the Cylinder number at the completion of SENSE INTERRUPT STATUS Command. Position of Head at present time.
R	Record	R stands for the Sector number, which will be read or written.
R/W	Read/Write	R/W stands for either Read (R) or Write (W) signal.
SC	Sector	SC indicates the number of Sectors per Cylinder.
SK	Skip	SK stands for Skip Deleted Data Address Mark.
SRT	Step Rate Time	SRT stands for the Stepping Rate for the FDD (1 to 16 ms in 1 ms increments). The same Stepping Rate applies to all drives (F = 1 ms, E = 2 ms, etc.)
ST 0 ST 1 ST 2 ST 3	Status 0 Status 1 Status 2 Status 3	ST 0-3 stand for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by A_0 = 0). ST 0-3 may be read only after a command has been executed and contain information relevant to that particular command.
STP		During a Scan operation, if STP = 1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA), and if STP = 2, then alternate sectors are read and compared.

automatically starts. In a similar fashion, when the last byte of data is read out in the Result Phase, the command is automatically ended and the 8272A is ready for a new command. A command may be aborted by simply sending a Terminal Count signal to pin 16 (TC = 1). This is a convenient means of ensuring that the processor may always get the 8272A's attention even if the disk system hangs up in an abnormal manner.

POLLING FEATURE OF THE 8272A

After power-up RESET, the Drive Select Lines DS0 and DS1 will automatically go into a polling mode. In between commands (and between step pulses in the SEEK command) the 8272A polls all four FDDs looking for a change in the Ready line from any of the drives. If the Ready line changes state (usually due to a door opening or closing) then the 8272A will generate an interrupt. When Status Register 0 (ST0) is read (after Sense Interrupt Status is issued), Not Ready (NR) will be indicated. The polling of the Ready line by the 8272A occurs continuously between instructions, thus notifying the processor which drives are on or off line. Approximate scan timing is shown in Table 6.

Table 6. Scan Timing

DS1	DS0	APPROXIMATE SCAN TIMING
0	0	220μS
0	1	220μS
1	0	220μS
1	1	440μS

COMMAND DESCRIPTIONS

During the Command Phase, the Main Status Register must be polled by the CPU before each byte is written into the Data Register. The DIO (DB6) and RQM (DB7) bits in the Main Status Register must be in the "0" and "1" states respectively, before each byte of the command may be written into the 8272A. The beginning of the execution phase for any of these commands will cause DIO and RQM to switch to "1" and "0" states respectively.

READ DATA

A set of nine (9) byte words are required to place the FDC into the Read Data Mode. After the Read Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify Command), and begins reading ID Address Marks and ID fields. When the current sector number ("R") stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC outputs data (from the data field) byte-by-byte to the main system via the data bus.

After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a "Multi-Sector Read Operation." The Read Data Command must be terminated by the receipt of a Terminal Count signal. Upon receipt of this signal, the FDC stops outputting data to the processor, but will continue to read data from the current sector, check CRC (Cyclic Redundancy Count) bytes, and then at the end of the sector terminate the Read Data Command.

The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track), MFM (MFM/FM), and N (Number of Bytes/Sector). Table 7 on the next page shows the Transfer Capacity.

Table 7. Transfer Capacity

Multi-Track MT	MFM/FM MFM	Bytes/Sector N	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Diskette
0	0	00	(128) (26) = 3,328	26 at Side 0
0	1	01	(256) (26) = 6,656	or 26 at Side 1
1	0	00	(128) (52) = 6,656	26 at Side 1
1	1	01	(256) (52) = 13,312	
0	0	01	(256) (15) = 3,840	15 at Side 0
0	1	02	(512) (15) = 7,680	or 15 at Side 1
1	0	01	(256) (30) = 7,680	15 at Side 1
1	1	02	(512) (30) = 15,380	
0	0	02	(512) (8) = 4,096	8 at Side 0
0	1	03	(1024) (8) = 8,192	or 8 at Side 1
1	0	02	(512) (16) = 8,192	8 at Side 1
1	1	03	(1024) (16) = 16,384	

The "multi-track" function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing at Sector L, Side 1 (Sector L = last sector on the side). Note, this function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, then DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a Sector, the data beyond DTL in the Sector is not sent to the Data Bus. The FDC reads (internally) the complete Sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read Operation. When N is non-zero, then DTL has no meaning and should be set to 0FFH.

At the completion of the Read Data Command, the head is not unloaded until after Head Unload Time Interval (specified in the Specify Command) has elapsed. If the processor issues another command before the head unloads then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another.

If the FDC detects the Index Hole twice without finding the right sector, (indicated in "R"), then the FDC sets the ND (No Data) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC sets the DE (Data Error) flag in Status Register 1 to a 1 (high), and if a CRC error occurs in the Data Field the FDC also sets the DD (Data Error in Data Field) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

If the FDC reads a Deleted Data Address Mark off the diskette, and the SK bit (bit D5 in the first Command Word) is not set (SK = 0), then the FDC sets the CM (Control Mark) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command, after reading all the data in the Sector. If SK = 1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector.

During disk data transfers between the FDC and the processor, via the data bus, the FDC must be serviced by the processor every 27 μs in the FM Mode, and every 13 μs in the MFM Mode, or the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command.

If the processor terminates a read (or write) operation in the FDC, then the ID Information in the Result Phase is dependent upon the state of the MT bit and EOT byte. Table 5 shows the values for C, H, R, and N, when the processor terminates the Command.

Table 8. ID Information When Processor Terminates Command

MT	EOT	Final Sector Transferred to Processor	ID Information at Result Phase			
			C	H	R	N
0	1A	Sector 1 to 25 at Side 0	NC	NC	R + 1	NC
	0F	Sector 1 to 14 at Side 0				
	08	Sector 1 to 7 at Side 0				
	1A	Sector 26 at Side 0	C + 1	NC	R = 01	NC
	0F	Sector 15 at Side 0				
	08	Sector 8 at Side 0				
	1A	Sector 1 to 25 at Side 1	NC	NC	R + 1	NC
	0F	Sector 1 to 14 at Side 1				
	08	Sector 1 to 7 at Side 1				
	1A	Sector 26 at Side 1	C + 1	NC	R = 01	NC
	0F	Sector 15 at Side 1				
	08	Sector 8 at Side 1				
1	1A	Sector 1 to 25 at Side 0	NC	NC	R + 1	NC
	0F	Sector 1 to 14 at Side 0				
	08	Sector 1 to 7 at Side 0				
	1A	Sector 26 at Side 0	NC	LSB	R = 01	NC
	0F	Sector 15 at Side 0				
	08	Sector 8 at Side 0				
	1A	Sector 1 to 25 at Side 1	NC	NC	R + 1	NC
	0F	Sector 1 to 14 at Side 1				
	08	Sector 1 to 7 at Side 1				
	1A	Sector 26 at Side 1	C + 1	LSB	R = 01	NC
	0F	Sector 15 at Side 1				
	08	Sector 8 at Side 1				

Notes: 1. NC (No Change): The same value as the one at the beginning of command execution

2. LSB (Least Significant Bit): The least significant bit of H is complemented.

WRITE DATA

A set of nine (9) bytes are required to set the FDC into the Write Data mode. After the Write Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify Command), and begins reading ID Fields. When the current sector number ("R"), stored in the ID Register (IDR) compares with the sector

number read off the diskette, then the FDC takes data from the processor byte-by-byte via the data bus, and outputs it to the FDD.

After writing data into the current sector, the Sector Number stored in "R" is incremented by one, and the next data field is written into. The FDC continues this "Multi-Sector Write Operation" until the issuance of a Terminal Count signal. If a Terminal Count signal is sent to the FDC it continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written then the remainder of the data field is filled with 00 (zeros).

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (incorrect CRC) in one of the ID Fields, it sets the DE (Data Error) flag of Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

The Write Command operates in much the same manner as the Read Command. The following items are the same; refer to the Read Data Command for details:

- Transfer Capacity
- EN (End of Cylinder) Flag
- ND (No Data) Flag
- Head Unload Time Interval
- ID Information when the processor terminates command (see Table 2)
- Definition of DTL when N = 0 and when N ≠ 0

In the Write Data mode, data transfers between the processor and FDC must occur every 31 μs in the FM mode, and every 15 μs in the MFM mode. If the time interval between data transfers is longer than this then the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Write Data Command.

For mini-floppies, multiple track writes are usually not permitted. This is because of the turn-off time of the erase head coils—the head switches tracks before the erase head turns off. Therefore the system should typically wait 1.3 mS before attempting to step or change sides.

WRITE DELETED DATA

This command is the same as the Write Data Command except a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark.

READ DELETED DATA

This command is the same as the Read Data Command except that when the FDC detects a Data Address Mark at the beginning of a Data Field (and SK = 0 (low)), it will read all the data in the sector and set the CM flag in Status Register 2 to a 1 (high), and then terminate the command. If SK = 1, then the FDC skips the sector with the Data Address Mark and reads the next sector.

READ A TRACK

This command is similar to READ DATA Command except that the entire data field is read continuously from each of the sectors of a track. Immediately after encountering the INDEX HOLE, the FDC starts reading all data fields on the track as continuous blocks of data. If the FDC finds an error in the ID or DATA CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR, and sets the ND flag of Status Register 1 to a 1 (high) if there is no comparison. Multi-track or skip operations are not allowed with this command.

This command terminates when EOT number of sectors have been read. If the FDC does not find an ID Address Mark on the diskette after it encounters the INDEX HOLE for the second time, then it sets the MA (missing address mark) flag in Status Register 1 to a 1 (high), and terminates the command. (Status Register 0 has bits 7 and 6 set to 0 and 1 respectively.)

READ ID

The READ ID Command is used to give the present position of the recording head. The FDC stores the values from the first ID Field it is able to read. If no proper ID Address Mark is found on the diskette, before the INDEX HOLE is encountered for the second time then the MA (Missing Address Mark) flag in Status Register 1 is set to a 1 (high), and if no data is found then the ND (No Data) flag is also set in Status Register 1 to a 1 (high) and the command is terminated.

FORMAT A TRACK

The Format Command allows an entire track to be formatted. After the INDEX HOLE is detected, Data is written on the Diskette: Gaps, Address Marks, ID Fields and Data Fields, all per the IBM System 34 (Double Density) or System 3740 (Single Density) Format are recorded. The particular format which will be written is controlled by the values programmed into N (number of bytes/sector), SC (sectors/cylinder), GPL (Gap Length), and D (Data Pattern) which are supplied by the processor during the Command Phase. The Data Field is filled with the Byte of data stored in D. The ID Field for each sector is supplied by the processor; that is, four data requests per sector are made by the FDC for C (Cylinder Number), H (Head Number), R (Sector Number) and N (Number of Bytes/Sector). This allows the diskette to be formatted with nonsequential sector numbers, if desired.

After formatting each sector, the processor must send new values for C, H, R, and N to the 8272A for each sector on the track. The contents of the R Register is incremented by one after each sector is formatted, thus, the R register contains a value of R + 1 when it is read during the Result Phase. This incrementing and formatting continues for the whole track until the FDC encounters the INDEX HOLE for the second time, whereupon it terminates the command.

If a FAULT signal is received from the FDD at the end of a write operation, then the FDC sets the EC flag of Status Register 0 to a 1 (high), and terminates the command after setting bits 7 and 6 of Status Register 0 to 0 and 1 respectively. Also the loss of a READY signal at the beginning of a command execution phase causes command termination.

Table 9 shows the relationship between N, SC, and GPL for various sector sizes:

Table 9. Sector Size Relationships.

	8" STANDARD FLOPPY						5¼" MINI FLOPPY				
FORMAT	SECTOR SIZE	N	SC	GPL[1]	GPL[2]	REMARKS	SECTOR SIZE	N	SC	GPL[1]	GPL[2]
FM Mode	128 bytes/Sector	00	1A	07	1B	IBM Diskette 1	128 bytes/Sector	00	12	07	09
	256	01	0F	0E	2A	IBM Diskette 2	128	00	10	10	19
	512	02	08	1B	3A		256	01	08	18	30
	1024	03	04	47	8A		512	02	04	46	87
	2048	04	02	C8	FF		1024	03	02	C8	FF
	4096	05	01	C8	FF		2048	04	01	C8	FF
MFM Mode	256	01	1A	0E	36	IBM Diskette 2D	256	01	12	0A	0C
	512	02	0F	1B	54		256	01	10	20	32
	1024	03	08	35	74	IBM Diskette 2D	512	02	08	2A	50
	2048	04	04	99	FF		1024	03	04	80	F0
	4096	05	02	C8	FF		2048	04	02	C8	FF
	8192	06	01	C8	FF		4096	05	01	C8	FF

Note: 1. Suggested values of GPL in Read or Write Commands to avoid splice point between data field and ID field of contiguous sections

2. Suggested values of GPL in format command.

SCAN COMMANDS

The SCAN Commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system (Processor in NON-DMA mode, and DMA Controller in DMA mode). The FDC compares the data on a byte-by-byte basis, and looks for a sector of data which meets the conditions of $D_{FDD} = D_{Processor}$, $D_{FDD} \leq D_{Processor}$, or $D_{FDD} \geq D_{Processor}$. Ones complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremented (R + STP → R), and the scan operation is continued. The scan operation continues until one of the following conditions occur; the conditions for scan are met (equal, low, or high), the last sector on the track is reached (EOT), or the terminal count signal is received.

If the conditions for scan are met then the FDC sets the SH (Scan Hit) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (Scan Not Satisfied) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. The receipt of a TERMINAL COUNT signal from the Processor or DMA Controller during the scan operation will cause the FDC to complete the comparison of the particular byte which is in process, and then to terminate the command. Table 10 shows the status of bits SH and SN under various conditions of SCAN.

Table 10. Scan Status Codes

COMMAND	STATUS REGISTER 2		COMMENTS
	BIT 2 = SN	BIT 3 = SH	
Scan Equal	0	1	$D_{FDD} = D_{Processor}$
	1	0	$D_{FDD} \neq D_{Processor}$
Scan Low or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} < D_{Processor}$
	1	0	$D_{FDD} \leq D_{Processor}$
Scan High or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} > D_{Processor}$
	1	0	$D_{FDD} \geq D_{Processor}$

If the FDC encounters a Deleted Data Address Mark on one of the sectors (and SK = 0), then it regards the sector as the last sector on the cylinder, sets CM (Control Mark) flag of Status Register 2 to a 1 (high) and terminates the command. If SK = 1, the FDC skips the sector with the Deleted Address Mark, and reads the next sector. In the second case (SK = 1), the FDC sets the CM (Control Mark) flag of Status Register 2 to a 1 (high) in order to show that a Deleted Sector had been encountered.

When either the STP (contiguous sectors STP = 01, or alternate sectors STP = 02 sectors are read) or the MT (Multi-Track) are programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26, and we start the Scan Command at sector 21; the following will happen. Sectors 21, 23, and 25 will be read, then the next sector (26) will be skipped and the Index Hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the Scan Command would be completed in a normal manner.

During the Scan Command data is supplied by either the processor or DMA Controller for comparison against the data read from the diskette. In order to avoid having the OR (Over Run) flag set in Status Register 1, it is necessary to have the data available in less than 27 μs (FM Mode) or 13 μs (MFM Mode). If an Overrun occurs the FDC terminates the command.

SEEK

The read/write head within the FDD is moved from cylinder to cylinder under control of the Seek Command. The FDC compares the PCN (Present Cylinder Number) which is the current head position with the NCN (New Cylinder Number), and performs the following operation if there is a difference:

PCN < NCN: Direction signal to FDD set to a 1 (high), and Step Pulses are issued. (Step In.)

PCN > NCN: Direction signal to FDD set to a 0 (low) and Step Pulses are issued. (Step Out.)

The rate at which Step Pulses are issued is controlled by SRT (Stepping Rate Time) in the SPECIFY Command. After each Step Pulse is issued NCN is compared against PCN, and when NCN = PCN, then the SE (Seek End) flag is set in Status Register 0 to a 1 (high), and the command is terminated.

During the Command Phase of the Seek operation the FDC is in the FDC BUSY state, but during the Execution Phase it is in the NON BUSY state. While the FDC is in the NON BUSY state, another Seek Command may be issued, and in this manner parallel seek operations may be done on up to 4 Drives at once.

If an FDD is in a NOT READY state at the beginning of the command execution phase or during the seek operation, then the NR (NOT READY) flag is set in Status Register 0 to a 1 (high), and the command is terminated.

Note that the 8272A Read and Write Commands do not have implied Seeks. Any R/W command should be preceded by: 1) Seek Command; 2) Sense Interrupt Status; and 3) Read ID.

RECALIBRATE

This command causes the read/write head within the FDD to retract to the Track 0 position. The FDC clears the contents of the PCN counter, and checks the status of the Track 0 signal from the FDD. As long as the Track 0 signal is low, the Direction signal remains 1 (high) and Step Pulses are issued. When the Track 0 signal goes high, the SE (SEEK END) flag in Status Register 0 is set to a 1 (high) and the command is terminated. If the Track 0 signal is still low after 77 Step Pulses have been issued, the FDC sets the SE (SEEK END) and EC (EQUIPMENT CHECK) flags of Status Register 0 to both 1s (highs), and terminates the command.

The ability to overlap RECALIBRATE Commands to multiple FDDs, and the loss of the READY signal, as described in the SEEK Command, also applies to the RECALIBRATE Command.

SENSE INTERRUPT STATUS

An Interrupt signal is generated by the FDC for one of the following reasons:

1. Upon entering the Result Phase of:
   a. Read Data Command
   b. Read a Track Command
   c. Read ID Command
   d. Read Deleted Data Command
   e. Write Data Command
   f. Format a Cylinder Command
   g. Write Deleted Data Command
   h. Scan Commands
2. Ready Line of FDD changes state
3. End of Seek or Recalibrate Command
4. During Execution Phase in the NON-DMA Mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. However, interrupts caused by reasons 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt Status Command. This command when issued resets the interrupt signal and via bits 5, 6, and 7 of Status Register 0 identifies the cause of the interrupt.

Neither the Seek or Recalibrate Command have a Result Phase. Therefore, it is mandatory to use the Sense Interrupt Status Command after these commands to effectively terminate them and to provide verification of the head position (PCN).

Table 11. Seek, Interrupt Codes

SEEK END BIT 5	INTERRUPT CODE		CAUSE
	BIT 6	BIT 7	
0	1	1	Ready Line changed state, either polarity
1	0	0	Normal Termination of Seek or Recalibrate Command
1	1	0	Abnormal Termination of Seek or Recalibrate Command

SPECIFY

The Specify Command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the Execution Phase of one of the Read/Write Commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (01 = 16 ms, 02 = 32 ms .... OF = 240 ms). The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms, etc.). The HLT (Head Load Time) defines the time between when the Head Load signal goes high and when the Read/Write operation starts. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms .... FE = 254 ms).

The step rate should be programmed 1 mS longer than the minimum time required by the drive.

The time intervals mentioned above are a direct function of the clock (CLK on pin 19). Times indicated above are for an 8 MHz clock, if the clock was reduced to 4 MHz (mini-floppy application) then all time intervals are increased by a factor of 2.

The choice of DMA or NON-DMA operation is made by the ND (NON-DMA) bit. When this bit is high (ND = 1) the NON-DMA mode is selected, and when ND = 0 the DMA mode is selected.

SENSE DRIVE STATUS

This command may be used by the processor whenever it wishes to obtain the status of the FDDs. Status Register 3 contains the Drive Status information.

INVALID

If an invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command. No interrupt is generated by the 8272A during this condition. Bit 6 and bit 7 (DIO and RQM) in the Main Status Register are both high ("1") indicating to the processor that the 8272A is in the Result Phase and the contents of Status Register 0 (ST0) must be read. When the processor reads Status Register 0 it will find an 80H indicating an invalid command was received.

A Sense Interrupt Status Command must be sent after a Seek or Recalibrate interrupt, otherwise the FDC will consider the next command to be an Invalid Command.

In some applications the user may wish to use this command as a No-Op command, to place the FDC in a standby or no operation state.

Table 12. Status Registers

BIT NO.	BIT NAME	BIT SYMBOL	DESCRIPTION
STATUS REGISTER 0			
D_7	Interrupt Code	IC	$D_7 = 0$ and $D_6 = 0$ Normal Termination of Command, (NT). Command was completed and properly executed.
D_6			$D_7 = 0$ and $D_6 = 1$ Abnormal Termination of Command, (AT). Execution of Command was started, but was not successfully completed.
			$D_7 = 1$ and $D_6 = 0$ Invalid Command issue, (IC). Command which was issued was never started.
			$D_7 = 1$ and $D_6 = 1$ Abnormal Termination because during command execution the ready signal from FDD changed state.
D_5	Seek End	SE	When the FDC completes the SEEK Command, this flag is set to 1 (high).
D_4	Equipment Check	EC	If a fault Signal is received from the FDD, or if the Track 0 Signal fails to occur after 77 Step Pulses (Recalibrate Command) then this flag is set.
D_3	Not Ready	NR	When the FDD is in the not-ready state and a read or write command is issued, this flag is set. If a read or write command is issued to Side 1 of a single sided drive, then this flag is set.
D_2	Head Address	HD	This flag is used to indicate the state of the head at Interrupt.
D_1	Unit Select 1	US 1	These flags are used to indicate a
D_0	Unit Select 0	US 0	Drive Unit Number at Interrupt
STATUS REGISTER 1			
D_7	End of Cylinder	EN	When the FDC tries to access a Sector beyond the final Sector of a Cylinder, this flag is set.
D_6			Not used. This bit is always 0 (low).
D_5	Data Error	DE	When the FDC detects a CRC error in either the ID field or the data field, this flag is set.
D_4	Over Run	OR	If the FDC is not serviced by the main-systems during data transfers, within a certain time interval, this flag is set.
D_3			Not used. This bit always 0 (low).
D_2	No Data	ND	During execution of READ DATA, WRITE DELETED DATA or SCAN Command, if the FDC cannot find the Sector specified in the IDR Register, this flag is set.
			During executing the READ ID Command, if the FDC cannot read the ID field without an error, then this flag is set.
			During the execution of the READ A Cylinder Command, if the starting sector cannot be found, then this flag is set.

BIT NO.	BIT NAME	BIT SYMBOL	DESCRIPTION
STATUS REGISTER 1 (CONT.)			
D_1	Not Writable	NW	During execution of WRITE DATA, WRITE DELETED DATA or Format A Cylinder Command, if the FDC detects a write protect signal from the FDD, then this flag is set.
D_0	Missing Address Mark	MA	If the FDC cannot detect the ID Address Mark after encountering the index hole twice, then this flag is set.
			If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. Also at the same time, the MD (Missing Address Mark in Data Field) of Status Register 2 is set.
STATUS REGISTER 2			
D_7			Not used. This bit is always 0 (low).
D_6	Control Mark	CM	During executing the READ DATA or SCAN Command, if the FDC encounters a Sector which contains a Deleted Data Address Mark, this flag is set.
D_5	Data Error in Data Field	DD	If the FDC detects a CRC error in the data field then this flag is set.
D_4	Wrong Cylinder	WC	This bit is related with the ND bit, and when the contents of C on the medium is different from that stored in the IDR, this flag is set.
D_3	Scan Equal Hit	SH	During execution, the SCAN Command, if the condition of "equal" is satisfied, this flag is set.
D_2	Scan Not Satisfied	SN	During executing the SCAN Command, if the FDC cannot find a Sector on the cylinder which meets the condition, then this flag is set.
D_1	Bad Cylinder	BC	This bit is related with the ND bit, and when the content of C on the medium is different from that stored in the IDR and the content of C is FF, then this flag is set.
D_0	Missing Address Mark in Data Field	MD	When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set.
STATUS REGISTER 3			
D_7	Fault	FT	This bit is used to indicate the status of the Fault signal from the FDD.
D_6	Write Protected	WP	This bit is used to indicate the status of the Write Protected signal from the FDD.
D_5	Ready	RDY	This bit is used to indicate the status of the Ready signal from the FDD.
D_4	Track 0	T0	This bit is used to indicate the status of the Track 0 signal from the FDD.
D_3	Two Side	TS	This bit is used to indicate the status of the Two Side signal from the FDD.
D_2	Head Address	HD	This bit is used to indicate the status of Side Select signal to the FDD.
D_1	Unit Select 1	US 1	This bit is used to indicate the status of the Unit Select 1 signal to the FDD.
D_0	Unit Select 0	US 0	This bit is used to indicate the status of the Unit Select 0 signal to the FDD.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −40°C to +125°C
All Output Voltages ..... −0.5 to +7 Volts
All Input Voltages ..... −0.5 to +7 Volts
Supply Voltage V_{CC} ..... −0.5 to +7 Volts
Power Dissipation ..... 1 Watt

*T_A = 25°C

NOTICE: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = +5V ±10%)

Symbol	Parameter	Limits		Unit	Test Conditions
		Min.	Max.		
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.0 mA
V_{OH}	Output High Voltage	2.4	V_{CC}	V	I_{OH} = −400 μA
I_{CC}	V_{CC} Supply Current		120	mA	
I_{IL}	Input Load Current (All Input Pins)		10 −10	μA μA	V_{IN} = V_{CC} V_{IN} = 0V
I_{LOH}	High Level Output Leakage Current		10	μA	V_{OUT} = V_{CC}
I_{OFL}	Output Float Leakage Current		±10	μA	0.45V ≤ V_{OUT} ≤ V_{CC}

CAPACITANCE (T_A = 25°C, f_c = 1 MHz, V_{CC} = 0V)

Symbol	Parameter	Limits		Unit	Test Conditions
		Min.	Max.		
$C_{IN(\Phi)}$	Clock Input Capacitance		20	pF	All Pins Except Pin Under Test Tied to AC Ground
C_{IN}	Input Capacitance		10	pF	
$C_{I/O}$	Input/Output Capacitance		20	pF	

A.C. CHARACTERISTICS (T_A0°C to +70°C, V_{CC} = +5.0V ±10%)

CLOCK TIMING

Symbol	Parameter	Min.	Max.	Unit	Notes
tCY	Clock Period	120	500	ns	Note 5
tCH	Clock High Period	40		ns	Note 4, 5
tRST	Reset Width	14		tCY	

READ CYCLE

tAR	Select Setup to $\overline{RD}$↓	0		ns	
tRA	Select Hold from $\overline{RD}$↑	0		ns	
tRR	$\overline{RD}$ Pulse Width	250		ns	
tRD	Data Delay from $\overline{RD}$↓		200	ns	
tDF	Output Float Delay	20	100	ns	

A.C. CHARACTERISTICS (Continued) (T_A 0°C to +70°C, V_{CC} = +5.0V ± 10%)

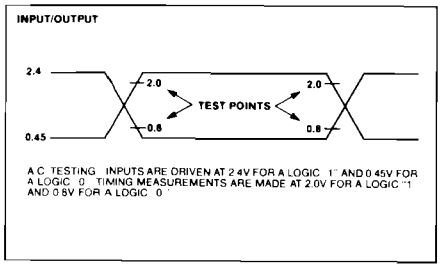
WRITE CYCLE

Symbol	Parameter	Typ.[1]	Min.	Max.	Unit	Notes
tAW	Select Setup to $\overline{WR}$↓		0		ns	
tWA	Select Hold from $\overline{WR}$↑		0		ns	
tWW	$\overline{WR}$ Pulse Width		250		ns	
tDW	Data Setup to $\overline{WR}$↑		150		ns	
tWD	Data Hold from $\overline{WR}$↑		5		ns	
INTERRUPTS						
tRI	INT Delay from $\overline{RD}$↑			500	ns	Note 6
tWI	INT Delay from $\overline{WR}$↑			500	ns	Note 6
DMA						
tRQCY	DRQ Cycle Period		13		µs	Note 6
tAKRQ	$\overline{DACK}$↓ to DRQ↓			200	ns	
tRQR	DRQ↑ to $\overline{RD}$↓		800		ns	Note 6
tRQW	DRQ↑ to $\overline{WR}$↓		250		ns	Note 6
tRQRW	DRQ↑ to $\overline{RD}$↑ or $\overline{WR}$↑			12	µs	Note 6
FDD INTERFACE						
tWCY	WCK Cycle Time	2 or 4 1 or 2			µs	MFM = 0 MFM = 1 Note 2
tWCH	WCK High Time	250	80	350	ns	
tCP	Pre-Shift Delay from WCK↑		20	100	ns	
tCD	WDA Delay from WCK↑		20	100	ns	
tWDD	Write Data Width		tWCH - 50		ns	
tWE	WE↑ to WCK↑ or WE↓ to WCK↓ Delay		20	100	ns	
tWWCY	Window Cycle Time	2 1			µs	MFM = 0 MFM = 1
tWRD	Window Setup to RDD↑		15		ns	
tRDW	Window Hold from RDD↓		15		ns	
tRDD	RDD Active Time (HIGH)		40		ns	
FDD SEEK/DIRECTION/STEP						
tUS	$US_{0,1}$ Setup to $\overline{RW}$/SEEK↑		12		µs	Note 6
tSU	$US_{0,1}$ Hold after $\overline{RW}$/SEEK↓		15		µs	Note 6
tSD	$\overline{RW}$/SEEK Setup to LCT/DIR		7		µs	Note 6
tDS	$\overline{RW}$/SEEK Hold from LCT/DIR		30		µs	Note 6
tDST	LCT/DIR Setup to FR/STEP↑		1		µs	Note 6
tSTD	LCT/DIR Hold from FR/STEP↓		24		µs	Note 6
tSTU	$DS_{2,1}$ Hold from FR/Step↓		5		µs	Note 6
tSTP	STEP Active Time (High)	5			µs	Note 6
tSC	STEP Cycle Time		33		µs	Note 3, 6
tFR	FAULT RESET Active Time (High)		8	10	µs	Note 6
tIDX	INDEX Pulse Width	10			tCY	
tTC	Terminal Count Width		1		tCY	

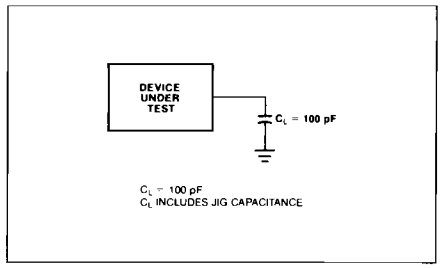
NOTES:

1. Typical values for T_A = 25°C and nominal supply voltage.
2. The former values are used for standard floppy and the latter values are used for mini-floppies.
3. tSC = 33 µs min. is for different drive units. In the case of same unit, tSC can be ranged from 1 ms to 16 ms with 8 MHz clock period, and 2 ms to 32 ms with 4 MHz clock, under software control.
4. From 2.0V to +2.0V.
5. At 4 MHz, the clock duty cycle may range from 16% to 76%. Using an 8 MHz clock the duty cycle can range from 32% to 52%. Duty cycle is defined as: D.C. = 100 (tCH ÷ tCY) with typical rise and fall times of 5 ns.
6. The specified values listed are for an 8 MHz clock period. Multiply timings by 2 when using a 4 MHz clock period.

A.C. TESTING INPUT, OUTPUT WAVEFORM

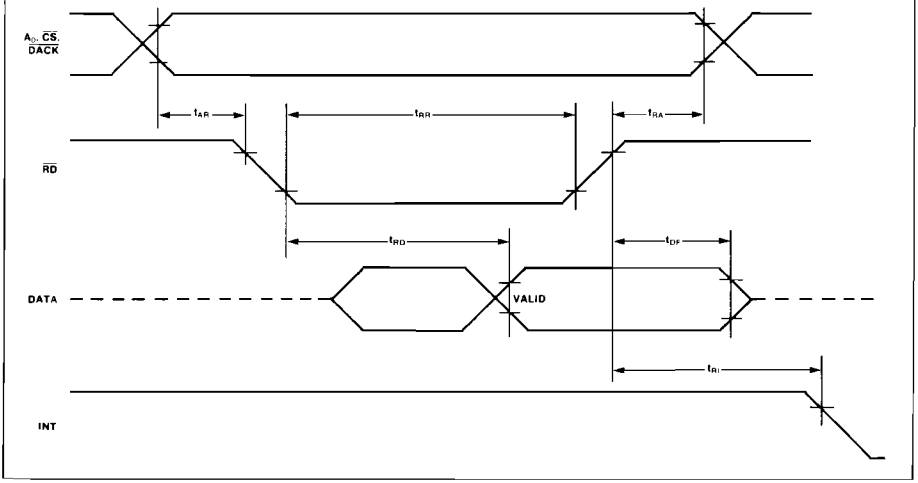


A.C. TESTING LOAD CIRCUIT



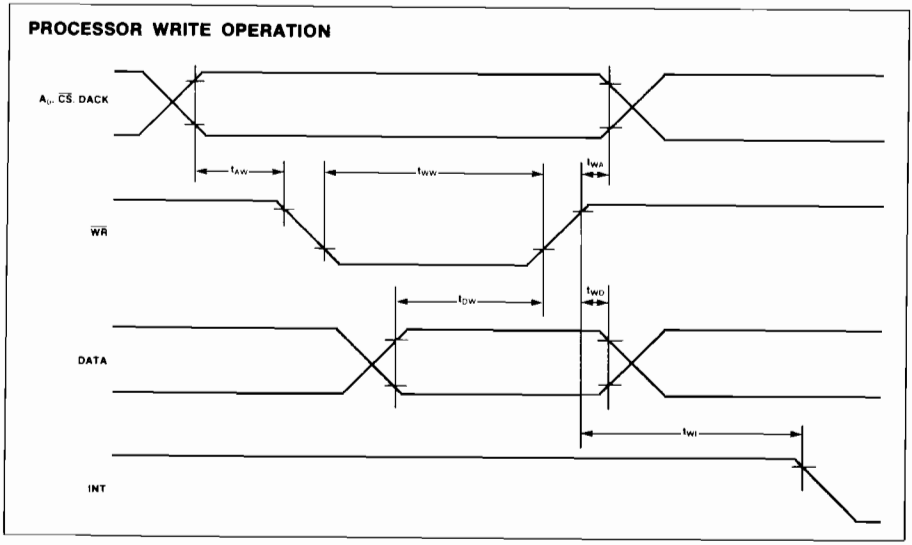
WAVEFORMS

PROCESSOR READ OPERATION

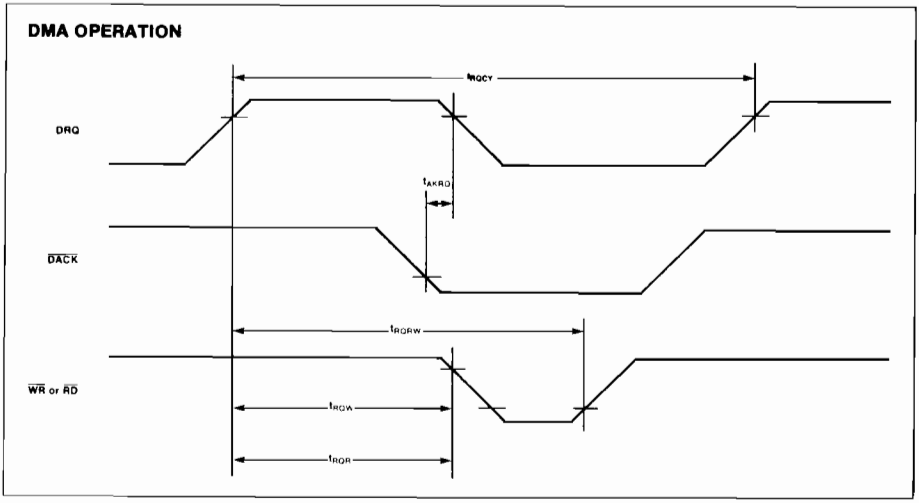


WAVEFORMS (Continued)

PROCESSOR WRITE OPERATION

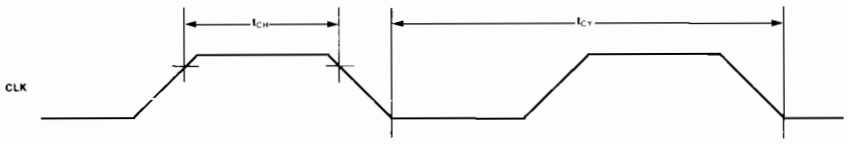


DMA OPERATION

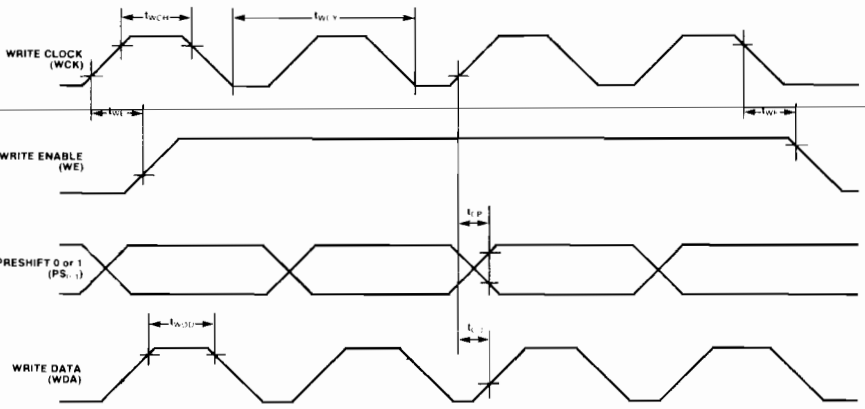


WAVEFORMS (Continued)

CLOCK TIMING

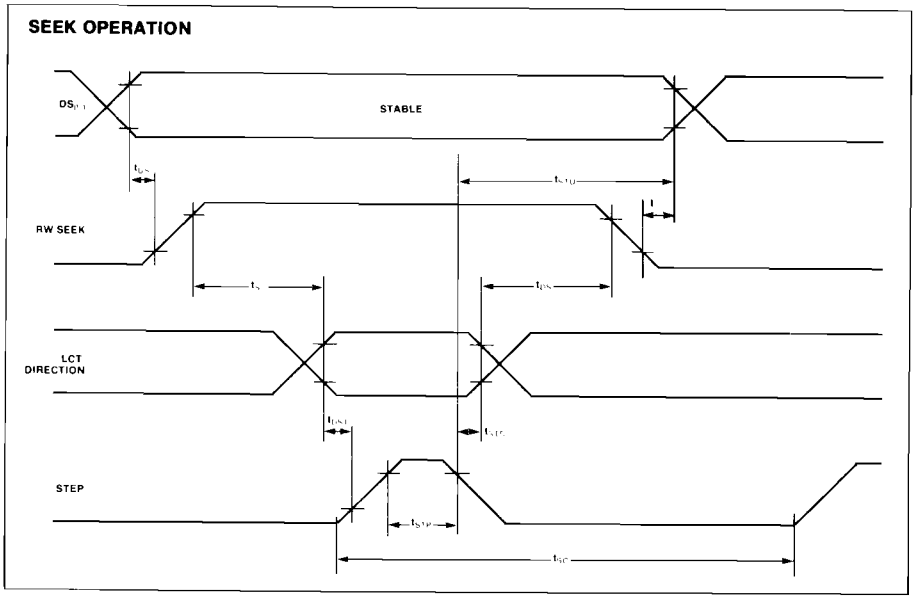


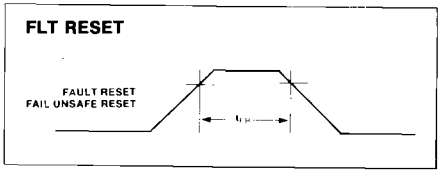
FDD WRITE OPERATION

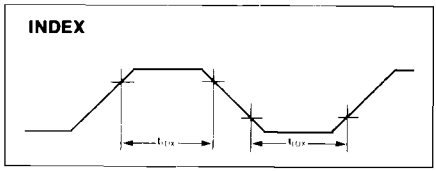


	PRESHIFT 0	PRESHIFT 1
NORMAL	0	0
LATE	0	1
EARLY	1	0
INVALID	1	1

WAVEFORMS (Continued)

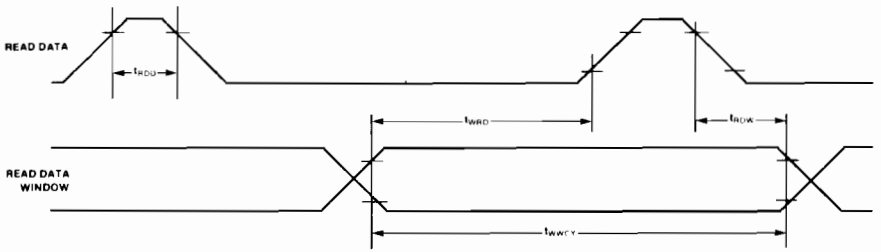




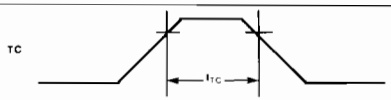


WAVEFORMS (Continued)

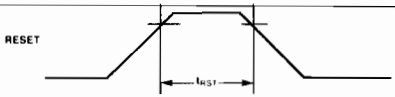
FDD READ OPERATION



TERMINAL COUNT



RESET

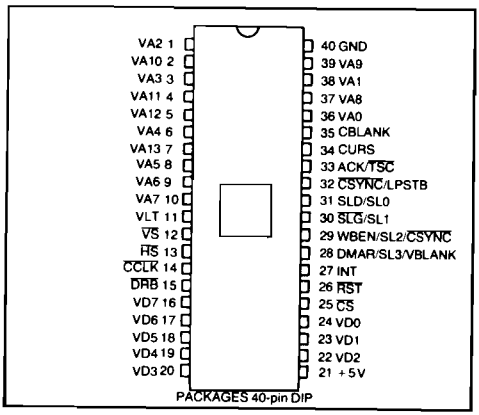


CRT Video Processor and Controller
VPAC™

FEATURES

- ☐ Fully Programmable Display Format
  - Characters per Data Row (8-240)
  - Data Rows per Frame (2-256)
  - Raster Scans per Data Row (1-32)
- ☐ Programmable Monitor Sync Format
  - Raster Scans/Frame (4-2048)
  - Front Porch — Horizontal (Negative or Positive)
  - — Vertical
  - Sync Width — Horizontal (1-128 Character Times)
  - — Vertical (2-256 Scan Lines)
  - Back Porch — Horizontal
  - — Vertical
- ☐ Direct Outputs to CRT Monitor
  - Horizontal Sync
  - Vertical Sync
  - Composite Sync
  - Composite Blanking
  - Cursor Coincidence
- ☐ Binary Addressing of Video Memory
- ☐ Row-Table Driven or Sequential Video Addressing Modes
- ☐ Programmable Status Row Position and Address Registers
- ☐ Bidirectional Partial or Full Page Smooth Scroll
- ☐ Attribute Assemble Mode
- ☐ Double Height Data Row Mode
- ☐ Double Width Data Row Mode
- ☐ Programmable DMA Burst Mode
- ☐ Configurable with a Variety of Memory Contention Arrangements
- ☐ Light Pen Register
- ☐ Cursor Horizontal and Vertical Position Registers
- ☐ Maskable Processor Interrupt Line
- ☐ Internal Status Register
- ☐ Three-state Video Memory Address Bus
- ☐ Partial or Full Page Blank Capability
- ☐ Two Interlace Modes: Enhanced Video and Alternate Scan Line

PIN CONFIGURATION



PACKAGES 40-pin DIP

- ☐ Ability to Delay Cursor and Blanking with respect to Active Video
- ☐ Programmable for Horizontal Split Screen Applications
- ☐ Graphics Compatible
- ☐ Ability to Externally Sync each Raster Line, each Field
- ☐ Single +5 Volt Power Supply
- ☐ TTL Compatible on All Inputs and Outputs
- ☐ VT-100 Compatible
- ☐ RS-170 Interlaced Composite Sync Available

GENERAL DESCRIPTION

The CRT 9007 VPAC™ is a next generation video processor/controller—an MOS LSI integrated circuit which supports either sequential or row-table driven memory addressing modes. As indicated by the features above, the VPAC™ provides the user with a wide range of programmable features permitting low cost implementation of high performance CRT systems. Its 14 address lines can directly address up to 16K of video memory. This is equivalent to eight pages of an 80 character by 24 line CRT display. Smooth or jump scroll operations may be performed anywhere within the addressable memory. In addition, status rows can be defined anywhere on the screen.

In the sequential video addressing mode, a Table Start Register points to the address of the first character of the first data row on the screen. It can be easily changed to produce a scrolling effect on the screen. By using this register in conjunction with two auxiliary address registers and two sequential break registers, a screen roll can be produced with a stable status row held at either the first or last data row position.

In the row-table driven video addressing mode, each row in the video display is designated by its own address. This provides the user with greater flexibility than sequential addressing since the rows of characters are linked by pointers instead of residing in sequential memory locations. Operations such as data row insertion, deletion, and replication are easily accomplished by manipulating pointers instead of entire lines. The row table itself can be stored in memory in a linked list or in a contiguous format.

The VPAC™ works with a variety of memory contention schemes including operation with a Single Row Buffer such as the CRT 9006, a Double Row Buffer such as the CRT 9212, or no buffer at all, in which case character addresses are output during each displayable scan line.

User accessable internal registers provide such features as light pen, interrupt enabling, cursor addressing, and VPAC™ status. Ten of these registers are used for screen formatting with the ability to define over 200 characters per data row and up to 256 data rows per frame. These 10 registers contain the "vital screen parameters".

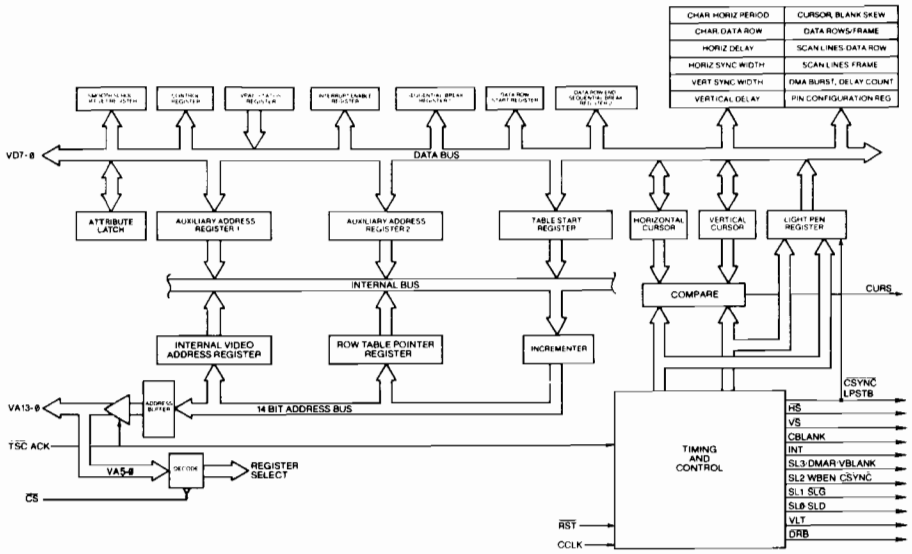


FIGURE 1: CRT 9007 BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PROCESSOR INTERFACE:

PIN NO.	NAME	SYMBOL	FUNCTION
7, 5, 4, 2, 39, 37, 10, 9, 8, 6, 3, 1, 38, 36	Video Address 13-0	VA13-VA0	These 14 signals are the binary address presented to the video memory by the CRT 9007. The function depends on the particular CRT 9007 mode of operation. VA13-6 are outputs only. VA5-0 are bidirectional. —Double Row Buffer Configuration: VA13-0 are active outputs for the DMA operations and are in their high impedance state at all other times. —Single Row Buffer Configuration: VA13-0 are active outputs during the first scan line of each data row and are in their high impedance state at all other times. —Repetitive Memory Addressing Configuration: VA13-0 are active outputs at all times except during horizontal and vertical retrace at which time they are in their high impedance state. If row table addressing is used for either single row buffer or repetitive memory addressing modes, VA13-0 are active outputs during the horizontal retrace at each data row boundary to allow the CRT 9007 to retrieve the row table address. For processor read/write operations VA5-0 are inputs that select the appropriate internal register.
16, 17, 18, 19, 20, 22, 23, 24	Video Data 7-0	VD7-VD0	Bidirectional video data bus: during processor Read/write operations data is transferred via VD7-VD0 when chip strobe ($\overline{CS}$) is active. These lines are in their high impedance state when $\overline{CS}$ is inactive. During CRT 9007 DMA operations, data from video memory is input via VD7-VD0 when a new row table address is being retrieved or when the attribute latch is being updated in the attribute assemble mode. VD7-VD0 are outputs when the external row buffer is updated with a new attribute in the attribute assemble mode.
25	Chip strobe	$\overline{CS}$	Input; this signal when active low, allows the processor to read or write internal CRT 9007 registers. When reading from an internal CRT 9007 register, the chip strobe ($\overline{CS}$) enables the output drivers. When writing to an internal CRT 9007 register, the trailing edge of this signal latches the incoming data. Figure 2 shows all processor read/write timing.
26	Reset	$\overline{RST}$	Input; this active low signal puts the CRT 9007 into a known, inactive state and insures that the horizontal sync (HS) output is inactive. Activating this input has the same effect as a RESET command. After initialization, a START command causes normal CRT 9007 operation. See processor addressable registers section, Register 16 for the reset state definition.
27	Interrupt	INT	Output; an interrupt to the processor from the CRT 9007 occurs when this signal is active high. The interrupt returns to its inactive low state when the status register is read.

DESCRIPTION OF PIN FUNCTIONS CONT'D

CRT INTERFACE:

PIN NO.	NAME	SYMBOL	FUNCTION
11	Visible Line Time	VLT	Output; this signal is active high during all visible scan lines and during the horizontal trace times at vertical retrace. This signal can be used to gate the character clock (CCLK) when supplying data to a character generator from a single or double row buffer.
12	Vertical Sync	$\overline{VS}$	Open drain output; this signal determines the vertical position of displayed text by initiating a vertical retrace. Its position and pulse width are user programmable. The open drain allows the vertical frame rate to be synchronized to the line frequency when using monitors with DC coupled vertical amplifiers. If the $\overline{VS}$ output is pulled active low externally before the CRT 9007 itself initiates a vertical sync, the CRT 9007 will start its own vertical sync at the next leading edge of horizontal sync ($\overline{HS}$).
13	Horizontal Sync	$\overline{HS}$	Open drain output; this signal determines the horizontal position of displayed text by initiating a horizontal retrace. Its position and pulse width are user programmable. During hardware and software reset, this signal is inactive high. The open drain allows the horizontal scan rate to be synchronized to an external source. If the $\overline{HS}$ output is pulled low externally before the CRT 9007 itself initiates a horizontal sync, the CRT 9007 will start its own horizontal sync on the next character clock ($\overline{CCLK}$).
14	Character Clock	$\overline{CCLK}$	Input; this signal defines the character rate of the screen and is used by the CRT 9007 for all internal timing. A minimum high voltage of 4.3V must be maintained for proper chip operation.
15	Data Row Boundary	$\overline{DRB}$	Output: this signal is active low for one full scan line (from VLT trailing edge to VLT trailing edge) at the top scan line of each new data row. This signal can be used to swap buffers in the double row buffer mode. It indicates the particular horizontal retrace time that the CRT 9007 outputs addresses (VA13-VA0) for single row buffer operation. There will always be one extra $\overline{DRB}$ signal which will become active during the first scan line of the vertical retrace interval.
34	Cursor	$\overline{CURS}$	Output; this signal marks the cursor position on the screen as specified by the horizontal and vertical cursor registers. The signal is active for one character time at the particular character position for all scan lines within the data row. For double height or width characters, this signal is active for 2 consecutive $\overline{CCLK}$'s in every scan line within the data row. For double height characters, this signal can be programmed to be active at the proper position for 2 consecutive data rows. $\overline{CURS}$ is also used to signal either a double height or double width data row by becoming active during the horizontal retrace (CBLANK active) prior to a double height or double width scan line. The time of activation and deactivation is a function of the addressing mode, buffer configuration and the scan line number. See section of Double height/width for details.
35	Composite Blank	CBLANK	Output. This signal when active high, indicates that a retrace (either horizontal or vertical) will be performed. The signal remains active for the entire retrace interval as programmed. It is used to blank the video to a CRT.

USER SELECTABLE PINS: (see Tables 4 and 5)

PIN NO.	NAME	SYMBOL	FUNCTION
28, 29, 30, 31	Scan Line 3-Scan Line 0	SL3-SL0	Output; these 4 signals are the direct scan line counter outputs, in binary form, that indicate to the character generator the current scan line. These signals continue to be updated during the vertical retrace interval. SL3 and SL0 are the most and least significant bits respectively.
28	Direct Memory Access Request	DMAR	Output; this signal is the DMA request issued by the CRT 9007. It will only become active if the acknowledge (ACK) input is inactive. It remains active high throughout the entire DMA operation.
28	Vertical Blank	VBLANK	Output; this signal is active high only during the vertical retrace period.
29	Write Buffer Enable	WBEN	Output; this active high signal is used to gate the clock feeding the write buffer in a double row buffer configuration.
29 or 32	Composite Sync	$\overline{CSYNC}$	Output; this signal provides a true RS-170 composite sync waveform with equalization pulses and vertical serrations in both interlace and noninterlace formats. Figure 3 illustrates the $\overline{CSYNC}$ output in both interlaced and noninterlaced formats.
30	Scan Line Gate	$\overline{SLG}$	Output; this active low signal is used as a clock gate. It captures the correct 5 or 6 $\overline{CCLK}$'s and, in conjunction with SLD (pin 31), allows scan line information to be loaded serially into an external shift register.
31	Scan Line Data	SLD	Output; this signal allows one to load an external shift register with the current scan line count. The count is presented least significant to most significant bit during the 5 or 6 $\overline{CCLK}$'s framed by $\overline{SLG}$. With this form of scan line representation, it is possible to define up to 32 scan lines per data row. The external shift register must be at least 5 bits in length. Even though 6 shifts can occur one should only use the 5 last bits shifted to define the scan line count. The extra shift occurs in interlace or double height character mode to allow the scan line count to be adjusted to its proper value. Figures 4 and 5 illustrate the serial scan line timing.
32	Light Pen Strobe	LPSTB	Input; this signal strobes the current row/column position into the light pen register at its positive transition.
33	Acknowledge	ACK	Input; this active high signal acknowledges a DMA request. It indicates that the processor bus has entered its high impedance state and the CRT 9007 may access video memory. It is not recommended to deactivate this signal during a CRT 9007 DMA cycle because the CRT 9007 will not shut down in a predictable amount of time.
33	Three State Control	$\overline{TSC}$	Input; this signal, when active low, places VA13-VA0 in their high impedance state.

Single Row Buffer Operation

The CRT 9007 configured with a CRT 9006 Single Row Buffer is shown in figure 6. The use of the CRT 9006 Single Row Buffer requires that the buffer be loaded at the video painting rate during the top scan line of each data row. However, after the CRT 9006 is loaded, the CRT 9007 address lines enter their high impedance state for the remaining N-1 scan lines of the data row, thereby permitting full processor access to memory during these scan lines. The percentage of total memory cycles available to the processor is approximately $[(N-1)/N] \times 100$ where N is the total number of scan lines per data row. For a typical system with 12 scan lines per data row this percentage is 92%. Figure 7 illustrates typical timing for the CRT 9007 used with the CRT 9006 Single Row Buffer.

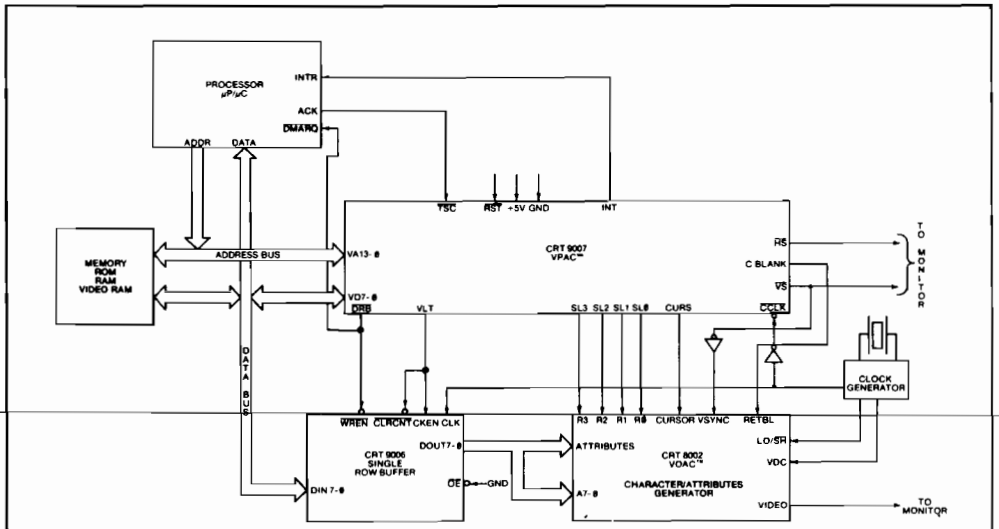


FIGURE 6: CRT 9007 CONFIGURATION WITH SINGLE ROW BUFFER

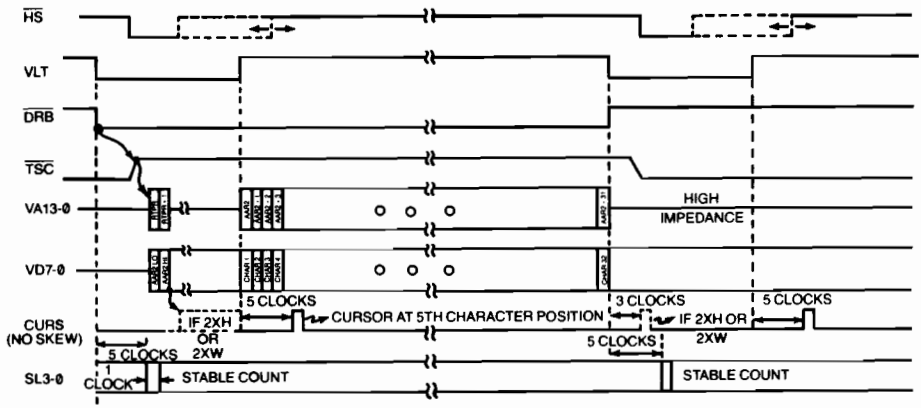


FIGURE 7: CRT 9007 SINGLE ROW BUFFER TIMING (32 CHARACTERS PER DATA ROW)

Double Row Buffer Operation

Figure 8 shows the CRT 9007 used in conjunction with a CRT 9212 Double Row Buffer. The Double Row Buffer has a read buffer which is read at the painting rate of the CRT during each scan line in the data row. While the read buffer is being read and supplying data to the character generator for the current displayed data row, the write buffer is being loaded with the next data row to be displayed. This arrangement allows for relaxed write timing to the write buffer as it may be filled in the time it takes for N scan lines on the CRT to be painted where N is the number of scan lines per data row. Used in this configuration, the CRT 9007 takes advantage of the relaxed write buffer timing by stealing memory cycles from the processor to fill the write buffer (Direct memory access operation). The CRT 9007 sends the DMAR (DMA request) signal, awaits an ACK (acknowledge) signal and then drives out on VA13-VA0 the address at which the next video data resides. The CRT 9007 then activates the WBEN (write buffer enable) signal to write the data into the buffer. If for example there are 80 characters per data row, the CRT 9007 performs 80 DMA operations. The user has the ability to program the number of DMA cycles performed during each DMAR-ACK sequence, as well as the delay between each DMAR-ACK sequence, via the DMA CONTROL REGISTER (RA). If 8 DMA operations are performed for each ACK received, 10 such DMAR-ACK sequences must be performed to completely fill the write buffer. The programmed delay allows the user to evenly distribute the DMA operations so as not to hold up the processor for an excessive length of time. This feature also permits other DMA devices to be used and allows the processor to respond to real time events. In addition, the user has the ability to disable the CRT 9007 DMA mechanism. Figure 9 illustrates typical timing for the CRT 9007 used with the CRT 9212 Double Row Buffer.

Since the CRT 9212 Double Row Buffer has separate inputs for read and write clocks (RCLK, WCLK), it is possible to display proportional character widths (variable number of dots per character) by reading out the buffer at a character clock rate determined by the particular character. The writing of the buffer can be clocked from a different and constant character clock. Figure 10 illustrates the CRT 9007 used with two double row buffers and a CRT 9021 Video Attributes Controller chip to provide proportional character display.

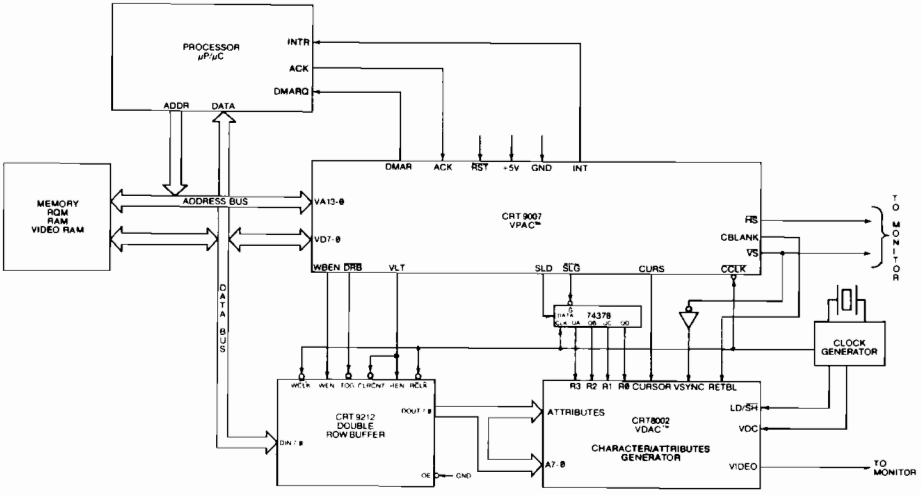


FIGURE 8: CRT 9007 CONFIGURATION WITH DOUBLE ROW BUFFER

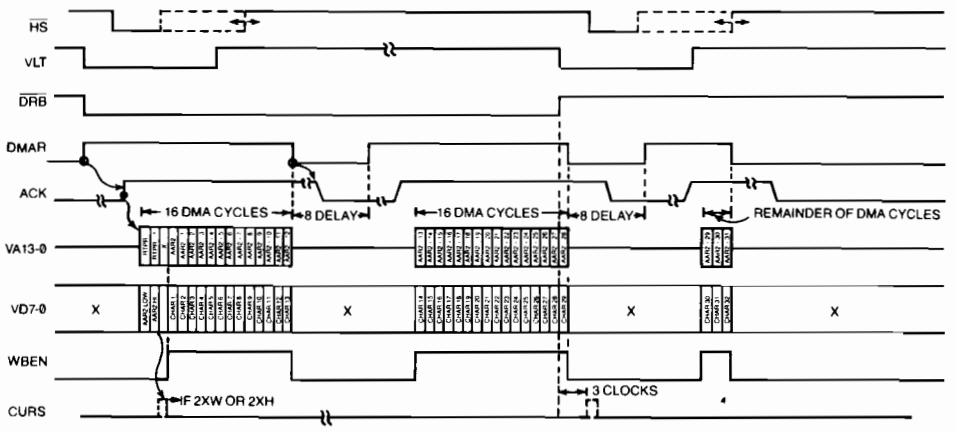


FIGURE 9: CRT 9007 DOUBLE ROW BUFFER TIMING (32 CHARACTERS PER DATA ROW)

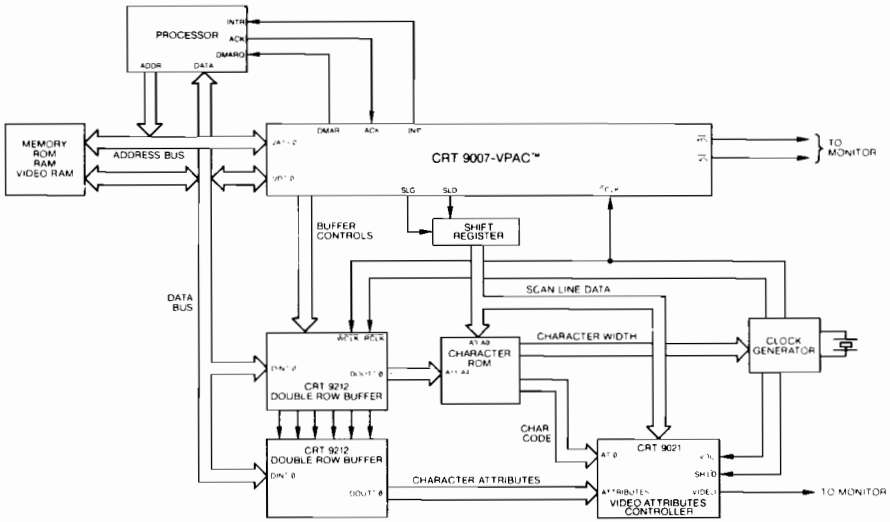


FIGURE 10: CRT 9007 CONFIGURATION FOR PROPORTIONAL CHARACTER DISPLAY

Repetitive Memory Addressing Operation

In this operation mode, the CRT 9007 will repeat the sequence of video addresses for every scan line of every data row. The CRT 9007 address bus will enter its high impedance state during all horizontal retrace intervals (except the retrace interval at a data row boundary if the CRT 9007 is configured in a row driven addressing mode). This arrangement allows for such low end contention schemes as retrace intervention (the processor is only allowed access to video memory during retrace intervals) and processor priority (the processor has an unlimited access to video memory). A high end contention scheme can be employed which uses a double speed memory such that in a single character period both the processor and the CRT 9007 are permitted access to video memory at predetermined time slots. Figure 11 illustrates the CRT 9007 configured with a double speed memory. Typical timing for this mode is illustrated in figure 12.

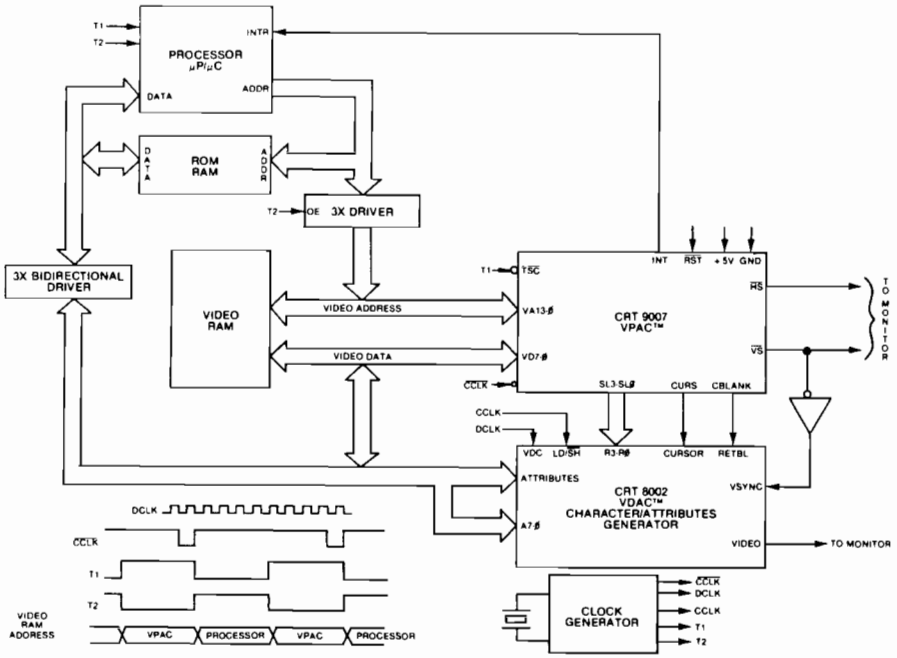


FIGURE 11: CRT 9007 CONFIGURATION WITH DOUBLE SPEED MEMORY

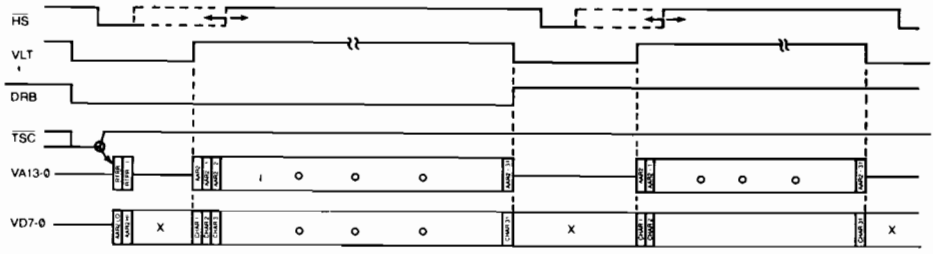


FIGURE 12: CRT 9007 REPETITIVE MEMORY ADDRESS TIMING (32 CHARACTERS PER DATA ROW)

Attribute Assemble Operation

This configuration allows the user to retain an 8 bit wide video memory in which attributes occupy memory locations but not positions on the CRT. This mode assumes that every other display position in video memory contains an attribute. During one clock cycle, attribute data is latched into the CRT 9007; during the next clock cycle a character location is addressed. The attribute data is driven out along with a WBEN signal allowing the character plus its associated attribute to be written simultaneously to two 8 bit double row buffers. Figure 13 illustrates the memory organization used for the Attribute Assemble mode. The first entry in each data row must begin with an attribute.

Figure 14 shows the CRT 9007 configured in the Attribute Assemble mode used with two CRT 9212 Double Row Buffers and 8, 16Kx1 dynamic RAMS. This mode, since it retains an 8 bit wide memory while providing all the advantages of a 16 bit wide memory, lends itself to some cost effective designs using dynamic RAMS. The CRT 9007 will refresh dynamic RAMS because twice the number of the programmed characters per data row are accessed sequentially for each data row.* Figure 15 illustrates typical timing of the CRT 9007 used in the Attribute Assemble mode.

Memory Address (typ)	Memory Data (8 bits)
0D00	Attribute 0
0D01	Character 0
0D02	Attribute 1
0D03	Character 1
0 0 0	0 0 0
2N	Attribute N
2N + 1	Character N

Figure 13: Attribute Assemble Memory Organization

*Note: For 50 Hz operation there usually is about 3 milliseconds extra vertical blanking where refreshing might fail. In this situation the CRT 9007 can be programmed with about 5 more "dummy" data rows while extending the vertical blank signal. This allows the CRT 9007 to start addressing video memory much earlier within the vertical blanking interval and hence provide refresh to the dynamic RAMS. When displaying double height or double width data rows, only half as many sequential locations are accessed each data row and dynamic RAM refresh might fail.

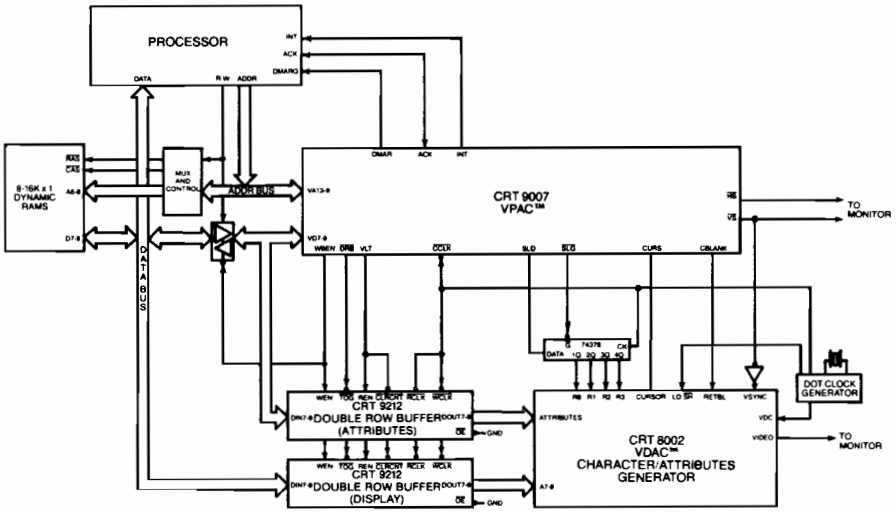
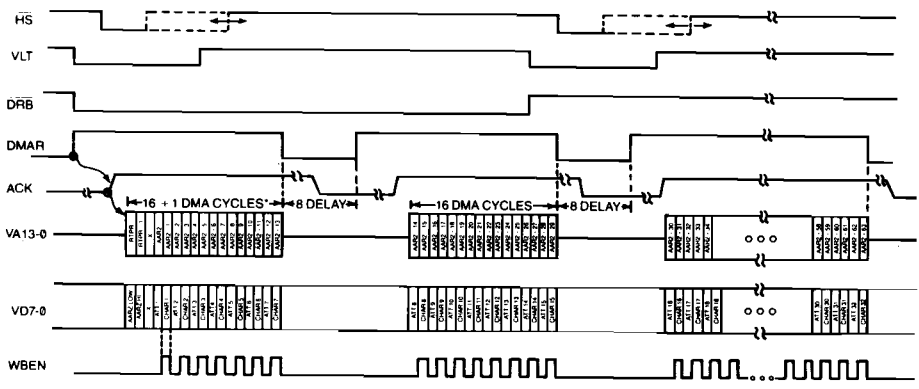


FIGURE 14: CRT 9007 CONFIGURATION FOR ATTRIBUTE ASSEMBLE MODE

Smooth Scroll Operation

Smooth scroll requires that all or a portion of the screen move up or down an integral number of scan lines at a time. 2 user programmable registers allow one to define the "start data row" and the "end data row" for the smooth scroll operation. A SMOOTH SCROLL OFFSET REGISTER (R17), when used in conjunction with a CRT 9007 vertically timed interrupt, allows the user to synchronize the update of the offset register to the vertical frame rate. The offset register causes the scan line counter outputs of the CRT 9007 to start at the programmed offset value rather than zero for the data row that starts the smooth scroll interval. To allow complete flexibility in smooth scroll direction and rate, one can update the offset register in the positive as well as negative direction and can also offset any number of scan lines each frame. Since a smooth scroll can momentarily result in a partial data row consisting of one scan line, the loading of the write buffer under DMA operations for the start and end data row of the smooth scroll operation is forced to occur in one scan line. This condition overrides the programmable DMA CONTROL REGISTER (RA).



*DMA cycles will always end at a character fetch

FIGURE 15: CRT 9007 ATTRIBUTE ASSEMBLE TIMING (32 CHARACTERS PER DATA ROW)

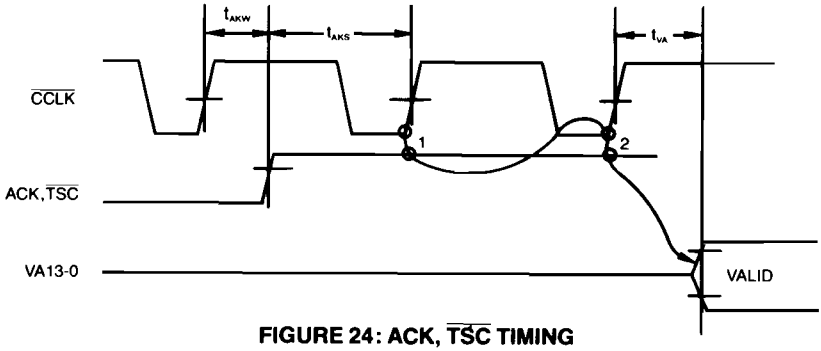


FIGURE 24: ACK, TSC TIMING

Row Table Addressing

In this addressing mode, each data row in video memory is designated by its own starting address. This provides greater flexibility with respect to screen operations than with other addressing schemes used by previous CRT controllers. The row table, which is a list of starting addresses for each data row, can be configured in one of 2 ways. The choice of row table format is highly dependent upon the particular application and the programmer's preference since each format allows full utilization of the CRT 9007 features.

Contiguous Row Table Format

In this format, the TABLE START REGISTER (RC and RD) points to the address where the row table begins. The contents of the first 2 locations define the starting address of the first data row. These 2 bytes define a 14 bit address where the first byte is the low order 8 bits and the second byte is the high order 6 bits. The 2 most significant bits of the second byte define double height/width characteristics to the current data row. The contents of the third and fourth locations define the address where the second data row begins. Figure 16 illustrates the contiguous row table organization in video memory.

Linked List Row Table Format

In this format the TABLE START REGISTER (RC and RD) points to the memory location which starts the entire addressing sequence into operation. The first byte read is the lower 8 bits and the second byte read is the upper 6 bits of the next data row's start address. The 2 most significant bits of the second byte define double height/width characteristics for the data row about to be read. The third, fourth, fifth, etc., bytes read are the first, second, third, etc., characters of the current data row. Figure 17 illustrates the linked list row table organization in video memory.

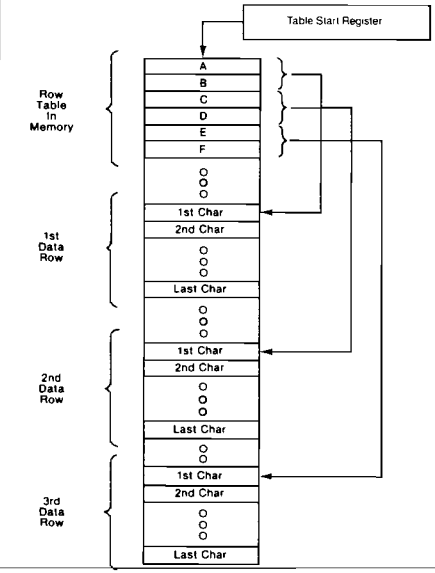


FIGURE 16:
CONTIGUOUS ROW TABLE ADDRESS FORMAT

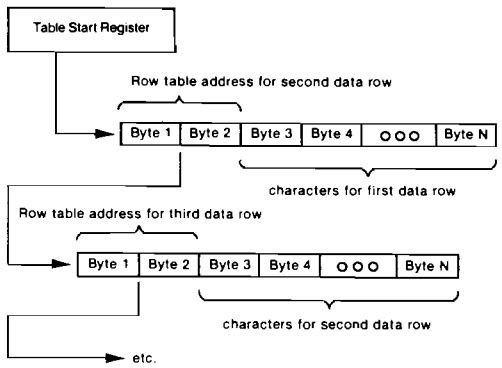


FIGURE 17: LINKED LIST ROW TABLE ADDRESS FORMAT

Sequential Addressing[1]

In this addressing mode, characters on the display screen are located in successive memory locations. The TABLE START REGISTER (RC and RD) points to the address of the first character of the first data row on the screen. In this mode the TABLE START REGISTER does not point to the start of a table but the start of the screen. As each character is read by the CRT 9007 for display refresh, the internal video address register is incremented by one to access the next character.

For more versatile systems operation in the sequential addressing mode, SEQUENTIAL BREAK REGISTER 1 (R10) and SEQUENTIAL BREAK REGISTER 2 (R12) may be used to define the data rows at which two additional

[1]SEQUENTIAL BREAK 2 is not functional in the repetitive memory addressing mode. It is fully functional in all other operation modes.

sequential display areas begin. Note that DATA ROW END REGISTER (R12) is defined as SEQUENTIAL BREAK REGISTER 2 (R12) for the sequential addressing mode only. The starting addresses for these two additional display areas are defined by AUXILIARY ADDRESS REGISTER 1 (RE and RF) and AUXILIARY ADDRESS REGISTER 2 (R13 and R14). When the raster begins painting a data row equal to the number programmed in one of the sequential break registers, the CRT 9007 addresses the video memory sequentially starting with the address specified by the corresponding auxiliary address register. Figure 18 illustrates a display with 80 characters per data row having sequential breaks at data rows 3 and 6.

Using the sequential addressing mode with 2 breaks, it is possible to roll a portion of the screen and keep the rest of the screen stable. Double height/width characteristics can be attached to the 2 sequentially addressed screens defined by SEQUENTIAL BREAK REGISTERS 1 and 2 by using the 2 most significant bits of AUXILIARY ADDRESS REGISTERS 1 and 2. See the description of these 2 registers for their bit definition.

TABLE START REGISTER = 1000
AUXILIARY ADDRESS REGISTER 1 = 2000
AUXILIARY ADDRESS REGISTER 2 = 0800
SEQUENTIAL BREAK REGISTER 1 = 3
SEQUENTIAL BREAK REGISTER 2 = 6

Data Row	Address range	
0	1000 to 104 F	
1	1050 to 109F	
2	10A0 to 10EF	
3	2000 to 204F	(Break 1)
4	2050 to 209F	
5	20A0 to 20EF	
6	0800 to 084F	(Break 2)
7	0850 to 089F	
8	08A0 to 08EF	
	○	
	○	
	○	

Figure 18: Sequential Addressing Example With Two Breaks

B

Double Height/Width Operation

When double height/width characters (2XH/2XW) are displayed, the following will occur:

1. the CRT 9007 will address half as many characters for each data row by incrementing its address every other character clock.
2. the high speed video shift register supplying serial video to the CRT must shift out dots at half frequency.
3. For double height, the scan line counter outputs (SL3-SL0 or SLG, SLD) are incremented every other scan line.

The CRT 9007 is informed of the double height or double width display modes via the 2 most significant bits of the row table address or the 2 most significant bits of the AUXILIARY ADDRESS registers depending on the selected addressing mode. In any case, once the information is obtained by the CRT 9007, it must initiate the 3 tasks listed above. Tasks 1 and 3 are performed as appropriate and task 2 is performed using the CURS output of the CRT 9007 during CBLANK (horizontal retrace) to signal the external logic that a change in the dot shift frequency is required. The exact time of activation and deactivation of the CURS signal during horizontal retrace is a function of addressing mode, operation mode and actual scan line number to be painted. Tables 1 and 2 show the cursor activation and deactivation times as a function of the buffer configuration and addressing mode for the top scan line of a new data row. Tables 1 and 2 assume a cursor skew of zero. A cursor skew will effect the cursor position during trace as well as retrace time. For all subsequent scan lines, the CURS signal is activated 3 CCLK's after VLT trailing edge and stays active for exactly 1 CCLK assuming no cursor skew. When the cursor is placed on a double height or double width data row, it will become active for 2 CCLK's to allow the cursor to be displayed as double width. If the cursor position is programmed to reside in the top half of a double height data row, it may become active for all scan lines in both the current and next data row to allow the cursor to be displayed as double height.

For row driven addressing, a particular data row or pair of data rows can appear in one of the following ways as a function of the two most significant bits of the row table address (bits 15 and 14).

—Single height, single width (Row table address bits 15, 14 = 00). The CRT 9007 will display the particular data row as single height, single width.

—Single height, double width (Row table address bits 15, 14 = 01). The CRT 9007 will display the particular data row as single height double width by accessing half as many characters as appear in a single width data row. The CURS signal becomes active during horizontal retrace in the manner described previously.

—Double height, double width top half (Row table address bits 15, 14 = 10). In addition to providing the special timing associated with single height double width data rows, the scan line counter is started from zero and incremented every other scan line until N scan lines are painted (N is the number of scan lines per single height data row). In this way, new dot information appears every other scan line and the top half of the data row appears in N scan lines.

—Double Height, Double Width Bottom Half (Row table address bits 15, 14 = 11)—Same as Double Height, Double Width Top except the scan line counter is started from N/2 (or (N-1)/2 if N is odd), and incremented every other scan line until N scan lines are painted. In single row buffer operation, a double height bottom data row can only stand alone during a smooth scroll operation; otherwise it is assumed to follow a double height top data row.

OPERATION MODE	ADDRESSING MODE	
	Row Driven (linked list or contiguous)	Sequential
Repetitive Memory Addressing	1 CCLK after high byte of row table read	1 CCLK after TSC leading edge
Single row buffer	1 CCLK after high byte of row table read	1 CCLK after TSC leading edge
Double row buffer	1 CCLK after high byte of row table read	1 CCLK after ACK leading edge

Table 1: Double Height/Width CURS activation for top scan line of new data row.

OPERATION MODE	ADDRESSING MODE	
	Row driven (linked list or contiguous)	Sequential
Repetitive Memory Addressing	at the leading edge of VLT	at the leading edge of VLT
Single row buffer	at the leading edge of VLT	at the leading edge of VLT
Double row buffer	1 CCLK after leading edge of CURS	1 CCLK after leading edge of CURS

Table 2: Double Height/Width CURS deactivation for top scan line of new data row.

PROCESSOR ADDRESSABLE REGISTERS

All CRT 9007 registers are selected by specifying the address on VA5-0 and asserting $\overline{CS}$. All 14 bit registers are written or read as two consecutive 8 bit registers addressed low byte first. Only the VERTICAL CURSOR REGISTER and the HORIZONTAL CURSOR REGISTER are read/write registers with 2 different addresses for read or write operations. The register address assigned to each register represents the actual address in hexadecimal form that must appear on VA5-0. Figure 2 illustrates all processor to CRT 9007 register timing. Tables 3a, 3b, and 3c summarize all register bits and provide register addresses.

HORIZONTAL TIMING REGISTERS

The following 4 registers define the horizontal timing parameters. Figure 19 relates the horizontal timing to these registers.

CHARACTERS PER HORIZONTAL PERIOD (R0)

This 8 bit write only register, programmed in units of character times, represents the total number of characters in the horizontal period (trace plus retrace time). This register is programmed with the binary number N where N is the total characters in the horizontal period. The horizontal period should not be programmed for less than 12 characters.

CHARACTERS PER DATA ROW (R1)

This 8 bit write only register, programmed in units of character times, represents the number of displayable characters during the horizontal trace interval. The difference R0 minus R1 represents the number of character times reserved for horizontal retrace. This register is programmed with the binary number (N-1) where N is the displayable characters per data row.

HORIZONTAL DELAY (R2)

This 8 bit write only register, programmed in units of character times, represents the time between the leading edge of horizontal sync and leading edge of VLT. This register is programmed with N where N represents the time of horizontal delay. By programming this time greater than the horizontal blank interval, one can obtain negative front porch (horizontal sync begins before the horizontal blank interval).

HORIZONTAL SYNC WIDTH (R3)

This 8 bit write only register defines the horizontal sync width in units of character times. The start of the sync pulse is defined by the HORIZONTAL DELAY REGISTER and the end is independent of the start of the active display time. This register is programmed with N where N is the horizontal sync width. However this register must be programmed less than or equal to [(A/2)-1] where A is the programmed contents of REGISTER Ø rounded to the smallest even integer.

VERTICAL TIMING REGISTERS

The following 5 registers define the vertical timing parameters. Figure 20 relates the vertical timing to these registers.

VERTICAL SYNC WIDTH (R4)

This 8 bit write only register defines the vertical sync width in units of horizontal periods. The start of this signal is defined by the delay register (R5) and the end is independent of the start of the active display time. This register is programmed with N where N is the vertical SYNC width.

VERTICAL DELAY (R5)

This 8 bit write only register, programmed in units of horizontal periods, represents the time between the leading edge of vertical sync and the leading edge of the first VLT after the vertical retrace interval. This register is programmed with (N+1) where N represents the time of the vertical delay.

VISIBLE DATA ROWS PER FRAME (R7)

This 8 bit write only register defines the number of data rows displayed on the screen. This register is programmed with (N-1) where N is the number of data rows displayed.

SCAN LINES PER DATA ROW (R8)

The 5 LSBs of this write only register define the number of scan lines per data row. These 5 bits are programmed with (N-1) where N is the number of scan lines per data row. When programming for scan lines per data row greater than 16, only the serial scan line pin option (SLD, $\overline{SLG}$) can be used.

SCAN LINES PER VERTICAL PERIOD (R8; R9)

Registers R9 and the 3 most significant bits of R8 define the number of scan lines for the entire frame. R8 contains the 3 most significant bits of the 11 bit programmed value and R9 contains the 8 least significant bits of the 11 bit programmed value. The 11 bits are programmed with N where N is the number of scan lines per frame. In the 2 interlace modes, the programmed value represents the number of scan lines per field.

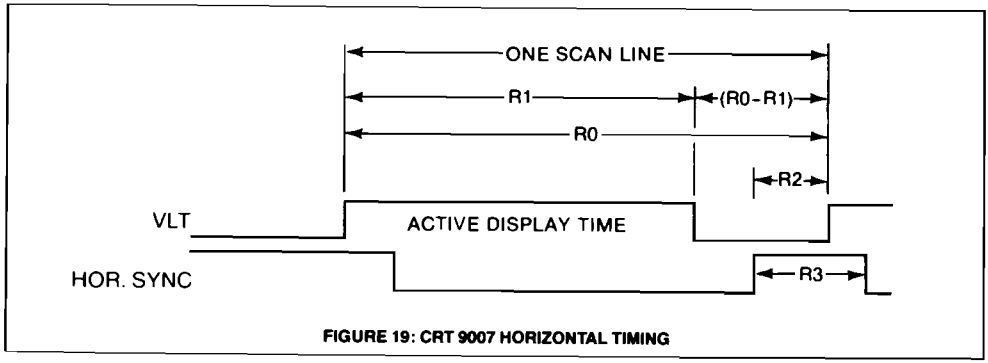


FIGURE 19: CRT 9007 HORIZONTAL TIMING

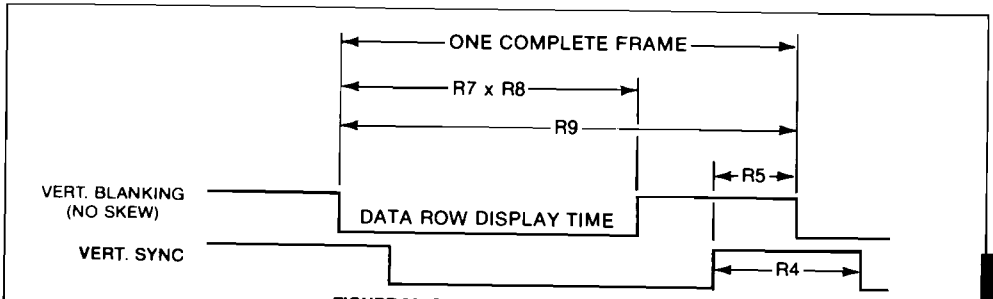


FIGURE 20: CRT 9007 VERTICAL TIMING

B

PIN CONFIGURATION/SKEW BITS REGISTER (R6)

This 8 bit write only register is used to select certain pin configurations and to skew (delay) the cursor and the blank signals independently with respect to the video signal sent to the monitor. The bits take on the following definition:

Bit 7, 6 (Pin Configuration)

These 2 bits, as illustrated in tables 4 and 5, define all pinout configurations as a function of double row buffer mode and non double row buffer mode. (The buffer mode is defined in the CONTROL REGISTER bits 3, 2, and 1.) The attribute assemble mode is assumed to be a double row buffer mode and obeys table 4.

Bits 5, 4, 3 (Cursor skew)

These three bits define the number of character clocks the cursor signal is skewed (delayed) from the VLT signal. The VLT signal is active for all characters within a data row and a non skewed cursor will always become active within the active VLT time at the designated position. The cursor can be skewed from 0 to 5 character clocks (Bits 5, 4 and 3 programmed from 000 to 101, bit 5 is the most significant bit; bit 3 is the least significant bit). For double height/width data rows, the cursor signal appearing during horizontal retrace is also skewed as programmed.

Bits 2, 1, 0 (Blank skew)

These three bits define the number of character clocks the horizontal blank component of the CBLANK signal is skewed (delayed) from the VLT signal. The edges of VLT will line up exactly with the edges of the horizontal component of the CBLANK signal if no skew is programmed. The CBLANK can be skewed from 0 to 5 character clocks (Bits 2, 1 and 0 programmed from 000 to 101, bit 2 is the most significant bit; bit 0 is the least significant bit).

SECTION V

REGISTER R6 BITS		CRT 9007 PIN NUMBER					
7	6	28	29	30	31	32	33
0	1	DMAR	WBEN	$\overline{SLG}$	SLD	$\overline{CSYNC}$	ACK
1	1	DMAR	WBEN	$\overline{SLG}$	SLD	LPSTB	ACK
0	0	NOT PERMITTED					
1	0	NOT PERMITTED					

Table 4: Pin configuration for double row buffer and attribute assemble modes.

REGISTER 6 BITS		CRT 9007 PIN NUMBER					
7	6	28	29	30	31	32	33
0	0	SL3	SL2	SL1	SL0	$\overline{CSYNC}$	$\overline{TSC}$
1	0	SL3	$\overline{SL2}$	SL1	SL0	LPSTB	$\overline{TSC}$
1	1	VBLANK	$\overline{CSYNC}$	$\overline{SLG}$	SLD	LPSTB	$\overline{TSC}$
0	1	NOT PERMITTED					

Table 5: Pin configuration for Single Row Buffer and Repetitive Memory Addressing Modes.

DMA CONTROL REGISTER (RA)

This 8 bit write only register allows the user to set up a DMA burst count and delay as well as disable the DMA mechanism of the CRT 9007. The register bits have the following definition:

Bit 7 (DMA Disable)

A logic one will immediately force the CRT 9007 DMA request to the inactive level and the CRT 9007 address bus (VA13-VA0) will enter its high impedance state. After enabling the DMA mechanism by setting this bit to a logic zero, a start command must be issued (see START COMMAND, R15).

Bits 6, 5, 4 (DMA Burst Delay)

These 3 bits define the number of clock delays ($\overline{CCLK}$) between successive DMAR–ACK sequences. Bit 6 is the most and bit 4 is the least significant bit respectively. When programmed with a number N, the CRT 9007 will delay for 4 (N + 1) clock cycles before initiating another DMA request. If 111 is programmed, however, this will result in a zero delay allowing all characters to be retrieved from video RAM in one DMA burst regardless of the value programmed for the DMA burst count.

Bits 3, 2, 1, 0 (DMA Burst Count)

These 4 bits define the number of DMA operations in one DMAR-ACK sequence. Bit 3 is the most and bit 0 is the least significant bit respectively. When programmed with a number N, the CRT 9007 will produce 4 (N + 1) DMA cycles before relinquishing the bus. When programmed with 0000, the minimum DMA Burst will occur ($4 \times 1 = 4$) and when programmed with 1111 the maximum DMA Burst will occur ($4 \times 16 = 64$). When bits 6, 5, and 4 are programmed with 111, no DMA delay will occur and the Burst count will equal the number of programmed characters per data row as specified in R1. Refer to figures 9 and 15 which illustrate a DMA burst of 16 and a DMA delay of 8 for double row buffer and attribute assemble modes respectively. For single row buffer operation, no DMA delay is permitted and bits 6, 5, 4 must be programmed with 000.

CONTROL REGISTER (RB)

This 7 bit write only register controls certain frame operations as well as specifying the operation mode used. Internal to the CRT 9007, this register is double buffered. Changes in the register are reflected into the CRT 9007 at a particular time during vertical retrace. This allows the user to update the CONTROL REGISTER at any time without running the risk of destroying the frame or field currently being painted.

The bits take on the following definition:

Bit 6 (PB/$\overline{SS}$)

= 0; The smooth scroll mechanism is enabled permitting the SMOOTH SCROLL OFFSET REGISTER (R17) to be loaded in the scan line counter (SL3-0 or SLG, SLD signals) allowing for a scroll on the screen of a predetermined number of scan lines per frame or field. The starting and ending of the smooth scroll operation is defined by the DATA ROW START REGISTER (R11) and DATA ROW END REGISTER (R12) respectively.

= 1; The page blank mechanism is enabled. The CBLANK signal is made active high for a continuous period of time starting and ending at the data row defined by the DATA ROW START REGISTER (R11) and DATA ROW END REGISTER (R12) respectively.

Bits 5, 4 (Interlace)—these 2 bits define one of 3 displayed modes as illustrated in figure 21

= 00; Non interlaced display

= 10; Enhanced video interlace. This display mode will produce an interlaced frame with the same dot information painted in adjacent odd/even scan lines.

= 11; Normal video interlace. This display mode will produce an interlaced frame with odd scan lines of characters displayed in odd fields and even scan lines displayed in even fields. This mode can be used to allow the screen to show twice as many data rows at half the height since it effectively doubles the character density on the screen.

= 01; This combination is not permitted.

Bits 3, 2, 1 (Operation modes): These 3 bits define the various buffer configuration modes as follows:

= 000; (Repetitive memory addressing)—In this mode the address information (VA13-VA0) appears during every visible scan line and the address bus enters its high impedance state during all retrace intervals. When using a row driven addressing mode (linked list or contiguous), the address bus is in the high impedance state for all retrace intervals except the horizontal retrace interval prior to the top scan line of a new data row. This period can be distinguished from other retrace intervals because the DRB (data row boundary) signal is active.

= 001; (Double row buffer)—In this mode, the CRT 9007 will address a particular data row from video memory one data row prior to the time when it is displayed on the CRT. During vertical retrace, the first data row is retrieved and loaded into the double row buffer. At the next data row boundary (in this case at the end of vertical retrace), the first data row feeds the character generator while the second data row is retrieved from video memory. The address bus will enter its high impedance state in accordance with the DMA mechanism for address bus arbitration.

= 100; (Single row buffer)—In this mode, during the first scan line of each data row, the CRT 9007 will address video memory, load the buffer and feed the character generator at the painting rate of the CRT. If the CRT 9007 is used in a row driven addressing mode, it will drive the address bus during the retrace period prior to the first scan line of each data row in order to retrieve the row table address. It will automatically enter the high impedance state at the end of the first visible scan line of each data row. If the CRT 9007 is used in a sequential addressing mode, it will drive the address bus only during the visible line time of the first scan line of each data row.

= 111; (Attribute assemble)—In the attribute assemble mode, character data and attribute data are shared in consecutive alternating byte locations in memory. When the CRT 9007 reads an attribute byte, it loads it into its internal attribute latch. During the next memory access, a character byte is fetched. At this time the CRT 9007 isolates its bus from the main system bus and outputs the previously latched attribute. A WBEN signal is produced during every character byte fetch to allow the character and its associated attribute to be simultaneously latched into two double row buffers. This mode assumes that there exists twice as many byte locations as there are displayable character positions on the CRT. The first byte of every data row is assumed to be an attribute.

All other combinations of the CONTROL REGISTER bits 3, 2, 1 are not permitted.

Bit 0 ($\overline{2XC}$/1XC): This bit allows for either single or double height cursor display when the cursor is placed within a double height data row as follows:

= 1; (Single height cursor)—The CURS signal will appear during every scan line for single height data rows and will appear only during the top half or bottom half of a double height data row depending upon where the VERTICAL CURSOR REGISTER (R18, R38) defines the CURSOR data row.

= 0; (Double height cursor)—If the VERTICAL CURSOR REGISTER (R18, R38) places the cursor in the top half of a double height data row, the CURS signal will appear during every scan line of the top half (the current data row) and the bottom half (the next data row) of the double height data row. If the cursor is placed in the bottom half of a double height data row or if it is placed in a single height data row, the CURS signal will only appear during the one particular data row.

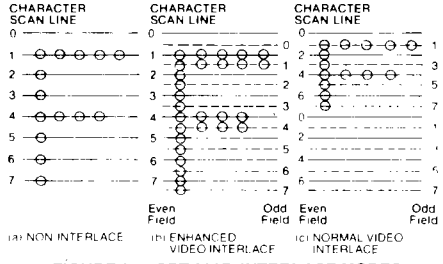


FIGURE 21: CRT 9007 INTERLACE MODES

TABLE START REGISTER (RC AND RD)

This 16 bit write only register contains a 14 bit address which is used in a variety of ways depending on the addressing mode chosen; the 2 remaining bits define the addressing mode. Register C contains the lower 8 bits of the 14 bit address. The 6 least significant bits of register D contain the upper 6 bits of the 14 bit address. The 2 most significant bits of register D define four addressing modes as follows:

„Register D bits 7, 6:

= 00; (Sequential addressing mode)—The CRT 9007 will address video memory in a sequential fashion starting with the 14 bit address contained in REGISTER D bits 5-0 and REGISTER C bits 7-0. 2 sequential breaks are allowed as defined by SEQUENTIAL BREAK 1 (R10) using AUXILIARY ADDRESS REGISTER 1 (RE and RF) and SEQUENTIAL BREAK 2 (R12) using AUXILIARY ADDRESS REGISTER 2 (R13 and R14).

= 01; (Sequential roll addressing mode)—The CRT 9007 will address video memory in a sequential fashion starting with the 14 bit address contained in REGISTER D bits 5-0 and REGISTER C bits 7-0. SEQUENTIAL BREAK REGISTER 1 and AUXILIARY ADDRESS REGISTER 1 can be used to cause one sequential break as described in the sequential addressing mode. A second break in the sequential addressing can be defined by SEQUENTIAL BREAK REGISTER 2 (R12) and AUXILIARY ADDRESS REGISTER 2 (R13 and R14) permitting up to 3 separate sequentially addressed screens to be painted.

= 10; (Contiguous row table mode)—The CRT 9007 will address video memory according to the contiguous row table format. The 14 address bits contained in REGISTER D bits 5-0 and REGISTER C bits 7-0 define an address that points to the beginning of the contiguous row table.

= 11; (Linked list row table mode)—The CRT 9007 will address video memory according to the linked list row table format. The 14 address bits contained in REGISTER D bits 5-0 and REGISTER C bits 7-0 define the address at which the second row table entry and the first data row reside.

AUXILIARY ADDRESS REGISTER 1 (RE and RF)

This 16 bit write only register contains a 14 bit address. The 6 least significant bits of REGISTER F contain the upper order 6 bits of the 14 bit address and REGISTER E contains the 8 lower order bits of the 14 bit address. When the current data row equals the value programmed in SEQUENTIAL BREAK REGISTER 1 (R10) the remainder of the screen is addressed sequentially starting at the 14 bit address specified in this register. This sequential break overrides any row driven addressing mode used prior to the sequential break.

The 2 most significant bits of REGISTER F allow one to attach double height and/or double width characteristics to every data row in this sequentially addressed area in the following way:

For Double row buffer or attribute assemble mode REGISTER F Bits 7, 6

= 00; single height single width

= 01; single height double width

= 10; even data rows are double height double width top half odd data rows are double height double width bottom half

= 11; odd data rows are double height double width top half even data rows are double height double width bottom half

For Single row buffer or repetitive memory addressing mode REGISTER F Bits 7, 6

= 00; single height single width

= 01; single height double width

= 10; odd data rows are double height double width top half even data rows are double height double width bottom half

= 11; even data rows are double height double width top half
odd data rows are double height double width bottom half

B

SECTION V

SEQUENTIAL BREAK REGISTER 1 (R10)

This 8 bit write only register defines the data row number in which a new sequential video address begins as specified by AUXILIARY ADDRESS REGISTER 1 (RE and RF). To disable the use of this break, the register should be loaded with a data row count greater than the number of displayable data rows on the screen.

DATA ROW START REGISTER (R11)

This 8 bit write only register defines the first data row number at which a page blank or smooth scroll operation will begin. Bit 6 of the CONTROL REGISTER determines if a page blank or smooth scroll operation will occur.

DATA ROW END/SEQUENTIAL BREAK REGISTER 2 (R12)

This 8 bit write only register has a dual function depending on the addressing mode used. For row driven addressing (contiguous or linked list as specified by the 2 most significant bits of the TABLE START REGISTER) this register defines the data row number which ends either a page blank or smooth scroll operation. The row numerically one less than the row defined by this register is the last data row on which the page blank or smooth scroll will occur. To use the page blank feature to blank a portion of the screen that includes the last displayed data row, this register must be programmed to zero. For sequential addressing, this register can cause a break in the sequential addressing at the data row number specified and a new sequential addressing sequence begins at the address contained in AUXILIARY ADDRESS REGISTER 2.

AUXILIARY ADDRESS REGISTER 2 (R13 and R14)

This 16 bit write only register contains a 14 bit address. The 6 least significant bits of REGISTER 14 contain the upper order 6 bits of the 14 bit address and REGISTER 13 contains the 8 lower order bits of the 14 bit address. In the row driven addressing mode, this register is automatically loaded by the CRT 9007 with the current table address. The two most significant bits of REGISTER 14 specify one of four combinations of row attributes (for example double height

double width) on a row by row basis. Refer to the section entitled Double Height/Double Width operation for the meaning of these 2 bits. In the sequential addressing mode, this register can be loaded by the processor with a 14 bit address and a 2 bit row attributes field. The bit positions are identical for the row driven addressing mode. When the current data row equals the value programmed in DATA ROW END/SEQUENTIAL BREAK REGISTER 2 (R12), the remainder of the screen is addressed sequentially starting at the location specified by the programmed 14 bit address. The 2 most significant bits of register 14 allow one to attach double height and or double width characteristics to every data row in this sequentially addressed area. The bit definitions take on the same meaning as the 2 most significant bits of AUXILIARY ADDRESS REGISTER 1 and affect the display in an identical manner.

START COMMAND (R15)

After all vital screen parameters are loaded, a START command can be initiated by addressing this dummy register location within the CRT 9007. A START command must be issued after the DMA mechanism is enabled (DMA CONTROL REGISTER bit 7).

RESET COMMAND (R16)

The CRT 9007 can be reset via software by addressing this dummy location. Activation of the RST input pin or initiating this software command will effect the CRT 9007 in an identical manner. The reset state of the CRT 9007 is defined as follows:

CRT 9007 outputs	Reset state
VA13-0	High impedance
VD7-0	High impedance
$\overline{HS}$	High
$\overline{VS}$	High
CBLANK	High
CURS	Low
$\overline{VLT}$	Low
$\overline{DRB}$	High
$\overline{INT}$	Low
Pin 28	Low
Pin 29	Low
Pin 30	Low
Pin 31	Low
Pin 32	Low

SMOOTH SCROLL OFFSET REGISTER (R17)

This register is loaded with the scan line offset number to allow a smooth scroll operation to occur. The offset register causes the scan line counter output of the CRT 9007 to start at the programmed value rather than zero for the data row that starts the smooth scroll interval. The start is specified in the DATA ROW START REGISTER (R11). Typically, this register is updated every frame and it ranges from zero (no offset) to a maximum of the programmed scan lines per data row (maximum offset). For example, if 12 scan lines per data row are programmed (scan line 0 to scan line 11) an offset of zero will cause an unscrolled display. An offset of one will cause a display starting at scan line 1 and ending at scan line 11 (eleven scan lines total). An offset of eleven will cause a display starting at scan line eleven.

The next scan line will be zero, starting the subsequent data row. To allow smooth scroll of double height rows, the programmed range of the register is from zero to twice the programmed scan lines per data row. Whenever the offset register if greater than the programmed scan lines per data row, bit 7 of the register must be set to a logic 1 (offset overflow). It must be set to a logic zero at all other times. The 6 bit offset value occupies bits 6 through 1. Bit 0 must always be programmed with a logic zero. By setting the offset overflow (bit 7) to a logic 1, it is possible to have the bottom half of a double height data row stand alone in Single Row Buffer Mode by programming the scrolled data row as double height top half and loading R17 with the proper value.

VERTICAL CURSOR REGISTER (R18 or R38)

This 8 bit read/write register specifies the data row in which the cursor appears. To write into this register it is addressed as R18 and to read from this register it is addressed as R38.

HORIZONTAL CURSOR REGISTER (R19 or R39)

This 8 bit read/write register specifies the character position in which the cursor appears. To write into this register it is addressed as R19 and to read from this register it is addressed as R39.

It should be noted that the vertical and horizontal cursor is programmed in an X-Y format with respect to the screen and not dependant upon a particular location in video memory. The cursor will remain stationary during all scroll operations.

INTERRUPT ENABLE REGISTER (R1A)

This 3 bit write only register allows each of the three CRT 9007 interrupt conditions to be individually enabled or disabled according to the following definition:

Bit 6 (Vertical retrace interrupt)—This bit, when set to a logic one, will cause the CRT 9007 to activate the INT signal when a vertical retrace (i.e., the start of the vertical blanking interval) begins.

Bit 5 (Light pen interrupt)—This bit, when set to a logic one, will cause the CRT 9007 to activate the INT signal when the LIGHT PEN REGISTER (R3B, R3C) captures an X-Y coordinate. This interrupt, which occurs at the beginning of vertical retrace, reflects the occurrence of a LPSTB input on the frame or field just painted. This interrupt need not be enabled when other CRT 9007 interrupt conditions are enabled since the STATUS REGISTER (R3A) will flag the occurance of a light pen update and servicing can be done off of other interrupts.

Bit 0 (Frame timer)—This bit, when set to a logic one, allows the CRT 9007 to activate the INT signal once every frame or field at a time when a potential smooth scroll update may occur. In this way the user can use the frame timer interrupt as both a real time clock and can service smooth scroll updates and other frame oriented operations by using the appropriate status bits. This interrupt will occur after the last row table entry is read by the CRT 9007. In single row buffer operation, this will occur one data row before the start of vertical retrace. In double row buffer operation, this will occur two data rows before the start of vertical retrace.

STATUS REGISTER (R3A)

This 5 bit register flags the various conditions that can potentially cause an interrupt regardless of whether the corresponding condition is enabled for interrupt. In this way some or all of the conditions can be reported to the processor via the STATUS REGISTER. If some of the conditions are enabled for interrupt, the processor, in response to an interrupt, simply has to read the STATUS REGISTER to determine the cause of the interrupt. The bit definition of the STATUS REGISTER is as follows:

Bit 7 (Interrupt Pending)—This bit will set when any other status bit, having its corresponding interrupt enabled, experiences a 0 to 1 transition. In this manner, when the processor services a potential CRT 9007 interrupt, it only has to test the interrupt pending bit to determine if the CRT 9007 caused the interrupt. If it did, the individual bits can then be tested to determine the details of the CRT 9007 interrupt. Any noninterruptable status change (corresponding interrupt enable bit reset to a logic 0) will not be reflected in the interrupt pending bit and must be polled by

the processor in order to provide service. The interrupt pending bit is reset when the status register is read. All other bits except Light Pen Update are reset to a logic 0 at the end of the vertical retrace interval. The light pen update bit is reset to a logic 0 when the HORIZONTAL LIGHT PEN REGISTER is read.

Bit 6 (Vertical Retrace)—A logic 1 indicates that a vertical retrace interval has begun.

Bit 5 (Light Pen Update)—A logic 1 indicates that a new coordinate has been strobed into the LIGHT PEN REGISTER. It is reset to a logic zero when the HORIZONTAL LIGHT PEN REGISTER is read. The light pen coordinates may have to be modified via software depending on light pen characteristics.

Bit 2 (odd/even)—For a normal video interlaced display, this bit is a logic 1 when the field about be painted is an odd field and is a logic zero when the field about be painted is an even field.

Bit 0 (Frame timer occurred)—This bit becomes a logic 1 either one or two data rows before the start of vertical retrace. Since this bit is set when the CRT has finished reading the row table for the frame or field just painted, it permits row table manipulation to start at the earliest possible time.

VERTICAL LIGHT PEN REGISTER (R3B)

This 8 bit read only register contains the vertical coordinate captured at the time the CRT 9007 received a light pen strobe signal (LPSTB).

HORIZONTAL LIGHT PEN REGISTER (R3C)

This 8 bit read only register contains the horizontal coordinate captured at the time the CRT 9007 received a light pen strobe signal. When a coordinate is captured, the appropriate status bit is set and further transitions on LPSTB are ignored until this register is read. The reading of this register will reset the light pen status bit in the STATUS REGISTER. The captured coordinate may have to be modified in software to allow for light pen response.

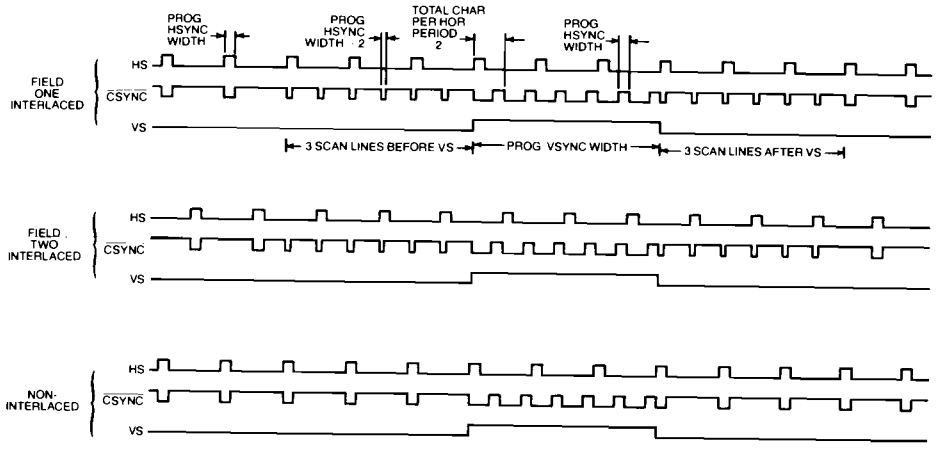


FIGURE 3: TYPICAL SYNC WAVEFORMS FOR INTERLACED AND NON-INTERLACED MODES

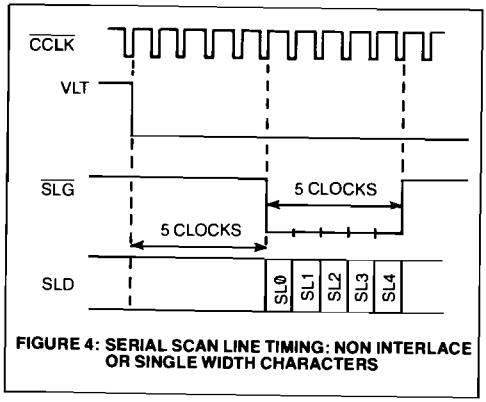


FIGURE 4: SERIAL SCAN LINE TIMING: NON INTERLACE OR SINGLE WIDTH CHARACTERS

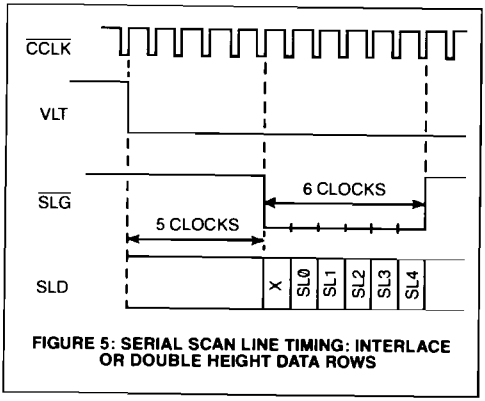


FIGURE 5: SERIAL SCAN LINE TIMING: INTERLACE OR DOUBLE HEIGHT DATA ROWS

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0° to + 70°C
Storage Temperature Range ..... − 55°C to + 150°C
Lead Temperature (soldering, 10 sec.) ..... + 325°C
Positive Voltage on any Pin, with respect to ground ..... + 8V
Negative Voltage on any Pin, with respect to ground ..... − 0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

DC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$

	PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
	Input voltage					
V_{IL}	Low			0.8	V	
V_{IH1}	High	2.0			V	all inputs except $\overline{CCLK}$
V_{IH2}	High	4.3			V	$\overline{CCLK}$ input; see note 4
	Output voltage					
V_{OL}	Low			0.4	V	I_{OL} = 1.6 mA
V_{OH}	High	2.4			V	I_{OH} = 100μA
	Input leakage current					
I_{L1}				10	μA	$0 \leq V_{IN} \leq 3.5V$; excluding $\overline{CCLK}$
I_{L2}				50	μA	V_{IN} = 5V; for $\overline{CCLK}$
I_{L3}				− 200	μA	V_{IN} = 0V; for $\overline{CCLK}$
	Input capacitance					
C_{IN1}			10	15	pF	all inputs except $\overline{CCLK}$ at 1 MHZ
C_{IN2}			25	50	pF [4]	$\overline{CCLK}$ input at 1 MHZ
	Power supply current					
I_{CC}			100	170	mA	

AC ELECTRICAL CHARACTERISTICS[3] $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$

	PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
	Clock					
t_{CY}	clock period	330		1200	ns	for double row buffer or attribute assemble
		300		1200	ns	for all other operation modes
t_{CKL}	clock low	90			ns	
t_{CKH}	clock high	150			ns	
t_{CKR}	clock rise time			15	ns	measured from 0.8V to 3.5V level
t_{CKF}	clock fall time			10	ns	measured from 90% to 10% points
	Output delay[1]					
t_{D1}				150	ns	
t_{D2}				150	ns	
t_{D3}				150	ns	
t_{D4}				150	ns	
t_{VA}		25		115	ns	measured to the 2.3V or 0.5V level on VA13-VA0
t_{DSL}				500	ns	
t_{DS}				185	ns	
t_{D6}				185	ns	
t_{DSY}				185	ns	
t_{VDS}		50			ns	valid for loading auxiliary address register 2 or the attribute latch
t_{VDH}		10			ns	
t_{VDO}				185	ns	C_L = 50pF
t_{SLG}				185	ns	
t_{SLD}				185	ns	
t_{D7}				240	ns	cursor skew of zero
t_{D7}				185	ns	cursor skew of one through five
t_{D8}				300	ns	
	Processor Read/write[2]					
t_{AS}		110			ns	
t_{AH}		0			ns	
t_{PW}		165			ns	
t_{CSH}		650			ns	
t_{PDS}		100			ns	
t_{PDH}		0			ns	
t_{PDA}				140	ns	
t_{PDO}		10		85	ns	
t_{IRR}				400	ns	
	Miscellaneous timing					
t_{ATS}		25		115	ns	measured from the 0.4V level of ACK or TSC falling edge
t_{RW}		$4t_{CY}$			ns	measured from the 0.4V level falling edge to 0.4V level rising edge
t_{AKW}		50			ns	see figure 24
t_{AKS}		50			ns	see figure 24

NOTE:
1. Timing measured from the 1.5V level of the rising edge of $\overline{CCLK}$ to the 2.4V (high) or 0.4V (low) voltage level of the ouput unless otherwise noted.
2. Reference points are 2.4V high and 0.4V low.
3. Loading on all outputs is 30 pF except where noted.
4. This level must be reached before the next falling edge of $\overline{CCLK}$.

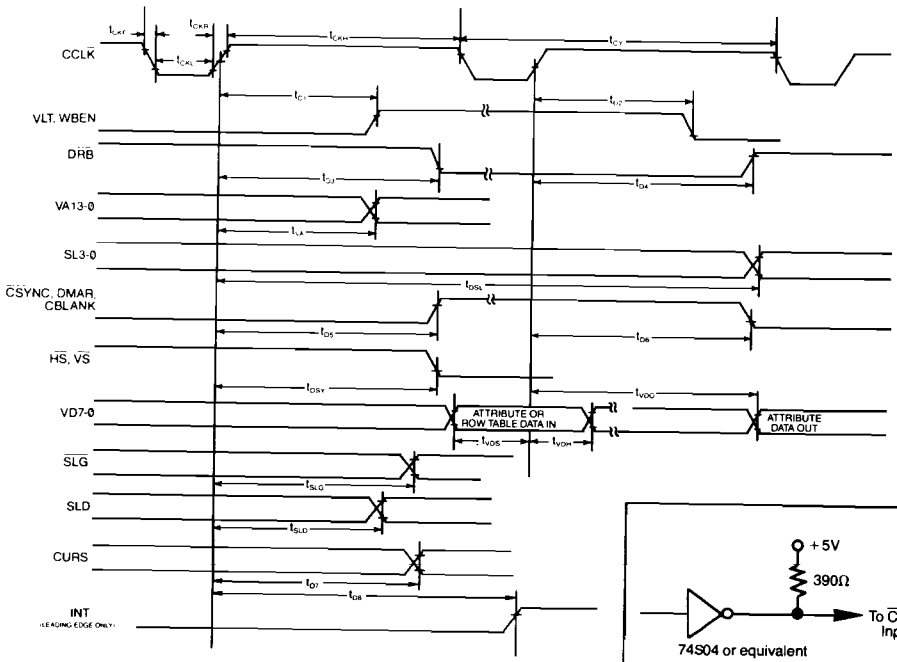


FIGURE 22: CRT 9007 TIMING PARAMETERS: OUTPUT SIGNALS

FIGURE 25: RECOMMENDED CCLK DRIVER CIRCUIT

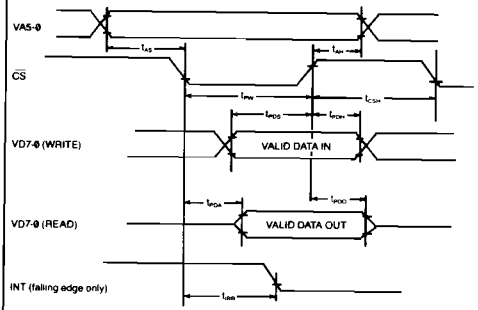
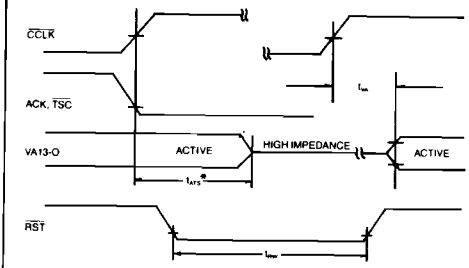


FIGURE 2: CRT 9007 PROCESSOR READ AND WRITE TIMING PARAMETERS



* t_{AFS} is controlled directly from ACK or TSC or from the particular CCLK that ends a DMA burst cycle

FIGURE 23: CRT 9007 MISCELLANEOUS TIMING PARAMETERS

Register Type	ADDRESS DECODE VA5	VA4	VA3	VA2	VA1	VA0	BIT DEFINITION D7	D6	D5	D4	D3	D2	D1	D0	REGISTER NUMBER (HEX)
WRITE	0	0	0	0	0	0	MSB	CHARACTERS PER HORIZONTAL PERIOD						LSB	R0
WRITE	0	0	0	0	0	1	MSB	CHARACTERS PER DATA ROW						LSB	R1
WRITE	0	0	0	0	1	0	MSB	HORIZONTAL DELAY						LSB	R2
WRITE	0	0	0	0	1	1	MSB	HORIZONTAL SYNC WIDTH						LSB	R3
WRITE	0	0	0	1	0	0	MSB	VERTICAL SYNC WIDTH						LSB	R4
WRITE	0	0	0	1	0	1	MSB	VERTICAL DELAY						LSB	R5
WRITE	0	0	0	1	1	0	PIN CONFIG-URATION	CURSOR SKEW MSB		LSB	BLANK SKEW MSB			LSB	R6
WRITE	0	0	0	1	1	1	MSB	VISIBLE DATA ROWS PER FRAME						LSB	R7
WRITE	0	0	1	0	0	0	SCAN LINES FRAME (B10)	(B8)	MSB	SCAN LINES PER DATA ROW				LSB	R8
WRITE	0	0	1	0	0	1	(B7)	SCAN LINES PER FRAME						LSB (B0)	R9

Table 3a: CRT 9007 Screen Format Registers

Register Type	ADDRESS DECODE VA5	VA4	VA3	VA2	VA1	VA0	BIT DEFINITION D7	D6	D5	D4	D3	D2	D1	D0	REGISTER NUMBER (HEX)
WRITE	0	0	1	0	1	0	DMA DIS-ABLE	DMA BURST DELAY MSB	LSB		DMA BURST COUNT MSB			LSB	RA
WRITE	0	0	1	0	1	1	X	PB/SS	INTERLACE MODES		OPERATION MODES			XC/1XC	RB
WRITE	0	0	1	1	0	0	MSB	TABLE START REGISTER (LS BYTE)						LSB	RC
WRITE	0	0	1	1	0	1	ADDRESS MODE	TABLE STRT REGISTER (MS BYTE) MSB						LSB	RD
WRITE	0	0	1	1	1	0	MSB	AUXILIARY ADDRESS REGISTER 1 (LS BYTE)						LSB	RE
WRITE	0	0	1	1	1	1	ROW ATTRIBUTES	AUXILIARY ADDRESS REGISTER 1 (MS BYTE) MSB						LSB	RF
WRITE	0	1	0	0	0	0	MSB	SEQUENTIAL BREAK REGISTER 1						LSB	R10
WRITE	0	1	0	0	0	1	MSB	DATA ROW START REGISTER						LSB	R11
WRITE	0	1	0	0	1	0	MSB	DATA ROW END/SEQUENTIAL BREAK REGISTER 2						LSB	R12
WRITE	0	1	0	0	1	1	MSB	AUXILIARY ADDRESS REGISTER 2 (LS BYTE)						LSB	R13
WRITE	0	1	0	1	0	0	ROW ATTRIBUTES	AUXILIARY ADDRESS REGISTER 2 (MS BYTE) MSB						LSB	R14

Table 3b: Control and Memory Address Registers

Register Type	ADDRESS DECODE VA5	VA4	VA3	VA2	VA1	VA0	BIT DEFINITION D7	D6	D5	D4	D3	D2	D1	D0	REGISTER NUMBER (HEX)
READ OR WRITE	0	1	0	1	0	1	START COMMAND								R15
READ OR WRITE	0	1	0	1	1	0	RESET COMMAND								R16
WRITE	0	1	0	1	1	1	OFFSET OVER-FLOW	OFFSET VALUE MSB					LSB	0	R17
WRITE	0	1	1	0	0	0	MSB	VERTICAL CURSOR REGISTER (ROW COORD)						LSB	R18 or R38
READ	1	1	1	0	0	0									
WRITE	0	1	1	0	0	1	MSB	HORIZONTAL CURSOR REGISTER (COL COORD)						LSB	R19 or R39
READ	1	1	1	0	0	1									
WRITE	0	1	1	0	1	0	X	VER-TICAL RE-TRACE	LIGHT PEN	INTERRUPT ENABLE REGISTER X	X	X	X	FRAME TIMER	R1A
READ	1	1	1	0	1	0	INT PEND-ING	VER-TICAL RE-TRACE	LIGHT PEN	STATUS REGISTER		ODD/ EVEN	X	FRAME TIMER	R3A
READ	1	1	1	0	1	1	MSB	VERTICAL LIGHT PEN REGISTER (ROW COORD)						LSB	R3B
READ	1	1	1	1	0	0	MSB	HORIZONTAL LIGHT PEN REGISTER (COL COORD)						LSB	R3C

Table 3c: Cursor, Light Pen, Offset, and Status Registers

STANDARD MICROSYSTEMS CORPORATION

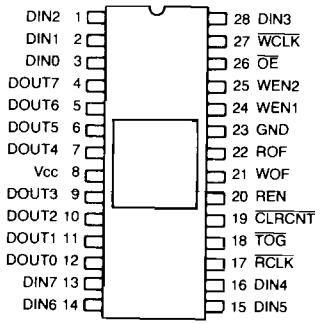
CRT 9212
μPC FAMILY

Double Row Buffer
DRB

FEATURES

- ☐ Low Cost Solution to CRT Memory Contention Problem
- ☐ Provides Enhanced Processor Throughput for CRT Display Systems
- ☐ Replaces Shift Registers or Several RAM and Counter IC's in CRT Display System
- ☐ Permits Display of One Data Row While Next Data Row is Being Loaded
- ☐ Data May be Written into Buffer at Less Than the Video Painting Rate
- ☐ Double Data Row Buffer Permits Second Data Row to be Loaded Anytime during the Display of the Preceding Data Row
- ☐ Permits Active Video on All Scan Lines of Data Row
- ☐ Dynamically Variable Number of Characters per Data Row—...64, 80, 132,...up to a Maximum of 135
- ☐ Cascadable for Data Rows Greater than 135 Characters
- ☐ Stackable for "Invisible Attributes" or Character Widths of Greater than 8 Bits

PIN CONFIGURATION



PACKAGE 28-pin D.I.P.

- ☐ Three-State Outputs
- ☐ Up to 4 MHz Read/Write Data Rate
- ☐ Compatible with SMC CRT 5037, CRT 9007, and other CRT Controllers
- ☐ 28 Pin Dual-In-Line Package
- ☐ +5 Volt Only Power Supply
- ☐ TTL Compatible

GENERAL DESCRIPTION

The CRT 9212 Double Row Buffer (DRB) provides a low cost solution to memory contention between the system processor and the CRT controller in video display systems.

The CRT 9212 DRB is a RAM-based buffer which provides two rows of buffering. It appears to the system as two octal shift registers of dynamically variable length (2-135 bytes) plus steering logic.

The CRT 9212 permits the loading of one data row while the previous data row is being displayed. The loading of data may take place during any of the scan line times of the data row. This relaxed time-constraint allows the processor to perform additional processing on the data or service other high priority interrupt conditions (such as a Floppy Disk DMA request) which may occur during a single video scan line. The result is enhanced processor throughput and flicker-free display of data.

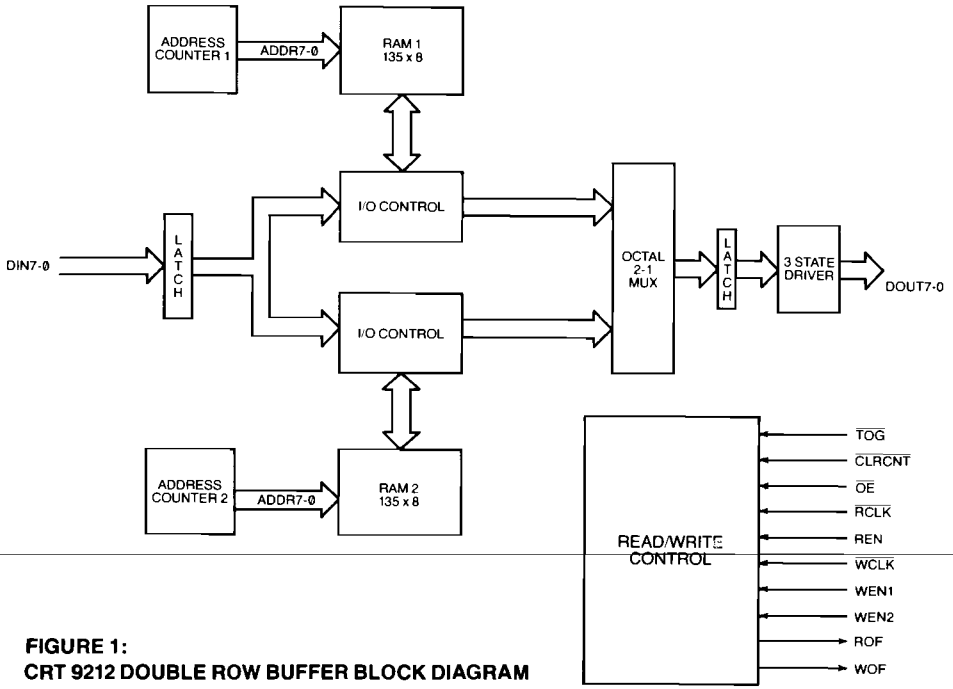


FIGURE 1:
CRT 9212 DOUBLE ROW BUFFER BLOCK DIAGRAM

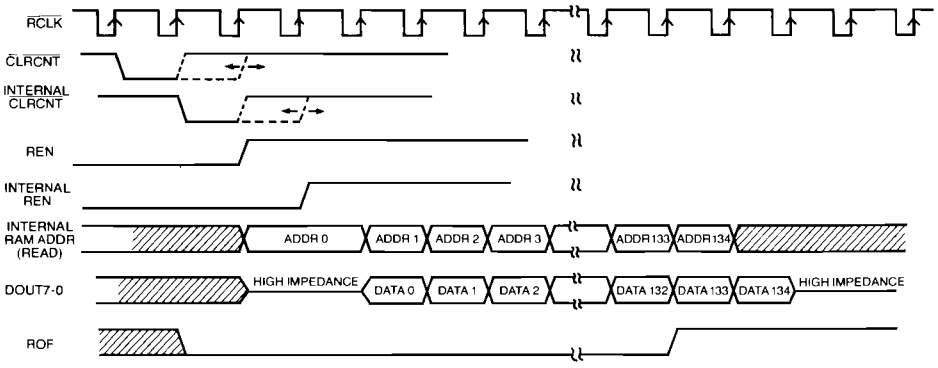


FIGURE 2: CRT 9212 DOUBLE ROW BUFFER READ TIMING

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
3-0, 28, 16-13	Data inputs	DIN0-DIN7	DIN0-DIN7 are the data inputs from the system memory.
12-9, 7-4	Data outputs	DOUT0-DOUT7	DOUT0-DOUT7 are the data outputs from the CRT 9212 internal data output latch. Valid information will appear on DOUT0-DOUT7 two $\overline{RCLK}$ periods after the rising edge of REN. This introduces two pipeline delays when supplying data to the character generator.
17	Read Clock	$\overline{RCLK}$	$\overline{RCLK}$ increments the current "read" address register. clocks data through the "read" buffer and moves data through the internal pipeline at the trailing edge.
18	Toggle Signal	$\overline{TOG}$	$\overline{TOG}$ alternates the function of each buffer between read and write. $\overline{TOG}$ normally occurs at every data row boundary. Switching of the buffers occurs when both $\overline{TOG}$ and CLRCNT are low.
19	Clear Counter	$\overline{CLRCNT}$	Clear Counter clears the current "read" address counter at the next $\overline{RCLK}$ positive edge. $\overline{CLRCNT}$ is normally asserted low at the beginning of each horizontal retrace interval. $\overline{CLRCNT}$ clears the current "write" address counter when the $\overline{TOG}$ is active.
20	Read Enable	REN	REN enables the loading of data from the selected "read" buffer into the output latch. Data is loaded when Read Clock is active.
21	Write Overflow	WOF	WOF high indicates that data is being written into the last memory position (position 135). When WOF is high, further writing into the selected "write" buffer is disabled. WOF may be connected to the WEN1 or WEN2 inputs of a second CRT 9212 for cascaded operation where data row lengths of greater than 135 characters are desired. See figure 4.
22	Read Overflow	ROF	The Read Overflow output is high when data is being read from the last memory position (position 135). ROF high disables further reading from the selected "read" buffer. ROF may be connected to the REN input of a second CRT 9212 for cascaded operation where data row lengths of greater than 135 characters are desired. DOUT0-7 will switch into a high impedance state at the second positive transition of $\overline{RCLK}$ after ROF goes high. See figure 4.
24; 25	Write Enable	WEN1, WEN 2	WEN allows input data to be written into the selected "write" buffer during $\overline{WCLK}$ active. Both WEN1 and WEN 2 must be high to enable writing. WEN1 has an internal pullup resistor allowing it to assume a high if pin 24 is left open.
26	Output Enable	$\overline{OE}$	When the $\overline{OE}$ input is low, the data outputs DOUT0-DOUT7 are enabled. When $\overline{OE}$ is high, DOUT0-DOUT7 present a high impedance state. $\overline{OE}$ has an internal pulldown resistor allowing it to assume a low if pin 26 is left open.
27	Write Clock	$\overline{WCLK}$	$\overline{WCLK}$ clocks input data into the selected "write" buffer and increments the current "write" address register when WEN1 and WEN2 are high.
8	Power Supply	V_{cc}	+ 5 Volt supply
23	Ground	GND	Ground

OPERATION

Figure 1 illustrates the internal architecture of the CRT 9212. It contains 135 bytes of RAM in each of its two buffers. In normal operation, data is written into the input latch on the positive-going edge of Write Clock ($\overline{WCLK}$). When both Write Enable (WEN1, WEN 2) signals go high, the next $\overline{WCLK}$ causes data from the input latch to be written into the selected buffer (1 or 2) and the associated address counter to be incremented by one. Loading of the selected RAM buffer continues until WEN goes inactive or until the buffer has been fully loaded. At the next data row boundary, the Toggle Signal ($\overline{TOG}$) will go low. When Clear Counter ($\overline{CLRCNT}$) goes low, the next Read Clock ($\overline{RCLK}$) will begin to reset both buffer address counters to zero, switching the buffer just loaded from a "write buffer" to a "read buffer", permitting the next row of data to be written into the other buffer. Data from the current "read" buffer is read out of the buffer and to the output latch whenever Read Enable (REN) is high during a Read Clock ($\overline{RCLK}$). Each read-out from the buffer RAM causes the "read" address counter to be incremented. REN is normally high during the entire visible line time of each scan line of the data row. $\overline{CLRCNT}$ resets the present "read" address counter. The negative edge of $\overline{CLRCNT}$ is detected by the CRT 9212 and the internal "read" address counter is cleared independent of the $\overline{CLRCNT}$ pulse width. The $\overline{CLRCNT}$ input may be tied to the REN input for proper operation.

Figures 2 and 3 illustrate the functional timing for reading and writing the CRT 9212. It is possible to cascade two or more CRT 9212's to allow for data storage greater than 135 bytes by employing the read overflow (ROF) and write overflow (WOF) outputs. Figure 4 illustrates two CRT 9212's cascaded together.

The CRT 9212 is compatible with the CRT 9007 video processor and controller (VPAC™) and the CRT 8002 video display attributes controller (VDAC™). A typical video configuration employing the three parts is illustrated in figure 5.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (soldering, 10 sec.)	+325°C
Positive Voltage on any Pin, with respect to ground	+8.0V
Negative Voltage on any Pin, with respect to ground	−0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ± 5%)

PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
DC CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low Level V_{IL}			0.8	V	
High Level V_{IH1}	2.0			V	excluding $\overline{RCLK}$; $\overline{WCLK}$
High Level V_{IH2}	4.2			V	$\overline{RCLK}$, $\overline{WCLK}$
OUTPUT VOLTAGE LEVELS					
Low Level V_{OL}			0.4	V	
High Level V_{OH}	2.4			V	
INPUT LEAKAGE CURRENT					
High Leakage I_{LH1}			10	µA	excluding $\overline{OE}$
Low Leakage I_{LL1}			10	µA	excluding WEN1
High Leakage I_{LH2}			400	µA	WEN1
Low Leakage I_{LL2}			400	µA	$\overline{OE}$
INPUT CAPACITANCE					
C_{IN1}		10		pF	excluding $\overline{RCLK}$, $\overline{WCLK}$
C_{IN2}		15		pF	$\overline{RCLK}$, $\overline{WCLK}$
POWER SUPPLY CURRENT					
I_{CC}		100		mA	

AC CHARACTERISTICS[1]

t_{CYW}	300			ns	Write clock period
t_{CYR}	300			ns	Read clock period
t_{CKH}	247		DC	ns	
t_{CKL}	33			ns	
t_{CKR}			10	ns	measured from 10% to 90% points
t_{CKF}			10	ns	measured from 90% to 10% points
t_{DS}	50			ns	referenced to $\overline{WCLK}$
t_{DH}	0			ns	referenced to $\overline{WCLK}$
t_{EN1}[2]	0			ns	
t_{EN2}[2]	100			ns	
t_{ENH}[2]	0			ns	
t_{DV}			175	ns	C_L = 50 pF; referenced from $\overline{RCLK}$
t_{DOFF}			175	ns	
t_{DON}			175	ns	
t_{OF}[3]			175	ns	C_L = 30 pF
t_{CS}	100			ns	
t_{CH}	0			ns	
t_{WT}[4]		$1t_{CYW}$			

1 - Reference points for all AC parameters are 2.4V high and 0.4V low.
2 - For REN, referenced from $\overline{RCLK}$; for WEN1 or WEN2 referenced to $\overline{WCLK}$.
3 - For ROF, referenced from $\overline{RCLK}$; for WOF referenced from $\overline{WCLK}$.
4 - At least 1 WCLK rising edge must occur between $\overline{CLRCNT}$ or $\overline{TOG}$ (whichever occurs last) and WEN (= WEN1-WEN2).

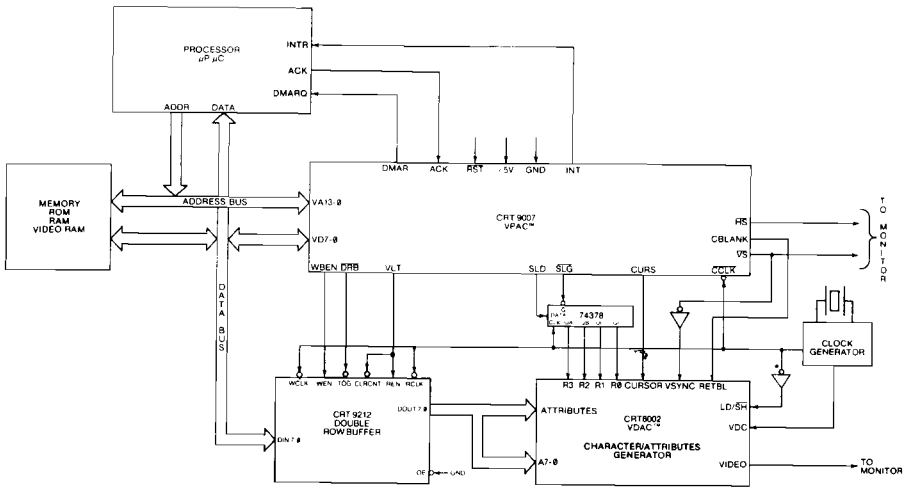


FIGURE 5: CRT 9212 CONFIGURED WITH THE CRT 9007 VPAC AND THE CRT 8002 VDAC™

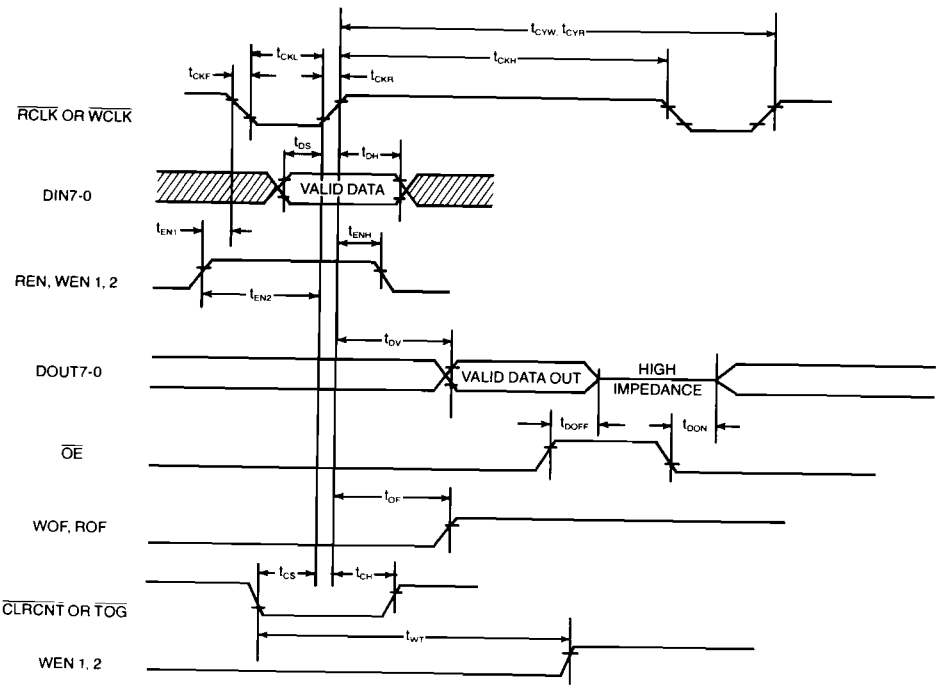
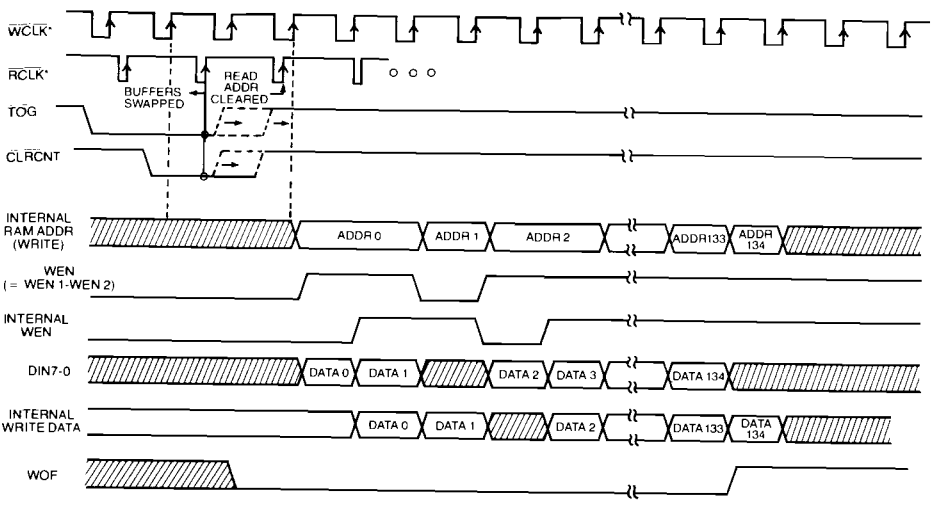


FIGURE 6: CRT 9212 I/O TIMING



* in general WCLK and RCLK can be different

FIGURE 3: CRT 9212 DOUBLE ROW BUFFER WRITE TIMING

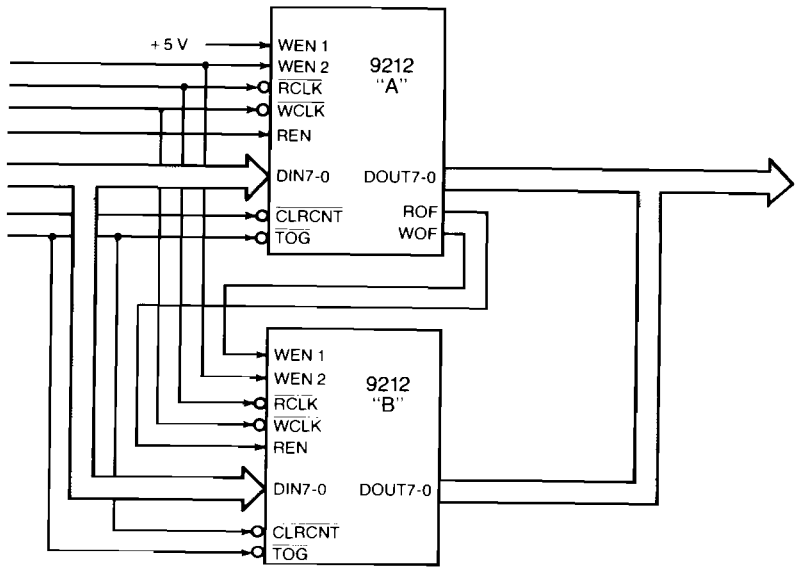


FIGURE 4: CRT 9212 CASCADED CONFIGURATION FOR DATA ROW LENGTHS UP TO 270 CHARACTERS

STANDARD MICROSYSTEMS CORPORATION

CRT 9021A
CRT 9021B
µPC FAMILY

CRT Video Attributes Controller VAC

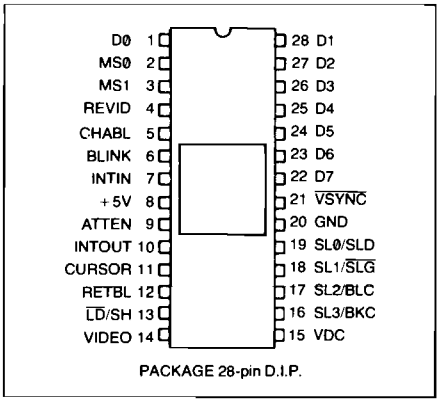
B

SECTION V

FEATURES

- ☐ On chip video shift register
  Maximum shift register frequency
  CRT 9021A 30 MHz
  CRT 9021B 28.5 MHz
- ☐ On chip attributes logic
  Reverse video
  Character blank
  Character blink
  Underline
  Full/half intensity
- ☐ Four modes of operation
  Wide graphics
  Thin graphics
  Character mode without underline
  Character mode with underline
- ☐ On Chip logic for double height/double width characters
- ☐ Accepts scan line information in parallel or serial format
- ☐ Four cursor modes dynamically selectable via 2 input pins
  Underline
  Blinking underline
  Reverse video
  Blinking reverse video
- ☐ Programmable character blink rate
- ☐ Programmable cursor blink rate
- ☐ On chip data and attribute latches
- ☐ +5 volt operation
- ☐ TTL compatible
- ☐ MOS n-Channel silicon gate COPLAMOS® process
- ☐ Compatible with CRT 5037 VTAC®; CRT 9007 VPAC™

PIN CONFIGURATION



PACKAGE 28-pin D.I.P.

GENERAL DESCRIPTION

The SMC CRT 9021 Video Attributes Controller (VAC) is an n-channel COPLAMOS MOS/LSI device containing Graphics logic, attributes logic, data and attributes latches, cursor control, and a high speed video shift register. The CRT 9021, a character generator ROM and a CRT controller such as the CRT 9007 provide all of the major circuitry for the display portion of a CRT video terminal.

The CRT 9021 serial video output may be connected directly to a CRT monitor's video input. The maximum video shift register frequency of 28.5 MHz or 30 MHz allows for CRT displays of up to 132 characters per data row.

The CRT 9021 attributes include: reverse video, underline, character blank, character blink, and full/half intensity selection. In addition, when used in conjunction with the CRT 9007 VPAC,™ the CRT 9021 will provide double height or double width characters.

Four programmable cursor modes are provided on the CRT 9021. They are: underline, blinking underline, reverse video character block, and blinking reverse video character block. When used in the serial scan line input mode, the cursor mode may be selected via two input pins. When used in the parallel scan line input mode, the cursor mode is a mask program option and is fixed at the time of manufacture.

Two graphics modes are provided. In the wide graphics mode, the CRT 9021 produces a graphic entity the size of the character block. The graphic entity contains eight parts, each of which is associated with one bit of the input byte, thereby providing 256 unique graphic symbols. The thin graphics mode enables the user to create thin line drawings and forms.

In both graphics modes, continuous horizontal and vertical lines may be drawn. Additional flexibility is provided by allowing the mask programming of the placement and dimensions of the blocks of lines within a character block. In the thin graphics mode, mask programming allows serrated horizontal or vertical lines.

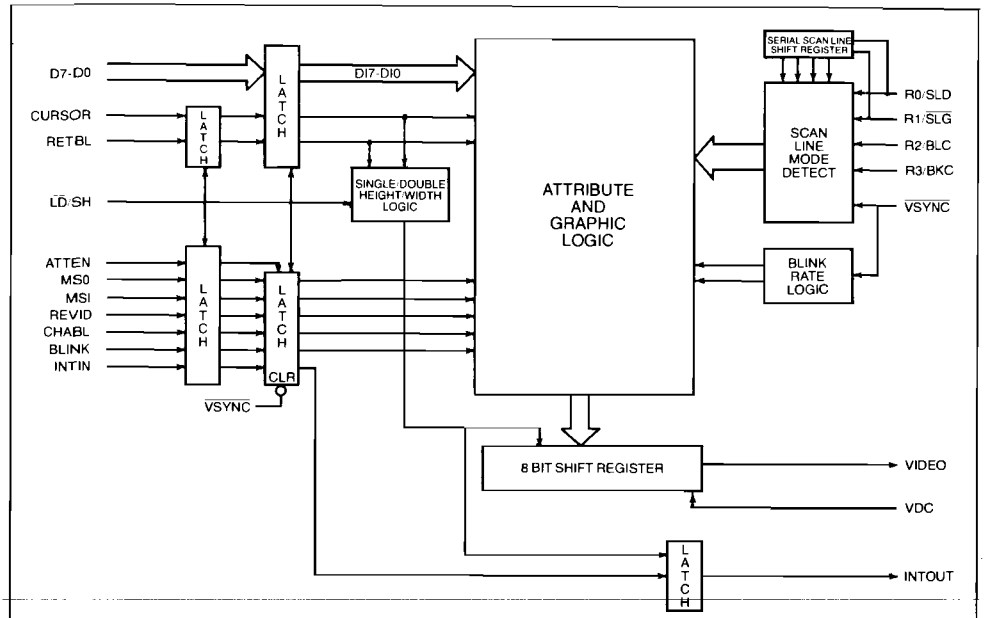


FIGURE 1: CRT 9021 BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
1, 28, 27, 26, 25, 24, 23, 22	Data	D7-D0	In the character mode, the data on these inputs is passed through the Attributes logic into the 8 bit high speed video shift register. The binary information on D7 will be the first bit output after the LD/SH input goes low. In the thin or wide graphics mode these 8 inputs will individually control the on/off condition of the particular portion of the character block or line drawing. Figures 2 and 3 illustrate the wide and thin graphics modes respectively and their relationships to D7-D0
2 3	Mode Select Ø Mode Select 1	MS0 MS1	These 2 inputs define the four modes of operation of the CRT 9021 as follows: MS1, MS0 = 00; Wide graphics mode = 10; Thin graphics mode = 01; Character mode without underline = 11; Character mode with underline See section entitled Display Modes for details.
4	Reverse Video	REVID	When this input and Retrace Blank (RETBL) are both low, data from the Attributes and Graphics logic is presented directly to the video shift register. When this input is high and RETBL is low, the Attribute and Graphics logic will invert the data before presenting it to the video shift register.
5	Character blank	CHABL	When this input is high, the parallel inputs to the video shift register are all set low (or high depending on the state of REVID) thus providing a constant video level for the entire length of the character block.
6	Blink	BLINK	When this input is high and both the RETBL and CHABL inputs are low, the character will blink at the programmed character blink rate. Blinking is accomplished by causing the video to go to the background level during the "off" portion of the Character Blink cycle. This video level may be either the white or black level depending on state of REVID. The duty cycle for the character blink is 75/25 (on/off). This input is ignored if it coincides with the CURSOR input and the cursor is formatted to blink.
7	Intensity In	INTIN	The INTIN input along with the INTOUT output provides a user controlled general purpose attribute. Data input to INTIN will appear at INTOUT with the same delay as that from any other attribute input to the serial video output (VIDEO). By using an external mixing circuit, it is possible to raise or lower the voltage level of the video output to produce such attributes as "half intensity" or "intensity".

DESCRIPTION OF PIN FUNCTIONS CONT'D

PIN NO.	NAME	SYMBOL	FUNCTION
8	Supply Voltage	+5V	+5 volt power supply
9	Attribute Enable	ATTEN	When this input is high, the internal attribute latch is updated at the positive going edge of the LD/SH input with data appearing on the REVID, CHABL, MS1, MS0, BLINK and INTIN inputs. By selectively bringing this input high, the user will update the attribute only at specific character times; all subsequent characters will carry with them the attributes last updated thus allowing "field" or "embedded" attributes. When using a wide video memory where attribute bits are attached to every character, the internal attribute latch may be updated at each character by tieing this input high (thus allowing for "invisible" attributes).
10	Intensity Out	INTOUT	This output is used in conjunction with the INTIN input to provide a three character pipeline delay to allow for general purpose attributes (such as intensity) to be implemented. See INTIN (pin 7).
11	Cursor	CURSOR	When this input is high and RETBL is low, the programmed cursor format will be displayed. When this input is high, and RETBL is high, the CRT 9021 enters the double width mode. See section entitled cursor formats for details.
12	Retrace Blank	RETBL	When this input is high, the parallel inputs to the video shift register are unconditionally cleared to all zeros and loaded on the next LD/SH pulse. This forces the VIDEO output to a low voltage level, independent of all attributes, for blanking the CRT during horizontal and vertical retrace time.
13	Load/Shift	LD/SH	The 8 bit video shift register parallel-in load or serial-out shift operation is established by the state of this input. When high, this input enables the shift register for serial shifting with each video dot clock pulse (VDC input). When low, the video shift register is parallel loaded on the next video dot clock pulse and all data and attributes are moved to the next position in the internal pipeline. In addition, input data and attributes are latched on the positive transition of LD/SH.
14	Video	VIDEO	The Video output provides the serial dot stream to the CRT. Video is shifted out on the rising edge of the video dot clock VDC. The timing of the LD/SH input will determine the number of backfill dots. See figure 5.
15	Video Dot Clock	VDC	This input clock controls the rate at which video is shifted out on the VIDEO output.
16	Scan line 3/Block Cursor	SL3/BKC	This input has two separate functions depending on the way scan line information is presented to the CRT 9021. *Parallel scan line mode*—This input is the most significant bit of the binary scan line row address. *Serial scan line mode*—This input controls the cursor's physical dimensions. If high the cursor will appear as a reverse video block (the entire character cell will be displayed in reverse video). If low, the cursor will appear as an underline on the scan line(s) programmed.
17	Scan line 2/Blink Cursor	SL2/BLC	This input has two separate functions depending on the way scan line information is presented to the CRT 9021. *Parallel scan line mode*—This input is the second most significant bit of the binary scan line row address. *Serial scan line mode*—This input if low, will cause the cursor to alternate between normal and reverse video at the programmed cursor blink rate. The duty cycle for the cursor blink is 50/50 (on/off). If this input is high, the cursor will be non-blinking.
18	Scan Line 1/Scan Line Gate	SL1/SLG	This input has two separate functions depending on the way scan line information is presented to the CRT 9021. *Parallel scan line mode*—This input is the next to the least significant bit of the binary scan line row address. *Serial scan line mode*—This input will be low for 5 or 6 LD/SH pulses to allow the scan line information to be serially shifted into the serial scan line shift register. If this signal is low for 7 or more LD/SH pulses, the CRT 9021 will assume the parallel input scan line row address mode.
19	Scan line 0/Scan Line data	SL0/SLD	This input has two separate functions depending on the way scan line information is presented to the CRT 9021. Refer to figure 6. *Parallel scan line mode*—This input is the least significant bit of the binary scan line row address. *Serial scan line mode*—This input will present the scan line information in serial form (least significant bit first) to the CRT 9021 and permits the proper scan line information to enter the serial scan line shift register during the LD/SH pulses framed by SLG (pin 18).
20	Ground	GND	Ground
21	Vertical Sync	VSYNC	This input is typically connected to the vertical sync output of the CRT controller and is used as the clock input for the two on-chip mask programmable blink rate dividers. The cursor blink rate (50/50 duty cycle) will always be twice the character blank rate (75/25 duty cycle). In addition, the internal attributes are reset when this input is low. The VSYNC input is also used to determine the scan line mode (parallel or serial) used. See the section "Scan Line Input Modes".

ATTRIBUTES FUNCTION

Retrace Blank —The RETBL input causes the VIDEO to go to the zero (black) level regardless of the state of all other inputs.

Reverse Video —The REVID input causes inverted data to be loaded into the video shift register.

Character Blank —The CHABL input forces the video to go to the current background level as defined by Reverse Video.

Underline —MS1, MSØ = 1, 1 forces the video to go to the inverse of the background level for the scan line(s) programmed for underline.

Blink —The BLINK input will cause characters to blink by forcing the video to the background level 25% of the time and allowing the normal video for 75% of the time. When the cursor is programmed to blink (not controlled by the BLINK input), the video alternates from normal to reverse video at 50% duty cycle. The cursor blink rate always overrides the character blink rate when they both appear at the same character position.

Intensity (Half Intensity) —The INTIN input and the INTOUT output allow an intensity (or half intensity) attribute to be carried through the pipeline of the CRT 9021. An external mixer can be used to combine VIDEO and INTOUT to create the desired video level. See figure 8.

Table 1 illustrates the effect of the REVID, CHABL, UNDLN attributes as a function of the cursor format and the CURSOR and RETBL inputs.

TABLE 1: CRT 9021 ATTRIBUTE COMBINATIONS

CURSOR FORMAT	CRT 9021 INPUTS					VIDEO SHIFT REGISTER LOADED WITH:	
	RETBL	CURSOR	REVID	CHABL	UNDLN		
	1	X	X	X	X	**all zero's**	
	0	0	0	0	0	data	
	0	0	0	0	1	One's for selected scan line(s); Data for all other scan lines.	
X	0	0	0	1	X	All zero's	
	0	0	1	0	0	$\overline{\text{data}}$	
	0	0	1	0	1	Zero's for selected scan line(s); $\overline{\text{data}}$ for all other scan lines.	
	0	0	1	1	X	One's for all scan lines.	
UNDERLINE[2]	0	1	0	0	X[1]	One's for selected scan line(s) for cursor; data for all other scan lines.	
	0	1	0	1	X[1]	One's for selected scan line(s) for cursor; zero's for all other scan lines.	
	0	1	1	0	X[1]	Zero's for selected scan line(s) for cursor; Data for all other scan lines.	
	0	1	1	1	X[1]	Zero's for selected scan line(s) for cursor; one's for all other scan lines.	
BLINKING[3] UNDERLINE[2]	0	1	0	0	X[1]	One's for selected scan line(s) blinking; Data for all other scan lines.	
	0	1	0	1	X[1]	One's for selected scan line(s) blinking; zero's for all other scan lines.	
	0	1	1	0	X[1]	Zero's for selected scan line(s) blinking; Data for all other scan lines.	
	0	1	1	1	X[1]	Zero's for selected scan line(s) blinking; one's for all other scan lines.	
REVID BLOCK	0	1	0	0	0	$\overline{\text{Data}}$ for all scan lines.	
	0	1	0	0	1	Zero's for selected scan line(s) for underline; $\overline{\text{data}}$ for all other scan lines.	
	0	1	0	1	X	One's for all scan lines.	
	0	1	1	0	0	Data for all scan lines	
	0	1	1	0	1	One's for selected scan line(s) for underline; data for all other scan lines.	
	0	1	1	1	X	Zero's for all scan lines.	
BLINKING[3] REVID BLOCK	0	1	0	0	0	On Data for all scan lines.	Off Data for all scan lines.
	0	1	0	0	1	Zero's for selected scan line(s) for underline; Data for all other scan lines.	One's for selected scan line(s) for underline; Data for all other scan lines.
	0	1	0	1	X	One's for all scan lines.	Zero's for all scan lines.
	0	1	1	0	0	Data for all scan lines.	$\overline{\text{Data}}$ for all scan lines.
	0	1	1	0	1	One's for selected scan line(s); Data for all other scan lines.	Zero's for selected scan line(s); Data for all other scan lines.
	0	1	1	1	X	Zero's for all scan lines.	One's for all scan lines.

1 - if the programmed scan line(s) for cursor and underline coincide, the cursor takes precedence; otherwise both are displayed.
2 - at programmed scan line(s) for underline
3 - at cursor blink rate
Note—cursor blink rate overrides character blink rate.

DISPLAY MODES

Inputs MS1 and MS0 select one of four display modes. All attributes except underline operate independent of the display mode used. Figures 8a and 8b illustrate a typical CRT 9021 configuration which operates in all display modes for both the parallel and serial scan line modes respectively.

MS1, MS0 = 00 —Wide Graphics Mode.
In this display mode, inputs D7-D0 define a graphics entity as illustrated in figure 2. Note that individual bits in D7-D0 will illuminate particular portions of the character block. Table 2 shows all programming ranges possible when defining the wide graphic boundaries. No underline is possible in this display mode.

MS1, MS0 = 10 —Thin Graphics Mode.
In this display mode, inputs D7-D0 define a graphic entity as illustrated in figure 3. Note that individual bits in D7-D0 will illuminate particular horizontal or vertical line segments within the character block. Table 3 shows all programming ranges possible when defining the thin graphics boundaries. No underline is possible in this display mode.

MS1, MS0 = 01 —Character Mode Without Underline.
In this display mode, inputs D7-D0 go directly from the input latch to the video shift register via the Attributes and Graphics logic. This mode requires either a bit mapped system RAM (1 bit in RAM equals 1 pixal on the CRT) or an external character generator as shown in figures 8a and 8b.

MS1, MS0 = 11 —Character Mode With Underline.
Same operation as MS1, MS0 = 01 with the underline attribute appearing on the scan line(s) mask programmed.

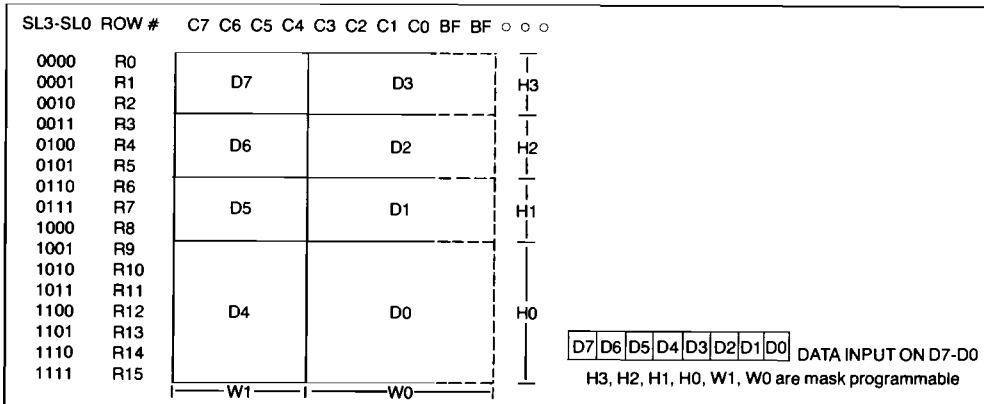


FIGURE 2: WIDE GRAPHICS MODE FOR STANDARD CRT 9021

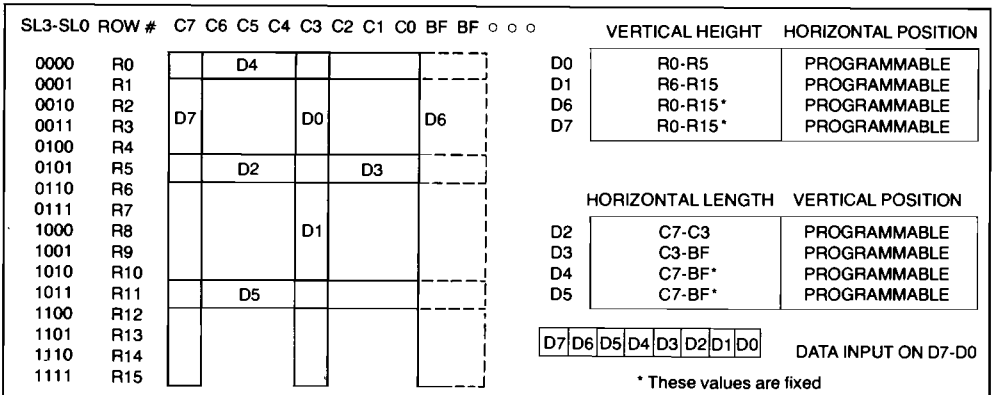


FIGURE 3: THIN GRAPHICS MODE FOR STANDARD CRT 9021

BACKFILL

Backfill is a mechanism that allows a character width of greater than 8 dots and provides dot information (usually blanks) for all dot positions beyond 8. The character width is defined by the period of the $\overline{LD}$/SH input. For the character modes, backfill is added to the tail end of the character by two methods which are mask programmable.

Method A — The backfill (BF) dots will be the same as the dot displayed in position C7.

Method B — The backfill (BF) dots will be the same as the dot displayed in position C0.

For the wide graphics mode, the backfill dots will always be the same as the dot displayed in position C0 (method B) with no programmable option.

CURSOR FORMATS

Four cursor formats are possible with the CRT 9021. If the parallel scan line input mode is used, one of four cursor formats may be selected as a mask programmed option. If the serial scan line input mode is used, the cursor format is selected via input pins 16 and 17 (SL3/BKC, SL2/BLC). See Table 5. The four cursor modes are as follows:

Underline — The cursor will appear as an underline. The position and width of the cursor underline is mask programmed.

Blinking Underline — The cursor will appear as an underline. The underline will alternate between normal and reverse video at the mask programmed cursor blink rate.

Reverse Video Block — The cursor will appear as a reverse video block (The entire character cell will be displayed in reverse video).

Blinking Reverse Video Block — The cursor will appear as a reverse video block and the entire block (character plus background) will alternate between normal and reverse video at the masked programmed cursor blink rate.

Scan Line Input Mode	Pin 17	Pin 16	Cursor Function
Serial	1	0	Underline
	1	1	Reverse Video Block
	0	0	Blinking Underline
	0	1	Blinking Reverse Video Block
Parallel	X	X	Mask programmable Only

TABLE 5: CURSOR FORMATS

DOUBLE WIDTH MODE

In order to display double width characters, video must be shifted out at half frequency and the video shift register must receive new information (parallel load) every other $\overline{LD}$/SH input pulse. In order to divide the video dot clock (VDC) and the $\overline{LD}$/SH pulse internally at the proper time, the cursor input should be pulsed during RETBL prior to the scan line to be displayed as double width. The CURSOR input must remain low for a minimum of 1 $\overline{LD}$/SH period from the leading edge of RETBL. The CURSOR input can stay high for the entire RETBL time but should not extend into active video. If it does, a cursor will be displayed. It is assumed that the CRT controller knows when a particular scan line should be double width and it should activate the CURSOR in the manner just described. Double height/double width characters can also be displayed if the scan line count is incremented by the CRT controller every other scan line. With respect to the CRT 9021, no distinction between double width and double height display is necessary. Figure 4 illustrated timing for both single and double width modes. The CRT 9007, which supports double height double width characters, will produce the CURSOR signal as required by the CRT 9021 with no additional hardware.

SCAN LINE INPUT MODES

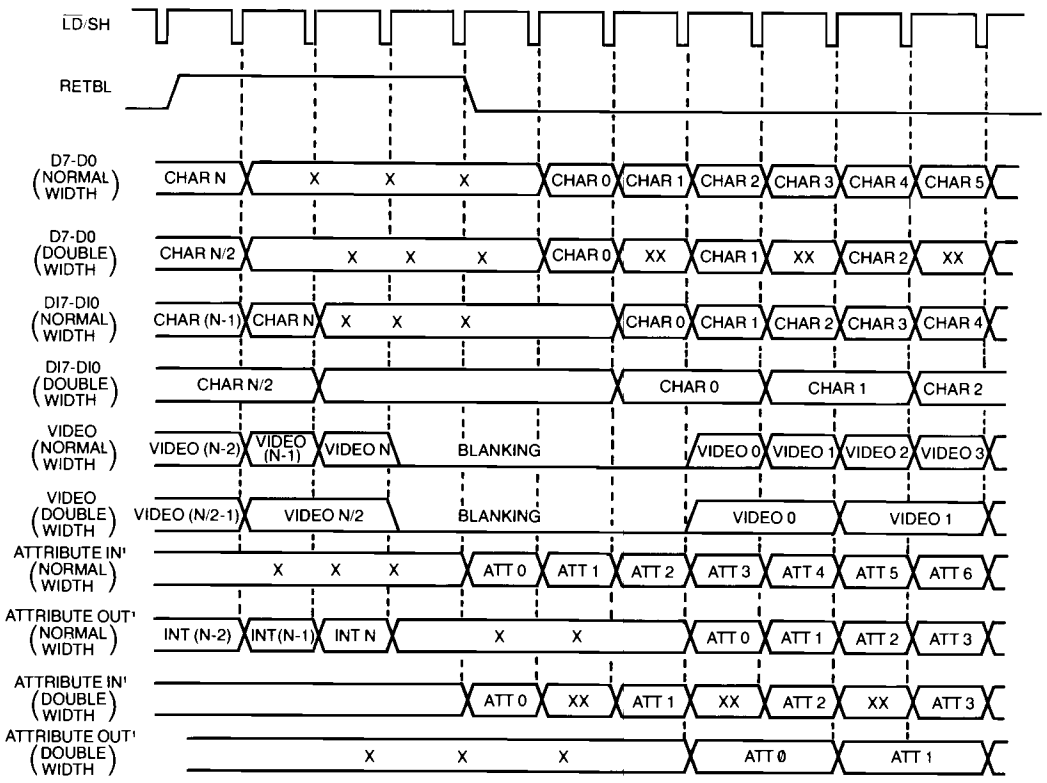
Scan line information can be introduced into the CRT 9021 in parallel format or serial format. Table 6 illustrates the pin definition as a function of the scan line input mode. The CRT 9021 will automatically recognize the proper scan line mode by observing the activity on pin 18. In parallel mode, this input will be stable for at least 1 scan line and in serial mode this input will remain low for about 5 or 6 $\overline{LD}$/SH periods. If pin 18 goes active low for less than seven but more than two continuous $\overline{LD}$/SH periods during the last scan line that has an active low on the $\overline{VSYNC}$ input, the serial mode will be locked in for the next field. The parallel scan line input mode will be selected for the next field if the following two conditions occur during $\overline{VSYNC}$ low time. First, at least one positive transition must occur on pin 18 and second, pin 18 must be low for seven or more $\overline{LD}$/SH periods. Refer to figure 7 for timing details.

Scan Line Input Mode	CRT 9021 Pin Number			
	19	18	17	16
Serial	SLD	$\overline{SLG}$	BLC	BKC
Parallel	SL0	SL1	SL2	SL3

TABLE 6: PIN DEFINITION FOR PARALLEL AND SERIAL SCAN LINE MODES

PROGRAM OPTIONS

The CRT 9021 has a variety of mask programmed options. Tables 2 and 3 illustrate the range of these options for the wide and thin graphics modes respectively. Table 4 illustrates the range of the miscellaneous mask programmed options. In addition, Tables 2, 3 and 4 show the mask programmed options for the standard CRT 9021.



1-Attributes include MS0, MSI, BLINK, CHABL, INTENSITY, REVID

FIGURE 4: CRT 9021 FUNCTIONAL I/O TIMING

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (soldering, 10 sec.)	+325°C
Positive Voltage on any Pin, with respect to ground	.15V
Negative Voltage on any Pin, with respect to ground	−0.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ± 5%, unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
DC CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low Level V_{IL}			0.8	V	
High Level V_{IH1}	2.0			V	All inputs except VDC, $\overline{LD}$/SH
High Level V_{IH2}	4.3			V	For VDC, $\overline{LD}$/SH input
OUTPUT VOLTAGE LEVELS					
Low Level V_{OL}			0.4	V	I_{OL} = 0.4 mA
High Level V_{OH}	2.4			V	I_{OH} = 100μA
INPUT LEAKAGE CURRENT					
Leakage I_{L1}			10	μA	$0 \leq V_{IN} < V_{CC}$; excluding VDC, $\overline{LD}$/SH
Leakage I_{L2}			50	μA	$0 \leq V_{IN} \leq V_{CC}$; for VDC $\overline{LD}$/SH
INPUT CAPACITANCE					
C_{IN1}		10		pf	Excluding VDC, $\overline{LD}$/SH
C_{IN2}		20		pf	For $\overline{LD}$/SH
C_{IN3}		25		pf	For VDC
POWER SUPPLY CURRENT					
I_{CC}		50		mA	

AC CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
VDC[1]					
$1/t_{CY1}$, VDC frequency	1.0		30.0	MHZ	CRT 9021A; see note 1
	1.0		28.5	MHZ	CRT 9021B
t_{CKL} VDC low	10				
t_{CKH} VDC high	10			ns	
t_{CKR} VDC rise time	10		10	ns	Measured from 10% to 90% points
t_{CKF} VDC fall time			10	ns	Measured from 90% to 10% points
$\overline{LD}$/SH					
t_{CY2}	290			ns	CRT 9021A; see note 1
	315			ns	CRT 9021B
t_{S1}	7			ns	
t_{H1}	0			ns	
INPUT SETUP AND HOLD					
t_{S2}	35			ns	
t_{H2}	0			ns	
MISCELLANEOUS TIMING					
t_{PD}			35	ns	C_L = 15 pf
t_{DW}	t_{CY2}				

1-These parameters are Preliminary.

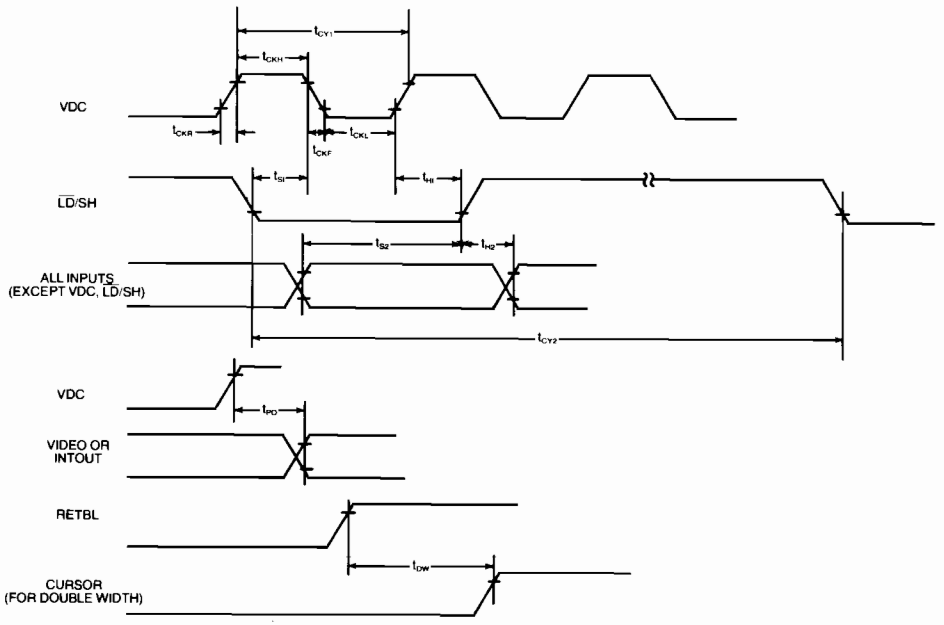


FIGURE 5: CRT 9021 INPUT/OUTPUT TIMING

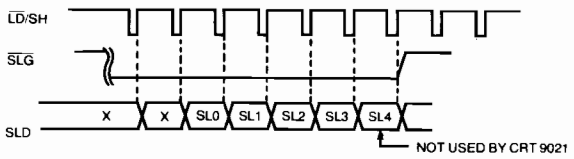


FIGURE 6: SERIAL SCAN LINE MODE TIMING

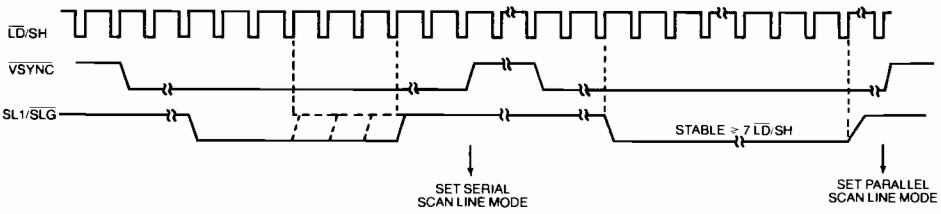


FIGURE 7: SERIAL/PARALLEL SCAN LINE MODE SELECTION TIMING

TABLE 2
WIDE GRAPHICS MASK PROGRAMMING OPTIONS

OPTION	CHOICES	STANDARD CRT 9021
Height of graphic block*		
D7 and D3	any scan line(s)	R0, R1, R2
D6 and D2	any scan line(s)	R3, R4, R5
D5 and D1	any scan line(s)	R6, R7, R8
D4 and D0	any scan line(s)	R9, R10, R11, R12, R13, R14, R15
Width of D7, D6, D5, D4**	any number of dots 0 to 8	C7, C6, C5, C4
Width of D3, D2, D1, D0**	any number of dots 0 to 8	C3, C2, C1, C0, BF

* Any graphic block pair can be removed by programming for zero scan lines.

** Total number of dots for both must be equal to the total dots per character with no overlap.

TABLE 3
THIN GRAPHICS MASK PROGRAMMING OPTIONS

OPTION	CHOICES	STANDARD CRT 9021
Backfill	C1 or C0	C0
Horizontal position for		
D2 and D3	any scan line(s) R0-R15	R5
D4	any scan line(s) R0-R15	R0
D5	any scan line(s) R0-R15	R11
Horizontal length for		
D2[2]	any continuous dots C7-C0, BF	C7-C3
D3[2]	all dots not covered by D2	C3-BF
Blanked dots for serrated horizontal lines		
D2	any dot(s) C7-C0, BF	none
D3	any dot(s) C7-C0, BF	none
D4 and D5	any dot(s) C7-C0, BF	none
Vertical position for		
D0 and D1	any dot(s) C7-C0, BF	C3
D6[1]	any dot(s) C6-C0, BF	BF
D7[1]	any dot(s) C7-C0	C7
Vertical length for		
D0	any scan line(s)	R0 to R5
D1	all scan lines not used by D0	R6 to R15
D6	no choice; always R0-R15	R0 to R15
D7	no choice; always R0-R15	R0 to R15

1-D7 must always come before D6 with no overlap; otherwise D6 is lost.
2-D2 and D3 must always overlap by one and only one dot.

TABLE 4
MISCELLANEOUS MASK PROGRAMMING OPTIONS

OPTION	CHOICES	STANDARD CRT 9021
Backfill in character mode	C7 or C0	C7
Character blink rate (division of $\overline{\text{VSYNC}}$ frequency)	8 to 60; divisible by 4 (7.5 Hz to 1 Hz)[1]	32 (1.875 Hz)[1]
Cursor blink rate[2]	Twice the character blink rate	16 (3.75 Hz)[1]
character underline position	any scan line(s) R0-R15	R11
cursor underline[3]	any scan line(s) R0-R15	not applicable
cursor format[4]	underline Blinking underline Reverse video block Blinking reverse video block	Blinking reverse video block

1 - Assumes $\overline{\text{VSYNC}}$ input frequency of 60 Hz.
2 - Valid only if the cursor is formatted to blink.
3 - Valid only if the cursor is formatted for underline.
4 - Valid for the parallel scan line mode only.

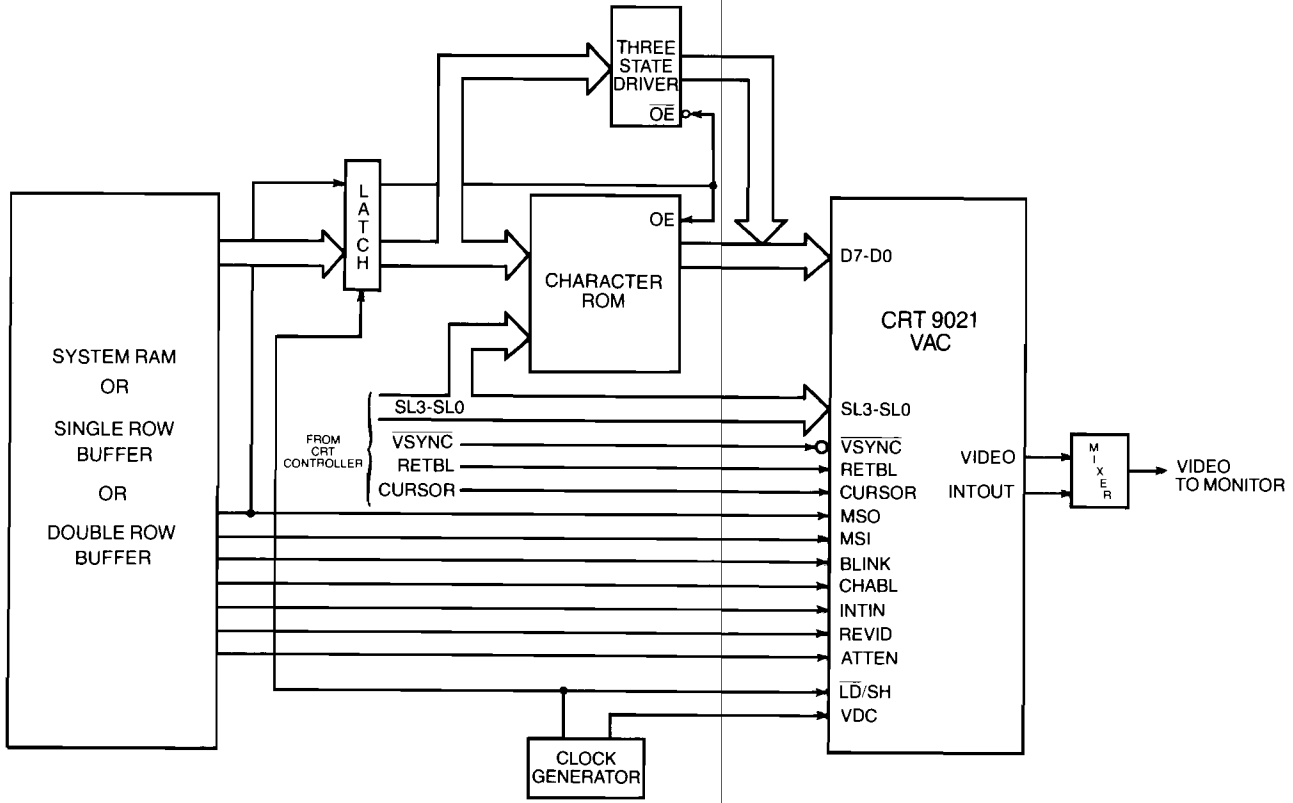


FIGURE 8a: CRT 9021 SYSTEM CONFIGURATION IN PARALLEL SCAN LINE MODE

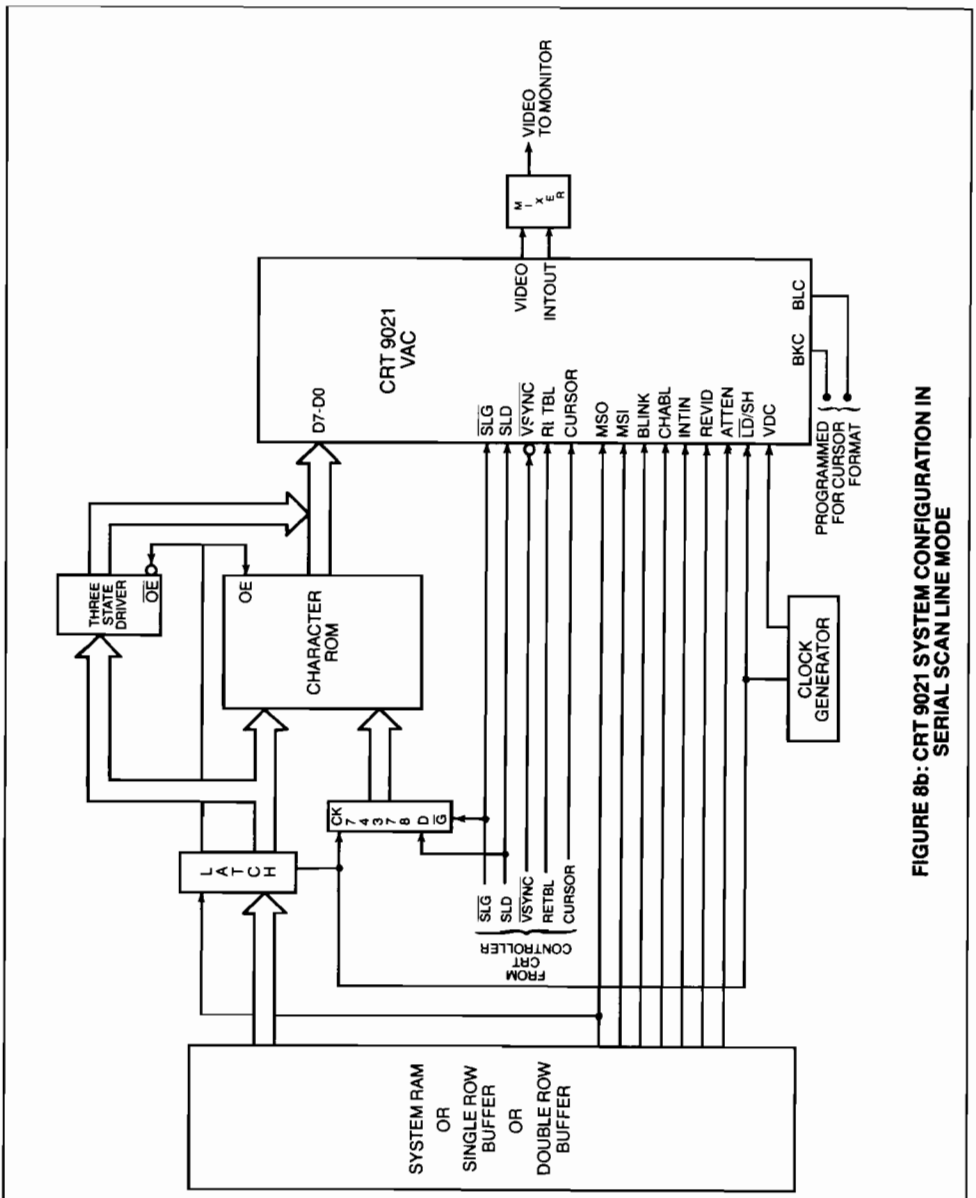


FIGURE 8b: CRT 9021 SYSTEM CONFIGURATION IN SERIAL SCAN LINE MODE

STANDARD MICROSYSTEMS CORPORATION

FDC 9216
FDC 9216B
μPC FAMILY

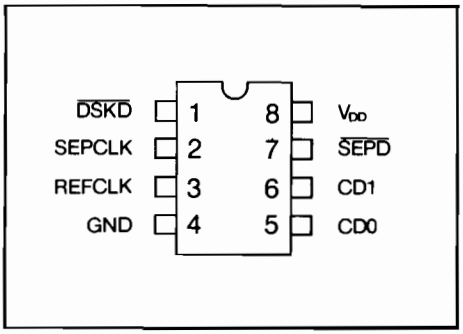
Floppy Disk Data Separator
FDDS

B

FEATURES

- ☐ PERFORMS COMPLETE DATA SEPARATION FUNCTION FOR FLOPPY DISK DRIVES
- ☐ SEPARATES FM OR MFM ENCODED DATA FROM ANY MAGNETIC MEDIA
- ☐ ELIMINATES SEVERAL SSI AND MSI DEVICES NORMALLY USED FOR DATA SEPARATION
- ☐ NO CRITICAL ADJUSTMENTS REQUIRED
- ☐ COMPATIBLE WITH STANDARD MICROSYSTEMS' FDC 1791, FDC 1793 AND OTHER FLOPPY DISK CONTROLLERS
- ☐ SMALL 8-PIN DUAL-IN-LINE PACKAGE
- ☐ +5 VOLT ONLY POWER SUPPLY
- ☐ TTL COMPATIBLE INPUTS AND OUTPUTS

PIN CONFIGURATION



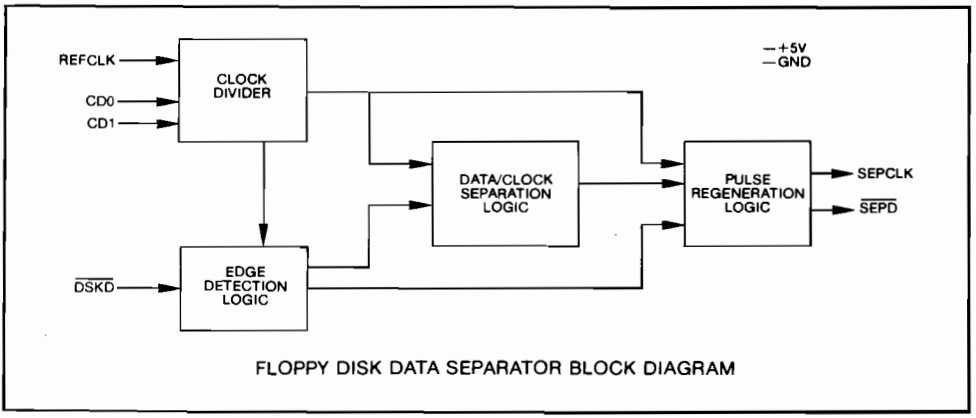
SECTION V

GENERAL DESCRIPTION

The Floppy Disk Data Separator provides a low cost solution to the problem of converting a single stream of pulses from a floppy disk drive into separate Clock and Data inputs for a Floppy Disk Controller.

The FDDS consists primarily of a clock divider, a long-term timing corrector, a short-term timing corrector, and reclocking circuitry. Supplied in an 8-pin Dual-In-Line package to save board real estate, the FDDS operates on +5 volts only and is TTL compatible on all inputs and outputs.

The FDC 9216 is available in two versions; the FDC 9216, which is intended for 5¼" disks and the FDC 9216B for 5¼" and 8" disks.



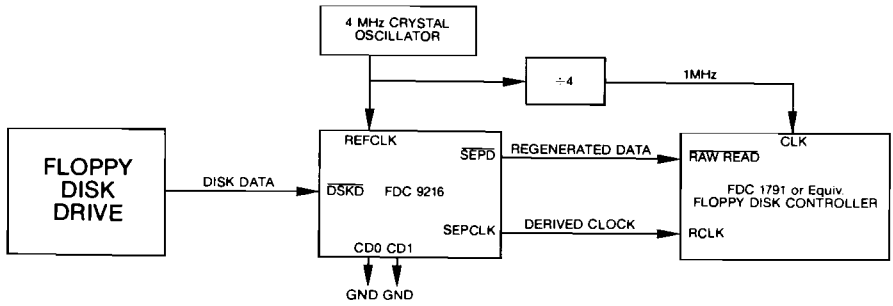
FLOPPY DISK DATA SEPARATOR BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
1	Disk Data	$\overline{DSKD}$	Data input signal direct from disk drive. Contains combined clock and data waveform.
2	Separated Clock	SEPCLK	Clock signal output from the FDDS derived from floppy disk drive serial bit stream.
3	Reference Clock	REFCLK	Reference clock input
4	Ground	GND	Ground
5,6	Clock Divisor	CD0, CD1	CD0 and CD1 control the internal clock divider circuit. The internal clock is a submultiple of the REFCLK according to the following table:
7	Separated Data	$\overline{SEPD}$	SEPD is the data output of the FDDS
8	Power Supply	V_{DD}	+5 volt power supply

CD1	CD0	Divisor
0	0	1
0	1	2
1	0	4
1	1	8

FIGURE 1
TYPICAL SYSTEM CONFIGURATION
(5¼" Drive, Double Density)



OPERATION

A reference clock (REFCLK) of between 2 and 8 MHz is divided by the FDDS to provide an internal clock. The division ratio is selected by inputs CD0 and CD1. The reference clock and division ratio should be chosen per table 1.

The FDDS detects the leading edges of the disk data pulses and adjusts the phase of the internal clock to provide the SEPARATED CLOCK output.

Separate short and long term timing correctors assure accurate clock separation.

The internal clock frequency is nominally 16 times the SEPCLK frequency. Depending on the internal timing correction, the internal clock may be a minimum of 12 times to a maximum of 22 times the SEPCLK frequency.

The reference clock (REFCLK) is divided to provide the internal clock according to pins CD0 and CD1.

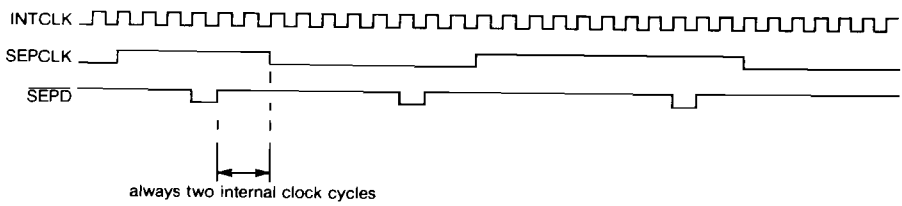
B

SECTION V

TABLE 1:
CLOCK DIVIDER SELECTION TABLE

DRIVE (8" or 5¼")	DENSITY (DD or SD)	REFCLK MHz	CD1	CD0	REMARKS
8	DD	8	0	0	
8	SD	8	0	1	Select either one
8	SD	4	0	0	
5¼	DD	8	0	1	
5¼	DD	4	0	0	Select either one
5¼	SD	8	1	0	
5¼	SD	4	0	1	Select any one
5¼	SD	2	0	0	

FIGURE 2



MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C
Lead Temperature (soldering, 10 sec.) ..... +325°C
Positive Voltage on any Pin, with respect to ground ..... +8.0V
Negative Voltage on any Pin, with respect to ground ..... −0.3V

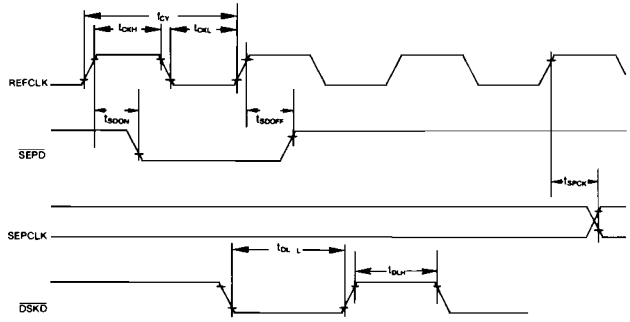
*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists it is suggested that a clamp circuit be used.

ELECTRICAL CHARACTERISTICS (T_A =0°C to 70°C, V_{DD}=+5V±5%, unless otherwise noted)

Parameter		Min.	Typ.	Max.	Units	Comments
D.C. CHARACTERISTICS						
INPUT VOLTAGE LEVELS						
Low Level V_{IL}				0.8	V	
High Level V_{IH}		2.0			V	
OUTPUT VOLTAGE LEVELS						
Low Level V_{OL}				0.4	V	I_{OL}=1.6mA
High Level V_{OH}		2.4			V	I_{OH}=−100 μA
INPUT CURRENT						
Leakage I_{IL}				10	μA	$0 \le V_{IN} \le V_{DD}$
INPUT CAPACITANCE						
All Inputs				10	pF	
POWER SUPPLY CURRENT						
I_{DD}				60	mA	
A.C. CHARACTERISTICS						
Symbol						
f_{cy}	REFCLK Frequency	0.2		4.3	MHz	FDC 9216
f_{cy}	REFCLK Frequency	0.2		8.3	MHz	FDC 9216B
t_{CKH}	REFCLK High Time	50		2500	ns	
t_{CKL}	REFCLK Low Time	50		2500	ns	
t_{SDON}	REFCLK to $\overline{SEPD}$ "ON" Delay		100		ns	
t_{SDOFF}	REFCLK to $\overline{SEPD}$ "OFF" Delay		100		ns	
t_{SPCK}	REFCLK to SEPCLK Delay	100			ns	
t_{DLL}	DSKD Active Low Time	0.1		100	μs	
t_{DLH}	DSKD Active High Time	0.2		100	μs	

FIGURE 3: AC CHARACTERISTICS



C

MODEL 2ØØØ PORT SPECIFICATIONS

DEVICE	ADDRESS	ACCESS	BIT(S)	FUNCTION
LS273	ØØØØ	WR	DØ	KEYBOARD POWER (1=ON)
			D1	EXTERNAL CLOCK ENABLE
			D2	SPEAKER GATE
			D3	SPEAKER DATA
			D4	REFRESH CLOCK GATE (1=ON)
			D5	FDC RESET (Ø=RESET)
			D6	186 TIMER Ø ENABLE (1=ON)
			D7	186 TIMER 1 ENABLE (1=ON)
LS273	ØØØØ	RD	DØ	RS-232 RING INDICATE (Ø=TRUE)
			D1	RS-232 CARRIER DETECT (Ø=TRUE)
			D2-D6	UNDEFINED
			D7	ACLOW (Ø = LOW AC LINE)
LS139	ØØØ2	WR		DMA CONTROL PORT
			DØ	REQUEST Ø ENABLE (1 = ENABLE)
			D1	REQUEST 1 ENABLE (1 = ENABLE)
			D2	REQUEST 2 ENABLE (1 = ENABLE)
			D3	REQUEST 3 ENABLE (1 = ENABLE)
				CHANNEL SELECTS ROUTE DMA REQUESTS TO EITHER CHANNEL Ø OR CHANNEL 1 DRQ'S, A Ø SELECTS DRQØ, A 1 SELECTS DRQ1.
			D4	REQUEST Ø SELECT
			D5	REQUEST 1 SELECT
			D6	REQUEST 2 SELECT
			D7	REQUEST 3 SELECT
8251	ØØ1Ø	RD/WR	DØ-D7	BIDIRECTIONAL DATA BUS TO/FROM 8251 DATA REGISTER
8251	ØØ12	RD/WR	DØ-D7	WRITE CONTROL WORD READ 8251 STATUS
LS138	ØØ2F	RD/WR	XX**	FDC TERMINATE TRANSFER STROBE
8272	ØØ3Ø	RD/WR	DØ-D7	READ - READ MAIN STATUS FDC WRITE - ILLEGAL
8272	ØØ32	RD/WR	DØ-D7	READ - READ DATA REGISTER WRITE - WRITE DATA REGISTER
8253	ØØ4Ø	RD/WR	DØ-D7	WRITE - LOAD COUNTER Ø READ - READ COUNTER Ø
8253	ØØ42	RD/WR	DØ-D7	WRITE - LOAD COUNTER 1 READ - READ COUNTER 1
8253	ØØ44	RD/WR	DØ-D7	WRITE - LOAD COUNTER 2 READ - READ COUNTER 2
8253	ØØ46	RD/WR	DØ-D7	WRITE - LOAD MODE WORD

MODEL 2ØØØ PORT SPECIFICATIONS

DEVICE	ADDRESS	ACCESS	BIT(S)	FUNCTION
				READ - ILLEGAL OPERATION
8255A-5	ØØ5Ø	RD/WR	DØ-D7	BIDIRECTIONAL DATA BUS
8255A-5	ØØ52*	RD	DØ-D7	INPUT KEYBOARD DATA
8255A-5	ØØ52*	RD	DØ-D2	UNDEFINED BITS
			D3	PRINTER ACK*
			D4	PRINTER FAULT*
			D5	SELECT
			D6	PAPER EMPTY
			D7	BUSY
LS244	ØØ52*	RD	DØ-D7	AUX.STATUS BITS
8255A-5	ØØ54	WR	DØ	DIRECTION FOR PORT ØØ5Ø
		WR	D1-D2	SELECTS DEVICE INPUT FOR PORT ØØ52
				D1 D2 SOURCE
				Ø Ø PRINTER STATUS
				Ø 1 READ KBOARD DATA
				1 Ø AUX.STATUS PORT
				1 1 UNDEFINED
			D3	INTRQ FOR LPRINTl3
			D4	STROBE INPUT (AUX INPUT)
			D5	INPUT BUFFER FULL (AUX)
			D6	PRINTER ACKNOWLEDGE
			D7	STROBE TO PRINTER
8259A-2	ØØ6Ø	WR	DØ-D7	WRITE COMMAND WORDS
	ØØ62	RD	DØ-D7	READ STATUS
8259A-2	ØØ7Ø	WR	DØ-D7	WRITE COMMAND WORDS
	ØØ72	RD	DØ-D7	READ STATUS
LS139	ØØ8Ø	RD/WR	DØ-D7	GENERATE DMACKØ
LS139	ØØAØ	RD/WR	DØ-D7	GENERATE DMACK1
LS139	ØØCØ	RD/WR	DØ-D7	GENERATE DMACK2
LS139	ØØEØ	RD/WR	DØ-D7	GENERATE DMACK3

* FOR DETERMINATION OF DEVICE ENABLED AT PORT ØØ52 REFER TO SETTING OF BITS D1 AND D2 OF PORT ØØ54.
** XX = DON'T CARE

9ØØ7	Ø1ØØ	RD	DØ-D7	9ØØ7 RØØ
LS374	Ø1Ø1	WR		ADDRESS CONTROL REGISTER
			D8	A15 OF VIDEO ACCESS
			D9	A16 OF VIDEO ACCESS
			D1Ø	A17 OF VIDEO ACCESS
			D11	A18 OF VIDEO ACCESS
			D12	A19 OF VIDEO ACCESS
			D13	CLOCK SPEED Ø = 22.4 MHZ
				1 = 28 MHZ
			D14	DOTS/CHAR Ø = 1Ø (8ØØX4ØØ)
				1 = 8 (64ØX4ØØ)
			D15	VIDOUT-SEL, SELECTS THE VIDEO SOURCE FOR DISPLAY ON MONOCHROME MONITOR.

MODEL 2ØØØ PORT SPECIFICATIONS

DEVICE	ADDRESS	ACCESS	BIT(S)	FUNCTION
				1 = 9ØØ7, Ø = BUS
9ØØ7	Ø1ØØ	WR	DØ-D7	9ØØ7 RØØ
LS374	Ø1Ø1	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø1Ø2	WR	DØ-D7	9ØØ7 RØ1
LS374	Ø1Ø3	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø1Ø4	WR	DØ-D7	9ØØ7 RØ2
LS374	Ø1Ø5	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø1Ø6	WR	DØ-D7	9ØØ7 RØ3
LS374	Ø1Ø7	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø1Ø8	WR	DØ-D7	9ØØ7 RØ4
LS374	Ø1Ø9	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø1ØA	WR	DØ-D7	9ØØ7 RØ5
LS374	Ø1ØB	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø1ØC	WR	DØ-D7	9ØØ7 RØ6
LS374	Ø1ØD	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø1ØE	WR	DØ-D7	9ØØ7 RØ7
LS374	Ø1ØF	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø11Ø	WR	DØ-D7	9ØØ7 RØ8
LS374	Ø111	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø112	WR	DØ-D7	9ØØ7 RØ9
LS374	Ø113	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø114	WR	DØ-D7	9ØØ7 RØA
LS374	Ø115	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø116	WR	DØ-D7	9ØØ7 RØB
LS374	Ø117	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø118	WR	DØ-D7	9ØØ7 RØC
LS374	Ø119	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø11A	WR	DØ-D7	9ØØ7 RØD
LS374	Ø11B	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø11C	WR	DØ-D7	9ØØ7 RØE
LS374	Ø11D	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø11E	WR	DØ-D7	9ØØ7 RØF
LS374	Ø11F	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø12Ø	WR	DØ-D7	9ØØ7 R1Ø
LS374	Ø121	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø122	WR	DØ-D7	9ØØ7 R11
LS374	Ø123	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø124	WR	DØ-D7	9ØØ7 R12
LS374	Ø125	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø126	WR	DØ-D7	9ØØ7 R13
LS374	Ø127	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø128	WR	DØ-D7	9ØØ7 R14
LS374	Ø129	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø12A	RD/WR	DØ-D7	9ØØ7 R15
LS374	Ø12B	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø12C	RD/WR	DØ-D7	9ØØ7 R16
LS374	Ø12D	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø12E	WR	DØ-D7	9ØØ7 R17
LS374	Ø12F	WR	D8-D15	ADDRESS CONTROL REGISTER

MODEL 2ØØØ PORT SPECIFICATIONS

DEVICE	ADDRESS	ACCESS	BIT(S)	FUNCTION
9ØØ7	Ø13Ø	WR	DØ-D7	9ØØ7 R18
9ØØ7	Ø17Ø	RD	DØ-D7	9ØØ7 R38
LS374	Ø131	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø132	WR	DØ-D7	9ØØ7 R19
9ØØ7	Ø172	RD	DØ-D7	9ØØ7 R39
LS374	Ø133	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø134	WR	DØ-D7	9ØØ7 R1A
LS374	Ø135	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø174	RD	DØ-D7	9ØØ7 R3A
LS374	Ø175	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø176	RD	DØ-D7	9ØØ7 R3B
LS374	Ø177	WR	D8-D15	ADDRESS CONTROL REGISTER
9ØØ7	Ø178	RD	DØ-D7	9ØØ7 R3C
LS374	Ø179	WR	D8-D15	ADDRESS CONTROL REGISTER

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